

## C++ AMP

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To ensure the ongoing accuracy of this book and its companion content, we've reviewed and confirmed the errors listed below. If you find a new error, we hope you'll report it to us on our website: www.microsoftpressstore.com/contact-us/errata.

Page	Location	Description	Date corrected
8	Last line of	Reads:	
	code block	bool bSSEInstructions = (CpuInfo[3] >> 24 && 0x1);	
		Should read:	
		bool bSSEInstructions = (CPUInfo[3] >> 24 & 0x1);	
10	Penultimate	Reads:	
	paragraph, last sentence	For example, this loop is not parallelizable:	
		Should read:	
		For example, this loop is not parallelizable in its current form:	
12	End of	Reads:	
	paragraph	see the "Lambdas in C++11" section in Chapter 2, "NBody Case	
	following the code block	Study," for an overview.	
		Should read:	
		see the "Lambdas in C++11" section in Chapter 3, "C++ AMP	
		Fundamentals," for an overview.	
36	Middle of code	Line reads:	
	block	acc = r * s;	
		Should read:	
		acc +=r*s;	
52	Fourth line of	Reads:	
	code block	parallel_for_each(av.grid, [=](index<1> idx) restrict(amp)	
		Should read:	
		parallel_for_each(av.extent, [=](index<1> idx) restrict(amp)	

Page	Location	Description	Date corrected
74	Last part of code block on page	<pre>Reads: for (int i = 0; i &lt; W; i += TS) { tile_static float sA[TileSize][TileSize]; tile_static float sB[TileSize][TileSize]; sA[row][col] = a(tidx.global[0], col + i); sB[row][col] = b(row + i, tidx.global[1]); for (int k = 0; k &lt; TS; k++) sum += sA[row][k] * sB[k][col]; } Should read: for (int l = 0; l &lt; W; l += TileSize) { tile_static float sA[TileSize][TileSize]; tile_static float sB[TileSize][TileSize]; sA[row][col] = a(tidx.global[0], col + i); sB[row][col] = b(row + l, tidx.global[1]); for (int k = 0; k &lt; TileSize; k++) sum += sA[row][k] * sB[k][col]; } </pre>	
148-149		The author has provided a detailed update and new illustration at http://ampbook.codeplex.com/. To view the updated information, click the Download tab, click the Book Errata link (below "Other Available Downloads"), and after opening the PDF, read the information in the the Chapter 7 section on page 2.	
198	First paragraph, ante- penultimate line	After this sentence: The emulated accelerators, WARP and REF, have warp sizes of 1 and 4, respectively. The following sentence should be added: These numbers may change in the future, so you should not rely on this when implementing applications that run on a wide range of hardware platforms.	
296	Time-Out Detection and Recovery	Currently, the TDR feature is not supported correctly in the NVIDIA and AMD drivers. This is tracked in an issue on CodePlex at http://ampbook.codeplex.com/workitem/33361. Although the code and text in the book is correct, the feature will not work correctly with the current drivers. No accelerator_view_removed is	