

RF MICROELECTRONICS

Second Edition

RF MICROELECTRONICS

Second Edition

Behzad Razavi

Upper Saddle River, NJ • Boston • Indianapolis • San Francisco
New York • Toronto • Montreal • London • Munich • Paris • Madrid
Capetown • Sydney • Tokyo • Singapore • Mexico City

Many of the designations used by manufacturers and sellers to distinguish their products are claimed as trademarks. Where those designations appear in this book, and the publisher was aware of a trademark claim, the designations have been printed with initial capital letters or in all capitals.

The author and publisher have taken care in the preparation of this book, but make no expressed or implied warranty of any kind and assume no responsibility for errors or omissions. No liability is assumed for incidental or consequential damages in connection with or arising out of the use of the information or programs contained herein.

The publisher offers excellent discounts on this book when ordered in quantity for bulk purchases or special sales, which may include electronic versions and/or custom covers and content particular to your business, training goals, marketing focus, and branding interests. For more information, please contact:

U.S. Corporate and Government Sales
(800) 382-3419
corpsales@pearsontechgroup.com

For sales outside the United States, please contact:

International Sales
international@pearson.com

Visit us on the Web: informit.com

Library of Congress Cataloging-in-Publication Data

Razavi, Behzad.

RF microelectronics / Behzad Razavi.—2nd ed.
p. cm.

Includes bibliographical references and index.

ISBN 978-0-13-713473-1 (hardcover : alk. paper) 1. Radio frequency integrated circuits—Design and construction. I. Title.

TK6560.R39 2011

621.384'12—dc23

2011026820

Copyright © 2012 Pearson Education, Inc.

All rights reserved. Printed in the United States of America. This publication is protected by copyright, and permission must be obtained from the publisher prior to any prohibited reproduction, storage in a retrieval system, or transmission in any form or by any means, electronic, mechanical, photocopying, recording, or likewise. To obtain permission to use material from this work, please submit a written request to Pearson Education, Inc., Permissions Department, One Lake Street, Upper Saddle River, New Jersey 07458, or you may fax your request to (201) 236-3290.

ISBN-13: 978-0-13-713473-1

ISBN-10: 0-13-713473-8

Text printed in the United States at Hamilton Printing Company in Castleton, New York.
First printing, September 2011

Publisher
Paul Boger

Acquisitions Editor
Bernard Goodwin

Managing Editor
John Fuller

**Full-Service Production
Manager**
Julie B. Nahil

Copy Editor
Geneil Breeze

Indexer
Ted Laux

Proofreader
Linda Seifert

Publishing Coordinator
Michelle Housley

Cover Designer
Gary Adair

Compositor
LaurelTech

To the memory of my parents

This page intentionally left blank

CONTENTS

PREFACE TO THE SECOND EDITION	xv
PREFACE TO THE FIRST EDITION	xix
ACKNOWLEDGMENTS	xxi
ABOUT THE AUTHOR	xxiii

CHAPTER 1 INTRODUCTION TO RF AND WIRELESS TECHNOLOGY **1**

1.1 A Wireless World	1
1.2 RF Design Is Challenging	3
1.3 The Big Picture	4
References	5

CHAPTER 2 BASIC CONCEPTS IN RF DESIGN **7**

2.1 General Considerations	7
2.1.1 Units in RF Design	7
2.1.2 Time Variance	9
2.1.3 Nonlinearity	12
2.2 Effects of Nonlinearity	14
2.2.1 Harmonic Distortion	14
2.2.2 Gain Compression	16
2.2.3 Cross Modulation	20
2.2.4 Intermodulation	21
2.2.5 Cascaded Nonlinear Stages	29
2.2.6 AM/PM Conversion	33
2.3 Noise	35
2.3.1 Noise as a Random Process	36
2.3.2 Noise Spectrum	37

2.3.3	Effect of Transfer Function on Noise	39
2.3.4	Device Noise	40
2.3.5	Representation of Noise in Circuits	46
2.4	Sensitivity and Dynamic Range	58
2.4.1	Sensitivity	59
2.4.2	Dynamic Range	60
2.5	Passive Impedance Transformation	62
2.5.1	Quality Factor	63
2.5.2	Series-to-Parallel Conversion	63
2.5.3	Basic Matching Networks	65
2.5.4	Loss in Matching Networks	69
2.6	Scattering Parameters	71
2.7	Analysis of Nonlinear Dynamic Systems	75
2.7.1	Basic Considerations	75
2.8	Volterra Series	77
2.8.1	Method of Nonlinear Currents	81
	References	86
	Problems	86
CHAPTER 3 COMMUNICATION CONCEPTS		91
3.1	General Considerations	91
3.2	Analog Modulation	93
3.2.1	Amplitude Modulation	93
3.2.2	Phase and Frequency Modulation	95
3.3	Digital Modulation	99
3.3.1	Intersymbol Interference	101
3.3.2	Signal Constellations	105
3.3.3	Quadrature Modulation	107
3.3.4	GMSK and GFSK Modulation	112
3.3.5	Quadrature Amplitude Modulation	114
3.3.6	Orthogonal Frequency Division Multiplexing	115
3.4	Spectral Regrowth	118
3.5	Mobile RF Communications	119
3.6	Multiple Access Techniques	123
3.6.1	Time and Frequency Division Duplexing	123
3.6.2	Frequency-Division Multiple Access	125
3.6.3	Time-Division Multiple Access	125
3.6.4	Code-Division Multiple Access	126
3.7	Wireless Standards	130
3.7.1	GSM	132
3.7.2	IS-95 CDMA	137
3.7.3	Wideband CDMA	139
3.7.4	Bluetooth	143
3.7.5	IEEE802.11a/b/g	147

3.8	Appendix I: Differential Phase Shift Keying	151
	References	152
	Problems	152
CHAPTER 4	TRANSCEIVER ARCHITECTURES	155
4.1	General Considerations	155
4.2	Receiver Architectures	160
4.2.1	Basic Heterodyne Receivers	160
4.2.2	Modern Heterodyne Receivers	171
4.2.3	Direct-Conversion Receivers	179
4.2.4	Image-Reject Receivers	200
4.2.5	Low-IF Receivers	214
4.3	Transmitter Architectures	226
4.3.1	General Considerations	226
4.3.2	Direct-Conversion Transmitters	227
4.3.3	Modern Direct-Conversion Transmitters	238
4.3.4	Heterodyne Transmitters	244
4.3.5	Other TX Architectures	248
4.4	OOK Transceivers	248
	References	249
	Problems	250
CHAPTER 5	LOW-NOISE AMPLIFIERS	255
5.1	General Considerations	255
5.2	Problem of Input Matching	263
5.3	LNA Topologies	266
5.3.1	Common-Source Stage with Inductive Load	266
5.3.2	Common-Source Stage with Resistive Feedback	269
5.3.3	Common-Gate Stage	272
5.3.4	Cascode CS Stage with Inductive Degeneration	284
5.3.5	Variants of Common-Gate LNA	296
5.3.6	Noise-Cancelling LNAs	300
5.3.7	Reactance-Cancelling LNAs	303
5.4	Gain Switching	305
5.5	Band Switching	312
5.6	High-IP ₂ LNAs	313
5.6.1	Differential LNAs	314
5.6.2	Other Methods of IP ₂ Improvement	323
5.7	Nonlinearity Calculations	325
5.7.1	Degenerated CS Stage	325
5.7.2	Undegenerated CS Stage	329
5.7.3	Differential and Quasi-Differential Pairs	331
5.7.4	Degenerated Differential Pair	332
	References	333
	Problems	333

CHAPTER 6 MIXERS	337
6.1 General Considerations	337
6.1.1 Performance Parameters	338
6.1.2 Mixer Noise Figures	343
6.1.3 Single-Balanced and Double-Balanced Mixers	348
6.2 Passive Downconversion Mixers	350
6.2.1 Gain	350
6.2.2 LO Self-Mixing	357
6.2.3 Noise	357
6.2.4 Input Impedance	364
6.2.5 Current-Driven Passive Mixers	366
6.3 Active Downconversion Mixers	368
6.3.1 Conversion Gain	370
6.3.2 Noise in Active Mixers	377
6.3.3 Linearity	387
6.4 Improved Mixer Topologies	393
6.4.1 Active Mixers with Current-Source Helpers	393
6.4.2 Active Mixers with Enhanced Transconductance	394
6.4.3 Active Mixers with High IP_2	397
6.4.4 Active Mixers with Low Flicker Noise	405
6.5 Upconversion Mixers	408
6.5.1 Performance Requirements	408
6.5.2 Upconversion Mixer Topologies	409
References	424
Problems	425
CHAPTER 7 PASSIVE DEVICES	429
7.1 General Considerations	429
7.2 Inductors	431
7.2.1 Basic Structure	431
7.2.2 Inductor Geometries	435
7.2.3 Inductance Equations	436
7.2.4 Parasitic Capacitances	439
7.2.5 Loss Mechanisms	444
7.2.6 Inductor Modeling	455
7.2.7 Alternative Inductor Structures	460
7.3 Transformers	470
7.3.1 Transformer Structures	470
7.3.2 Effect of Coupling Capacitance	475
7.3.3 Transformer Modeling	475
7.4 Transmission Lines	476
7.4.1 T-Line Structures	478
7.5 Varactors	483
7.6 Constant Capacitors	490
7.6.1 MOS Capacitors	491
7.6.2 Metal-Plate Capacitors	493

References	495
Problems	496
CHAPTER 8 OSCILLATORS	497
8.1 Performance Parameters	497
8.2 Basic Principles	501
8.2.1 Feedback View of Oscillators	502
8.2.2 One-Port View of Oscillators	508
8.3 Cross-Coupled Oscillator	511
8.4 Three-Point Oscillators	517
8.5 Voltage-Controlled Oscillators	518
8.5.1 Tuning Range Limitations	521
8.5.2 Effect of Varactor Q	522
8.6 LC VCOs with Wide Tuning Range	524
8.6.1 VCOs with Continuous Tuning	524
8.6.2 Amplitude Variation with Frequency Tuning	532
8.6.3 Discrete Tuning	532
8.7 Phase Noise	536
8.7.1 Basic Concepts	536
8.7.2 Effect of Phase Noise	539
8.7.3 Analysis of Phase Noise: Approach I	544
8.7.4 Analysis of Phase Noise: Approach II	557
8.7.5 Noise of Bias Current Source	565
8.7.6 Figures of Merit of VCOs	570
8.8 Design Procedure	571
8.8.1 Low-Noise VCOs	573
8.9 LO Interface	575
8.10 Mathematical Model of VCOs	577
8.11 Quadrature Oscillators	581
8.11.1 Basic Concepts	581
8.11.2 Properties of Coupled Oscillators	584
8.11.3 Improved Quadrature Oscillators	589
8.12 Appendix I: Simulation of Quadrature Oscillators	592
References	593
Problems	594
CHAPTER 9 PHASE-LOCKED LOOPS	597
9.1 Basic Concepts	597
9.1.1 Phase Detector	597
9.2 Type-I PLLs	600
9.2.1 Alignment of a VCO's Phase	600
9.2.2 Simple PLL	601
9.2.3 Analysis of Simple PLL	603
9.2.4 Loop Dynamics	606
9.2.5 Frequency Multiplication	609
9.2.6 Drawbacks of Simple PLL	611

9.3	Type-II PLLs	611
9.3.1	Phase/Frequency Detectors	612
9.3.2	Charge Pumps	614
9.3.3	Charge-Pump PLLs	615
9.3.4	Transient Response	620
9.3.5	Limitations of Continuous-Time Approximation	622
9.3.6	Frequency-Multiplying CPPLL	623
9.3.7	Higher-Order Loops	625
9.4	PFD/CP Nonidealities	627
9.4.1	Up and Down Skew and Width Mismatch	627
9.4.2	Voltage Compliance	630
9.4.3	Charge Injection and Clock Feedthrough	630
9.4.4	Random Mismatch between Up and Down Currents	632
9.4.5	Channel-Length Modulation	633
9.4.6	Circuit Techniques	634
9.5	Phase Noise in PLLs	638
9.5.1	VCO Phase Noise	638
9.5.2	Reference Phase Noise	643
9.6	Loop Bandwidth	645
9.7	Design Procedure	646
9.8	Appendix I: Phase Margin of Type-II PLLs	647
	References	651
	Problems	652
CHAPTER 10 INTEGER-N FREQUENCY SYNTHESIZERS		655
10.1	General Considerations	655
10.2	Basic Integer- N Synthesizer	659
10.3	Settling Behavior	661
10.4	Spur Reduction Techniques	664
10.5	PLL-Based Modulation	667
10.5.1	In-Loop Modulation	667
10.5.2	Modulation by Offset PLLs	670
10.6	Divider Design	673
10.6.1	Pulse Swallow Divider	674
10.6.2	Dual-Modulus Dividers	677
10.6.3	Choice of Prescaler Modulus	682
10.6.4	Divider Logic Styles	683
10.6.5	Miller Divider	699
10.6.6	Injection-Locked Dividers	707
10.6.7	Divider Delay and Phase Noise	709
	References	712
	Problems	713

CHAPTER 11	FRACTIONAL-N SYNTHESIZERS	715
11.1	Basic Concepts	715
11.2	Randomization and Noise Shaping	718
11.2.1	Modulus Randomization	718
11.2.2	Basic Noise Shaping	722
11.2.3	Higher-Order Noise Shaping	728
11.2.4	Problem of Out-of-Band Noise	732
11.2.5	Effect of Charge Pump Mismatch	733
11.3	Quantization Noise Reduction Techniques	738
11.3.1	DAC Feedforward	738
11.3.2	Fractional Divider	742
11.3.3	Reference Doubling	743
11.3.4	Multiphase Frequency Division	745
11.4	Appendix I: Spectrum of Quantization Noise	748
	References	749
	Problems	749
CHAPTER 12	POWER AMPLIFIERS	751
12.1	General Considerations	751
12.1.1	Effect of High Currents	754
12.1.2	Efficiency	755
12.1.3	Linearity	756
12.1.4	Single-Ended and Differential PAs	758
12.2	Classification of Power Amplifiers	760
12.2.1	Class A Power Amplifiers	760
12.2.2	Class B Power Amplifiers	764
12.2.3	Class C Power Amplifiers	768
12.3	High-Efficiency Power Amplifiers	770
12.3.1	Class A Stage with Harmonic Enhancement	771
12.3.2	Class E Stage	772
12.3.3	Class F Power Amplifiers	775
12.4	Cascode Output Stages	776
12.5	Large-Signal Impedance Matching	780
12.6	Basic Linearization Techniques	782
12.6.1	Feedforward	783
12.6.2	Cartesian Feedback	786
12.6.3	Predistortion	787
12.6.4	Envelope Feedback	788
12.7	Polar Modulation	790
12.7.1	Basic Idea	790
12.7.2	Polar Modulation Issues	793
12.7.3	Improved Polar Modulation	796

12.8	Outphasing	802
12.8.1	Basic Idea	802
12.8.2	Outphasing Issues	805
12.9	Doherty Power Amplifier	811
12.10	Design Examples	814
12.10.1	Cascode PA Examples	815
12.10.2	Positive-Feedback PAs	819
12.10.3	PAs with Power Combining	821
12.10.4	Polar Modulation PAs	824
12.10.5	Outphasing PA Example	826
	References	830
	Problems	831
CHAPTER 13 TRANSCEIVER DESIGN EXAMPLE		833
13.1	System-Level Considerations	833
13.1.1	Receiver	834
13.1.2	Transmitter	838
13.1.3	Frequency Synthesizer	840
13.1.4	Frequency Planning	844
13.2	Receiver Design	848
13.2.1	LNA Design	849
13.2.2	Mixer Design	851
13.2.3	AGC	856
13.3	TX Design	861
13.3.1	PA Design	861
13.3.2	Upconverter	867
13.4	Synthesizer Design	869
13.4.1	VCO Design	869
13.4.2	Divider Design	878
13.4.3	Loop Design	882
	References	886
	Problems	886
INDEX		889

PREFACE TO THE SECOND EDITION

In the 14 years since the first edition of this book, RF IC design has experienced a dramatic metamorphosis. Innovations in transceiver architectures, circuit topologies, and device structures have led to highly-integrated “radios” that span a broad spectrum of applications. Moreover, new analytical and modeling techniques have considerably improved our understanding of RF circuits and their underlying principles. A new edition was therefore due.

The second edition differs from the first in several respects:

1. I realized at the outset—three-and-a-half years ago—that simply adding “patches” to the first edition would not reflect today’s RF microelectronics. I thus closed the first edition and began with a clean slate. The two editions have about 10% overlap.
2. I wanted the second edition to contain greater pedagogy, helping the reader understand both the fundamentals and the subtleties. I have thus incorporated hundreds of examples and problems.
3. I also wanted to teach *design* in addition to analysis. I have thus included step-by-step design procedures and examples. Furthermore, I have dedicated Chapter 13 to the step-by-step transistor-level design of a dual-band WiFi transceiver.
4. With the tremendous advances in RF design, some of the chapters have inevitably become longer and some have been split into two or more chapters. As a result, the second edition is nearly three times as long as the first.

Suggestions for Instructors and Students

The material in this book is much more than can be covered in one quarter or semester. The following is a possible sequence of the chapters that can be taught in one term with reasonable depth. Depending on the students’ background and the instructor’s preference, other combinations of topics can also be covered in one quarter or semester.

Chapter 1: Introduction to RF and Wireless Technology

This chapter provides the big picture and should be covered in about half an hour.

Chapter 2: Basic Concepts in RF Design

The following sections should be covered: General Considerations, Effects of Nonlinearity (the section on AM/PM Conversion can be skipped), Noise, and Sensitivity and Dynamic Range. (The sections on Passive Impedance Transformation, Scattering Parameters, and Analysis of Nonlinear Dynamic Systems can be skipped.) This chapter takes about six hours of lecture.

Chapter 3: Communication Concepts

This chapter can be covered minimally in a quarter system—for example, Analog Modulation, Quadrature Modulation, GMSK Modulation, Multiple Access Techniques, and the IEEE802.11a/b/g Standard. In a semester system, the concept of signal constellations can be introduced and a few more modulation schemes and wireless standards can be taught. This chapter takes about two hours in a quarter system and three hours in a semester system.

Chapter 4: Transceiver Architectures

This chapter is relatively long and should be taught selectively. The following sections should be covered: General Considerations, Basic and Modern Heterodyne Receivers, Direct-Conversion Receivers, Image-Reject Receivers, and Direct-Conversion Transmitters. In a semester system, Low-IF Receivers and Heterodyne Transmitters can be covered as well. This chapter takes about eight hours in a quarter system and ten hours in a semester system.

Chapter 5: Low-Noise Amplifiers

The following sections should be covered: General Considerations, Problem of Input Matching, and LNA Topologies. A semester system can also include Gain Switching and Band Switching or High-IP₂ LNAs. This chapter takes about six hours in a quarter system and eight hours in a semester system.

Chapter 6: Mixers

The following sections should be covered: General Considerations, Passive Downconversion Mixers (the computation of noise and input impedance of voltage-driven sampling mixers can be skipped), Active Downconversion Mixers, and Active Mixers with High IP₂. In a semester system, Active Mixers with Enhanced Transconductance, Active Mixers with Low Flicker Noise, and Upconversion Mixers can also be covered. This chapter takes about eight hours in a quarter system and ten hours in a semester system.

Chapter 7: Passive Devices

This chapter may not fit in a quarter system. In a semester system, about three hours can be spent on basic inductor structures and loss mechanisms and MOS varactors.

Chapter 8: Oscillators

This is a long chapter and should be taught selectively. The following sections should be covered: Basic Principles, Cross-Coupled Oscillator, Voltage-Controlled

Oscillators, Low-Noise VCOs. In a quarter system, there is little time to cover phase noise. In a semester system, both approaches to phase noise analysis can be taught. This chapter takes about six hours in a quarter system and eight hours in a semester system.

Chapter 9: Phase-Locked Loops

This chapter forms the foundation for synthesizers. In fact, if taught carefully, this chapter naturally teaches integer-N synthesizers, allowing a quarter system to skip the next chapter. The following sections should be covered: Basic Concepts, Type-I PLLs, Type-II PLLs, and PFD/CP Nonidealities. A semester system can also include Phase Noise in PLLs and Design Procedure. This chapter takes about four hours in a quarter system and six hours in a semester system.

Chapter 10: Integer-N Synthesizers

This chapter is likely sacrificed in a quarter system. A semester system can spend about four hours on Spur Reduction Techniques and Divider Design.

Chapter 11: Fractional-N Synthesizers

This chapter is likely sacrificed in a quarter system. A semester system can spend about four hours on Randomization and Noise Shaping. The remaining sections may be skipped.

Chapter 12: Power Amplifiers

This is a long chapter and, unfortunately, is often sacrificed for other chapters. If coverage is desired, the following sections may be taught: General Considerations, Classification of Power Amplifiers, High-Efficiency Power Amplifiers, Cascode Output Stages, and Basic Linearization Techniques. These topics take about four hours of lecture. Another four hours can be spent on Doherty Power Amplifier, Polar Modulation, and Outphasing.

Chapter 13: Transceiver Design Example

This chapter provides a step-by-step design of a dual-band transceiver. It is possible to skip the state-of-the-art examples in Chapters 5, 6, and 8 to allow some time for this chapter. The system-level derivations may still need to be skipped. The RX, TX, and synthesizer transistor-level designs can be covered in about four hours.

A solutions manual is available for instructors via the Pearson Higher Education Instructor Resource Center web site: pearsonhighered.com/irc; and a set of Powerpoint slides is available for instructors at informit.com/razavi. Additional problems will be posted on the book's website (informit.com/razavi).

—Behzad Razavi
July 2011

This page intentionally left blank

PREFACE TO THE FIRST EDITION

The annual worldwide sales of cellular phones has exceeded \$2.5B. With 4.5 million customers, home satellite networks comprise a \$2.5B industry. The global positioning system is expected to become a \$5B market by the year 2000. In Europe, the sales of equipment and services for mobile communications will reach \$30B by 1998. The statistics are overwhelming.

The radio frequency (RF) and wireless market has suddenly expanded to unimaginable dimensions. Devices such as pagers, cellular and cordless phones, cable modems, and RF identification tags are rapidly penetrating all aspects of our lives, evolving from luxury items to indispensable tools. Semiconductor and system companies, small and large, analog and digital, have seen the statistics and are striving to capture their own market share by introducing various RF products.

RF design is unique in that it draws upon many disciplines unrelated to integrated circuits (ICs). The RF knowledge base has grown for almost a century, creating a seemingly endless body of literature for the novice.

This book deals with the analysis and design of RF integrated circuits and systems. Providing a systematic treatment of RF electronics in a tutorial language, the book begins with the necessary background knowledge from microwave and communication theory and leads the reader to the design of RF transceivers and circuits. The text emphasizes both architecture and circuit level issues with respect to monolithic implementation in VLSI technologies. The primary focus is on bipolar and CMOS design, but most of the concepts can be applied to other technologies as well. The reader is assumed to have a basic understanding of analog IC design and the theory of signals and systems.

The book consists of nine chapters. Chapter 1 gives a general introduction, posing questions and providing motivation for subsequent chapters. Chapter 2 describes basic concepts in RF and microwave design, emphasizing the effects of nonlinearity and noise.

Chapters 3 and 4 take the reader to the communication system level, giving an overview of modulation, detection, multiple access techniques, and wireless standards. While initially appearing to be unnecessary, this material is in fact essential to the concurrent design of RF circuits and systems.

Chapter 5 deals with transceiver architectures, presenting various receiver and transmitter topologies along with their merits and drawbacks. This chapter also includes a number of case studies that exemplify the approaches taken in actual RF products.

Chapters 6 through 9 address the design of RF building blocks: low-noise amplifiers and mixers, oscillators, frequency synthesizers, and power amplifiers, with particular attention to minimizing the number of off-chip components. An important goal of these chapters is to demonstrate how the system requirements define the parameters of the circuits and how the performance of each circuit impacts that of the overall transceiver.

I have taught approximately 80% of the material in this book in a 4-unit graduate course at UCLA. Chapters 3, 4, 8, and 9 had to be shortened in a ten-week quarter, but in a semester system they can be covered more thoroughly.

Much of my RF design knowledge comes from interactions with colleagues. Helen Kim, Ting-Ping Liu, and Dan Avidor of Bell Laboratories, and David Su and Andrew Gzegorek of Hewlett-Packard Laboratories have contributed to the material in this book in many ways. The text was also reviewed by a number of experts: Stefan Heinen (Siemens), Bart Jansen (Hewlett-Packard), Ting-Ping Liu (Bell Labs), John Long (University of Toronto), Tadao Nakagawa (NTT), Gitty Nasserbakht (Texas Instruments), Ted Rappaport (Virginia Tech), Tirdad Sowlati (Gennum), Trudy Stetzler (Bell Labs), David Su (Hewlett-Packard), and Rick Wesel (UCLA). In addition, a number of UCLA students, including Farbod Behbahani, Hooman Darabi, John Leete, and Jacob Rael, “test drove” various chapters and provided useful feedback. I am indebted to all of the above for their kind assistance.

I would also like to thank the staff at Prentice Hall, particularly Russ Hall, Maureen Diana, and Kerry Riordan for their support.

—*Behzad Razavi*
July 1997

ACKNOWLEDGMENTS

I have been fortunate to benefit from the support of numerous people during the writing, review, and production phases of this book. I would like to express my thanks here.

Even after several rounds of self-editing, it is possible that typos or subtle mistakes have eluded the author. Sometimes, an explanation that is clear to the author may not be so to the reader. And, occasionally, the author may have missed a point or a recent development. A detailed review of the book by others thus becomes necessary. The following individuals meticulously reviewed various chapters, discovered my mistakes, and made valuable suggestions:

Ali Afsahi (Broadcom)	Abbas Komijani (Atheros)
Pietro Andreani (Lund University)	Tai-Cheng Lee (National Taiwan University)
Ashkan Borna (UC Berkeley)	Antonio Liscidini (University of Pavia)
Jonathan Borremans (IMEC)	Shen-Iuan Liu (National Taiwan University)
Debopriyo Chowdhury (UC Berkeley)	Xiaodong Liu (Lund University)
Matteo Conta (Consultant)	Jian Hua Lu (UCLA)
Ali Homayoun (UCLA)	Howard Luong (Hong Kong University of Science and Technology)
Velintina del Lattorre (Consultant)	Elvis Mak (University of Macau)
Jane Gu (University of Florida)	Rabih Makarem (Atheros)
Peng Han (Beken)	Rui Martins (University of Macau)
Pavan Hanumolu (Oregon State University)	Andrea Mazzanti (University of Pavia)
Daquan Huang (Texas Instruments)	Karthik Natarajan (University of Washington)
Sy-Chyuan Hwu (UCLA)	Nitin Nidhi (UCLA)
Amin Jahanian (UCI)	Joung Park (UCLA)
Jithin Janardhan (UCLA)	Paul Park (Atheros)
Shinwon Kang (UC Berkeley)	Stefano Pellerano (Intel)
Iman Khajenasiri (Sharif University of Technology)	Jafar Savoj (Xilinx)
Yanghyo Kim (UCLA)	

Parmoon Seddighrad (University of Washington)	Vidojkovic Vojkan (IMEC)
Alireza Shirvani (Ralink)	Ning Wang (UCLA)
Tirdad Sowlati (Qualcomm)	Weifeng Wang (Beken)
Francesco Svelto (University of Pavia)	Zhi Gong Wang (Southeast University)
Enrico Temporiti (ST Microelectronics)	Marco Zanuso (UCLA)
Federico Vecchi (University of Pavia)	Yunfeng Zhao (Beken)
Vijay Viswam (Lund University)	Alireza Zolfaghari (Broadcom)

I am thankful for their enthusiastic, organized, and to-the-point reviews.

The book's production was proficiently managed by the staff at Prentice Hall, including Bernard Goodwin and Julie Nahil. I would like to thank both.

As with my other books, my wife, Angelina, typed the entire second edition in Latex and selflessly helped me in this three-and-a-half-year endeavor. I am grateful to her.

—*Behzad Razavi*

ABOUT THE AUTHOR

Behzad Razavi received the BSEE degree from Sharif University of Technology in 1985 and MSEE and PhDEE degrees from Stanford University in 1988 and 1992, respectively. He was with AT&T Bell Laboratories and Hewlett-Packard Laboratories until 1996. Since 1996, he has been associate professor and, subsequently, professor of electrical engineering at University of California, Los Angeles. His current research includes wireless transceivers, frequency synthesizers, phase-locking and clock recovery for high-speed data communications, and data converters.

Professor Razavi was an adjunct professor at Princeton University from 1992 to 1994, and at Stanford University in 1995. He served on the Technical Program Committees of the International Solid-State Circuits Conference (ISSCC) from 1993 to 2002 and VLSI Circuits Symposium from 1998 to 2002. He has also served as guest editor and associate editor of the *IEEE Journal of Solid-State Circuits*, *IEEE Transactions on Circuits and Systems*, and *International Journal of High Speed Electronics*.

Professor Razavi received the Beatrice Winner Award for Editorial Excellence at the 1994 ISSCC; the best paper award at the 1994 European Solid-State Circuits Conference; the best panel award at the 1995 and 1997 ISSCC; the TRW Innovative Teaching Award in 1997; the best paper award at the IEEE Custom Integrated Circuits Conference (CICC) in 1998; and McGraw-Hill First Edition of the Year Award in 2001. He was the co-recipient of both the Jack Kilby Outstanding Student Paper Award and the Beatrice Winner Award for Editorial Excellence at the 2001 ISSCC. He received the Lockheed Martin Excellence in Teaching Award in 2006; the UCLA Faculty Senate Teaching Award in 2007; and the CICC Best Invited Paper Award in 2009. He was also recognized as one of the top ten authors in the fifty-year history of ISSCC. He received the IEEE Donald Pederson Award in Solid-State Circuits in 2012.

Professor Razavi is an IEEE Distinguished Lecturer, a Fellow of IEEE, and the author of *Principles of Data Conversion System Design*, *RF Microelectronics, First Edition* (translated to Chinese, Japanese, and Korean), *Design of Analog CMOS Integrated Circuits* (translated to Chinese, Japanese, and Korean), *Design of Integrated Circuits for*

Optical Communications, and Fundamentals of Microelectronics (translated to Korean and Portuguese), and the editor of *Monolithic Phase-Locked Loops and Clock Recovery Circuits* and *Phase-Locking in High-Performance Systems*.

INTRODUCTION TO RF AND WIRELESS TECHNOLOGY

Compare two RF transceivers designed for cell phones:

“A 2.7-V GSM RF Transceiver IC” [1] (published in 1997)

“A Single-Chip 10-Band WCDMA/HSDPA 4-Band GSM/EDGE SAW-Less CMOS Receiver with DigRF 3G Interface and +90-dBm IIP₂” [2] (published in 2009)

Why is the latter much more complex than the former? Does the latter have a higher performance or only greater functionality? Which one costs more? Which one consumes a higher power? What do all the acronyms GSM, WCDMA, HSDPA, EDGE, SAW, and IIP₂ mean? Why do we care?

The field of RF communication has grown rapidly over the past two decades, reaching far into our lives and livelihood. Our cell phones serve as an encyclopedia, a shopping terminus, a GPS guide, a weather monitor, and a telephone—all thanks to their wireless communication devices. We can now measure a patient’s brain or heart activity and transmit the results wirelessly, allowing the patient to move around untethered. We use RF devices to track merchandise, pets, cattle, children, and convicts.

1.1 A WIRELESS WORLD

Wireless communication has become almost as ubiquitous as electricity; our refrigerators and ovens may not have a wireless device at this time, but it is envisioned that our homes will eventually incorporate a wireless network that controls every device and appliance. High-speed wireless links will allow seamless connections among our laptops, digital cameras, camcorders, cell phones, printers, TVs, microwave ovens, etc. Today’s WiFi and Bluetooth connections are simple examples of such links.

How did wireless communication take over the world? A confluence of factors has contributed to this explosive growth. The principal reason for the popularity of wireless

communication is the ever-decreasing cost of electronics. Today's cell phones cost about the same as those a decade ago but they offer many more functions and features: many frequency bands and communication modes, WiFi, Bluetooth, GPS, computing, storage, a digital camera, and a user-friendly interface. This affordability finds its roots in *integration*, i.e., how much functionality can be placed on a single chip—or, rather, how few components are left off-chip. The integration, in turn, owes its steady rise to (1) the scaling of VLSI processes, particularly, CMOS technology, and (2) innovations in RF architectures, circuits, and devices.

Along with higher integration levels, the performance of RF circuits has also improved. For example, the power consumption necessary for a given function has decreased and the speed of RF circuits has increased. Figure 1.1 illustrates some of the trends in RF integrated circuits (ICs) and technology for the past two decades. The minimum feature size of CMOS

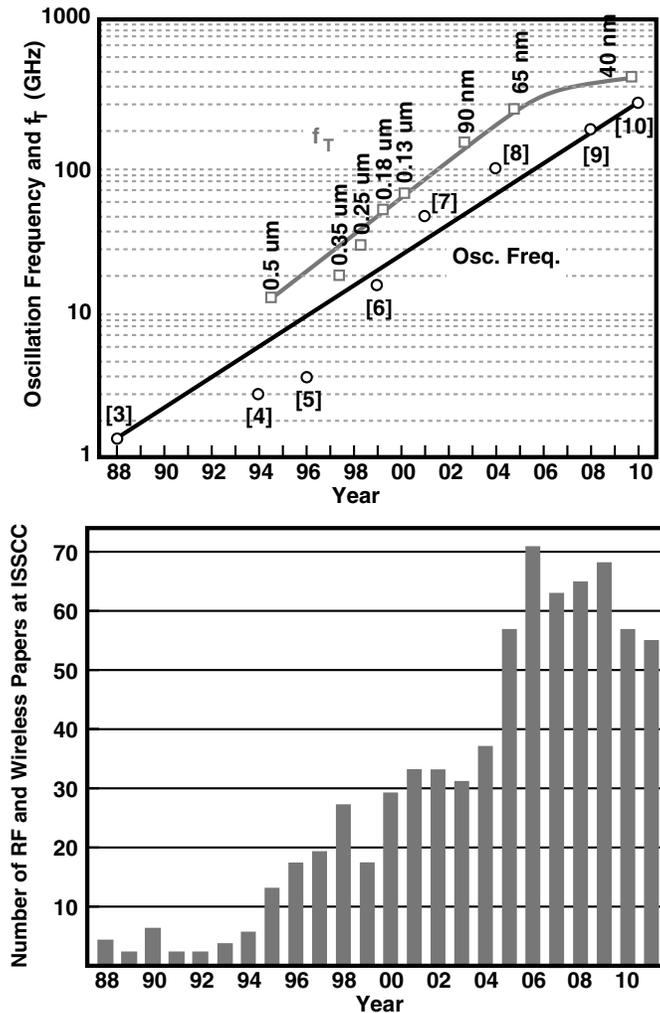


Figure 1.1 Trends in RF circuits and technology.

technology has fallen from 0.5 μm to 40 nm, the transit frequency,¹ f_T , of NMOS devices has risen from about 12 GHz to several hundred gigahertz, and the speed of RF oscillators has gone from 1.2 GHz to 300 GHz. Also shown is the number of RF and wireless design papers presented at the International Solid-State Circuits Conference (ISSCC) each year, revealing the fast-growing activity in this field.

1.2 RF DESIGN IS CHALLENGING

Despite many decades of work on RF and microwave theory and two decades of research on RF ICs, the design and implementation of RF circuits and transceivers remain challenging. This is for three reasons. First, as shown in Fig. 1.2, RF design draws upon a multitude of disciplines, requiring a good understanding of fields that are seemingly irrelevant to integrated circuits. Most of these fields have been under study for more than half a century, presenting a massive body of knowledge to a person entering RF IC design. One objective of this book is to provide the necessary background from these disciplines without overwhelming the reader.

Second, RF circuits and transceivers must deal with numerous trade-offs, summarized in the “RF design hexagon” of Fig. 1.3. For example, to lower the noise of a front-end amplifier, we must consume a greater power or sacrifice linearity. We will encounter these trade-offs throughout this book.

Third, the demand for higher performance, lower cost, and greater functionality continues to present new challenges. The early RF IC design work in the 1990s strove to integrate *one* transceiver—perhaps along with the digital baseband processor—on a single chip. Today’s efforts, on the other hand, aim to accommodate multiple transceivers operating in different frequency bands for different wireless standards (e.g., Bluetooth, WiFi, GPS, etc.). The two papers mentioned at the beginning of this chapter exemplify this trend. It is interesting to note that the silicon chip area of early single-transceiver systems was

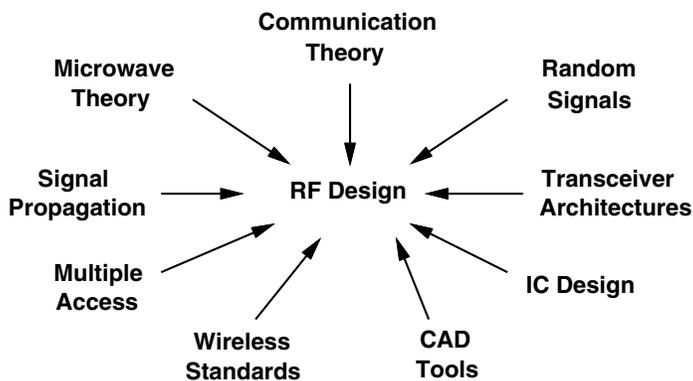


Figure 1.2 Various disciplines necessary in RF design.

1. The transit frequency is defined as the frequency at which the small-signal current gain of a device falls to unity.

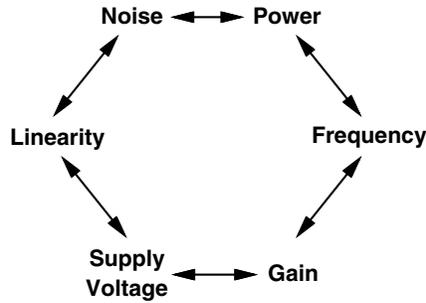


Figure 1.3 RF design hexagon.

dominated by the digital baseband processor, allowing RF and analog designers some latitude in the choice of their circuit and device topologies. In today's designs, however, the multiple transceivers tend to occupy a *larger* area than the baseband processor, requiring that RF and analog sections be designed with much care about their area consumption. For example, while on-chip spiral inductors (which have a large footprint) were utilized in abundance in older systems, they are now used only sparingly.

1.3 THE BIG PICTURE

The objective of an RF transceiver is to transmit and receive information. We envision that the transmitter (TX) somehow processes the voice or data signal and applies the result to the antenna [Fig. 1.4(a)]. Similarly, the receiver (RX) senses the signal picked up by the antenna and processes it so as to reconstruct the original voice or data information. Each black box in Fig. 1.4(a) contains a great many functions, but we can readily make two observations: (1) the TX must drive the antenna with a high power level so that the transmitted signal is strong enough to reach far distances, and (2) the RX may sense a small signal (e.g., when a cell phone is used in the basement of a building) and must first amplify the signal with low noise. We now architect our transceiver as shown in Fig. 1.4(b), where the signal to be transmitted is first applied to a “modulator” or “upconverter” so that its center frequency goes from zero to, say, $f_c = 2.4$ GHz. The result drives the antenna through a “power amplifier” (PA). On the receiver side, the signal is sensed by a “low-noise amplifier” (LNA) and subsequently by a “downconverter” or “demodulator” (also known as a “detector”).

The upconversion and downconversion paths in Fig. 1.4(b) are driven by an oscillator, which itself is controlled by a “frequency synthesizer.” Figure 1.4(c) shows the overall transceiver.² The system looks deceptively simple, but we will need the next 900 pages to cover its RF sections. And perhaps another 900 pages to cover the analog-to-digital and digital-to-analog converters.

2. In some cases, the modulator and the upconverter are one and the same. In some other cases, the modulation is performed in the digital domain before upconversion. Most receivers demodulate and detect the signal digitally, requiring only a downconverter in the analog domain.

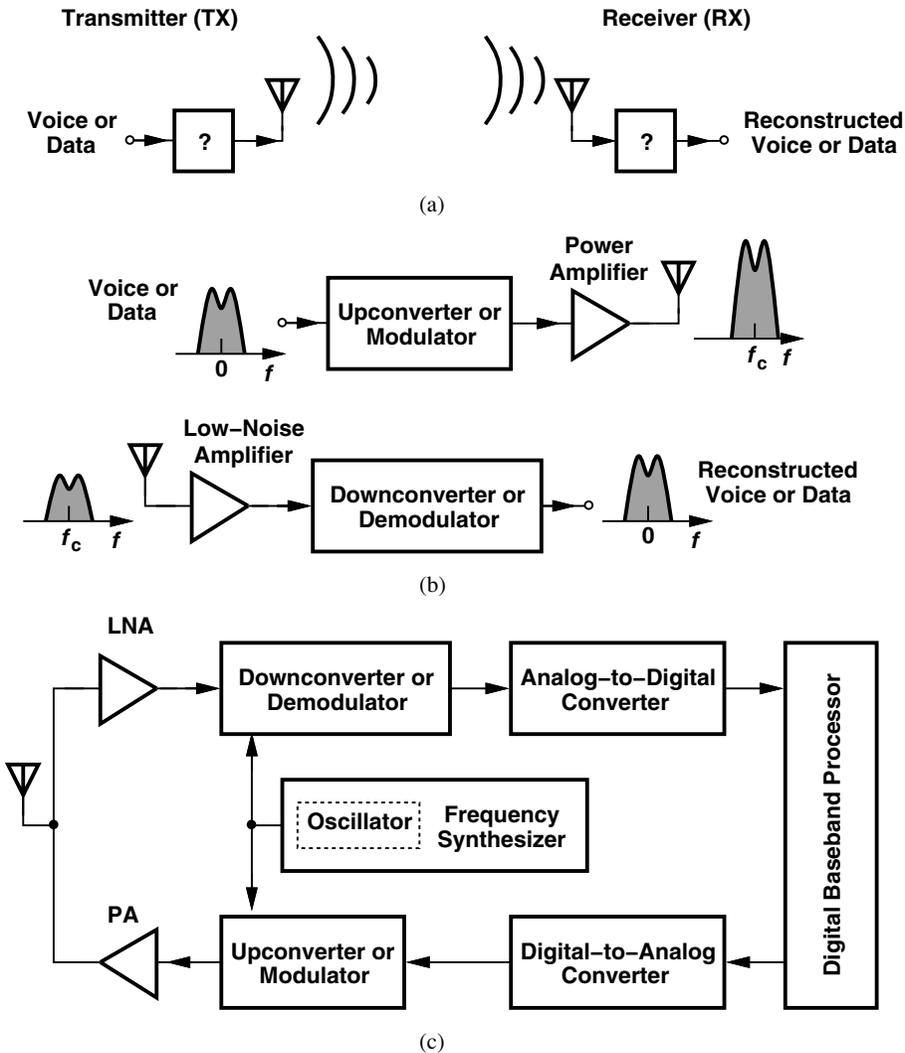


Figure 1.4 (a) Simple view of RF communication, (b) more complete view, (c) generic RF transceiver.

REFERENCES

- [1] T. Yamawaki et al., "A 2.7-V GSM RF Transceiver IC," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2089–2096, Dec. 1997.
- [2] D. Kaczman et al., "A Single-Chip 10-Band WCDMA/HSDPA 4-Band GSM/EDGE SAW-less CMOS Receiver with DigRF 3G Interface and +90-dBm IIP2," *IEEE J. Solid-State Circuits*, vol. 44, pp. 718–739, March 2009.
- [3] M. Banu, "MOS Oscillators with Multi-Decade Tuning Range and Gigahertz Maximum Speed," *IEEE J. Solid-State Circuits*, vol. 23, pp. 474–479, April 1988.
- [4] B. Razavi et al., "A 3-GHz 25-mW CMOS Phase-Locked Loop," *Dig. of Symposium on VLSI Circuits*, pp. 131–132, June 1994.

- [5] M. Soyuer et al., "A 3-V 4-GHz nMOS Voltage-Controlled Oscillator with Integrated Resonator," *IEEE J. Solid-State Circuits*, vol. 31, pp. 2042–2045, Dec. 1996.
- [6] B. Kleveland et al., "Monolithic CMOS Distributed Amplifier and Oscillator," *ISSCC Dig. Tech. Papers*, pp. 70–71, Feb. 1999.
- [7] H. Wang, "A 50-GHz VCO in 0.25- μ m CMOS," *ISSCC Dig. Tech. Papers*, pp. 372–373, Feb. 2001.
- [8] L. Franca-Neto, R. Bishop, and B. Bloechel, "64 GHz and 100 GHz VCOs in 90 nm CMOS Using Optimum Pumping Method," *ISSCC Dig. Tech. Papers*, pp. 444–445, Feb. 2004.
- [9] E. Seok et al., "A 410GHz CMOS Push-Push Oscillator with an On-Chip Patch Antenna" *ISSCC Dig. Tech. Papers*, pp. 472–473, Feb. 2008.
- [10] B. Razavi, "A 300-GHz Fundamental Oscillator in 65-nm CMOS Technology," *Symposium on VLSI Circuits Dig. Of Tech. Papers*, pp. 113–114, June 2010.

INDEX

A

- AC coupling
 - constant capacitors, 490
 - direct-conversion receivers, 183–184, 187
 - mixers, 412–413, 867
 - predrivers, 865, 867
 - transformers, 470
 - VCOs, 526, 573
- Acceptable quality, 59
- Accumulation-mode MOS varactors, 486
- Accuracy
 - DAC, 739
 - I/Q calibration, 232
 - inductor equations, 438–439
 - input matching, 72
 - integer-N frequency synthesizers, 656
 - output matching, 73
- ACPR in power amplifiers, 756–758
- Acquisition range of PLLs, 611, 614
- Active mixers
 - with current-source helpers, 393–394
 - downconversion, 368–369
 - conversion gain, 370–377
 - double-balanced, 369–370
 - linearity, 387–392
 - noise, 377–387
 - with enhanced transconductance, 394–397
 - with high IP_2 , 397–405
 - with low flicker noise, 405–408
 - upconversion, 416–420
 - design procedure, 421–424
 - mixer carrier feedthrough, 420–421
- ADCs (analog-to-digital converters) in receivers
 - AGC range, 836
 - baseband, 858–859
 - direct-conversion, 186
 - resolution, 837
- Additive noise
 - AM, 94
 - conversion to phase noise, 550–552, 554
 - I/Q mismatches, 198
- Adjacent-channel interference
 - GSM, 135
 - IEEE802.11, 149
 - low-IF receivers, 214
 - wideband CDMA, 140, 142–143
- ADS simulator, 439
- AGC in receivers
 - design, 856–861
 - range, 836–837
- Aliasing
 - passive downconversion mixers, 360–361
 - power amplifiers, 798
- Aligned resultants in AM signals, 97
- Alignment of VCO phase, 600–601
- AM (amplitude modulation), 93–94
 - direct-conversion receivers, 189–190
 - heterodyne receivers, 172–173
 - tail noise, 567, 569–570
- AM/AM conversion, 757–758
- AM/PM conversion (APC)
 - concepts, 33–35
 - polar modulation, 794–795, 799–801
 - power amplifiers, 757–758
- Ampere's law, 452
- Amplitude
 - direct-conversion receivers, 196
 - in modulation, 92

- Amplitude (*Contd.*)
 - oscillators, 505–507
 - power amplifiers, 757–758
 - VCO variation, 532
- Amplitude modulation (AM), 93–94
 - direct-conversion receivers, 189–190
 - heterodyne receivers, 172–173
 - tail noise, 567, 569–570
- Amplitude shift keying (ASK), 100, 105
- Analog modulation, 93
 - amplitude, 93–94
 - phase and frequency, 95–99
- Analog-to-digital converters (ADCs) in receivers
 - AGC range, 836
 - baseband, 858–859
 - direct-conversion, 186
 - resolution, 837
- Analysis and Simulation of Spiral Inductors and Transformers (ASITIC) simulator, 437–439
- Analytic signals, 202
- AND gates
 - current-steering circuits, 683
 - dual-modulus dividers, 677, 880
 - phase/frequency detectors, 613–614
- Antennas
 - cellular systems, 122
 - duplexing method, 130
 - LNA interface, 258–259
 - thermal noise, 42, 49–50
- Anti-phase coupling, 582, 584–586, 592
- APC (AM/PM conversion)
 - concepts, 33–35
 - polar modulation, 794–795, 799–801
 - power amplifiers, 757–758
- ASITIC (Analysis and Simulation of Spiral Inductors and Transformers) simulator, 437–439
- ASK (amplitude shift keying), 100, 105
- Asymmetries
 - cascode power amplifiers, 817
 - direct-conversion receivers, 179, 181, 187–189
 - heterodyne receivers, 172–174
 - I/Q mismatches, 194
 - LO self-mixing, 357
 - sequence-asymmetric polyphase filters, 221
 - single-balanced mixers, 398–399
 - transformers, 471, 473–474
- Attenuation
 - channel, 92
 - image, 224–225
- Auxiliary amplifiers in PLLs, 634–635
- Available noise power, 42
- Available power gain, 54
- Average power in noise, 36
- Axis of symmetry, inductors along, 465
- B**
- Balance systems, 12
- Baluns
 - differential LNAs, 315–324
 - outphasing, 810
 - power amplifiers, 758–760, 764, 767
- Band-pass filters
 - differential LNAs, 315
 - FDD, 123–124
 - heterodyne transmitters, 244–245
 - noise spectrum, 37–39, 58
 - Q, 157
 - transceivers, 158–159
 - transmitter overview, 156
- Band selection in transceivers, 157–159
- Band switching LNAs, 262, 312–314
- Bandwidth
 - divide-by-2 circuits, 693–696
 - efficiency, 93
 - fractional, 176
 - frequency synthesizers, 663, 842–843, 883
 - LNAs, 261–263, 304
 - offset PLLs, 672
 - outphasing, 805
 - passive upconversion mixers, 410–411
 - PLL-based modulation, 667–668
 - polar modulation, 794, 801–802
 - power amplifiers, 757, 865
 - QPSK, 107
 - VCO phase noise, 645–646
- Barkhausen's criteria, 503–505, 512, 544, 583
- Baseband
 - ADC resolution, 858–859
 - AGC gain, 859
 - DACs, 409
 - description, 91–92
 - mixers, 337, 409, 414
 - offset, 414
 - outphasing, 804
 - polar modulation, 796–797
 - pulses, 103, 227
 - QPSK signals, 108–109
- Basic design concepts, 7
 - dynamic range, 60–62
 - noise. *See* Noise and noise figure (NF)
 - nonlinear dynamic systems, 75–77
 - nonlinearity. *See* Nonlinearity
 - passive impedance transformation, 62–63
 - matching networks, 65–71
 - quality factor, 63
 - series-to-parallel conversions, 63–65
 - scattering parameters, 71–75
 - sensitivity, 59–60, 131

- time variance, 9–12
- units, 7–9
- Volterra series, 77–85
- Basis functions, 105
- BER. *See* Bit error rate (BER)
- Bias
 - LNA common-gate stage, 280–281
 - LNA nonlinearity calculations, 325–326
 - phase noise current source, 565–570
- Bipolar transistor noise, 46
- Bit error rate (BER)
 - GSM, 132
 - I/Q mismatch, 198
 - power amplifiers, 756
 - receiver noise, 834
 - in sensitivity, 59, 346
 - transmitters, 838
 - wireless standards, 131
- Blind zones with VCOs, 535–536, 846, 869
- Blocking
 - Bluetooth tests, 145–146
 - GSM requirements, 133–134
 - with interferers, 19
 - wideband CDMA, 140–142
- Bluetooth standard
 - frequency channels, 655
 - GFSK for, 113
 - ISM band, 130
 - LOs, 660
 - overview, 143–147
 - receivers, 22–24
- Bode plots
 - charge pumps, 619–620
 - PLLs, 608–609
- Bond wires
 - cascode CS stage, 284–285
 - coupling between, 430–431
 - differential LNAs, 320, 322
 - MOS capacitors, 491
 - outphasing, 810
 - power amplifiers, 755, 758–759, 815
- Bootstrapping, cascode power amplifiers with, 816–817
- Bottom-biased PMOS oscillators, 573
- Bottom-plate capacitance
 - inductors, 440
 - parallel-plate capacitors, 494
 - VCOs, 534, 879
- Brickwall spectrum, 103
- Broadband model of inductors, 457
- Broadband noise, 670–671
- Buffers
 - LOs, 380–381, 413, 499, 576–577
 - PLLs, 602, 607, 668
 - polar modulation, 794, 824
- Bypass, LNA, 312
- C**
- Calibration of image-reject receivers, 213
- Capacitance and capacitors
 - AM/PM conversion, 795, 799
 - constant, 490–495
 - divide-by-2 circuits, 690, 692, 694–696
 - inductors, 437, 439–444, 461–463, 466–469
 - input impedance, 9
 - integer-N synthesizer loop design, 883–885
 - large-signal impedance matching, 780–781
 - LNAs
 - band switching, 312–313
 - common-gate stage, 280–282
 - common-source stage, 269–271, 286–287, 291–293
 - differential, 321
 - gain switching, 308–309
 - input, 851
 - noise-cancelling, 301, 303
 - matching networks, 65–69
 - metal-plate, 493–495
 - Miller dividers, 703
 - mixers
 - downconversion, 352, 376–377, 382–383, 500
 - with enhanced transconductance, 395–397
 - with high IP_2 , 398, 403–404
 - port-to-port feedthrough, 339–340
 - upconversion, 410, 415–416, 422
- MOS, 491–493
- oscillators, 571
 - cross-coupled, 514–515
 - drive capability, 498–499
- outphasing, 808–810
- parallel-plate, 493–495
- phase noise, 555–557
- PLL higher-order loops, 625–626
- power amplifiers, 754
 - cascode, 815–817
 - class B, 765
 - class E, 772–774
 - polar modulation, 792, 795–796
 - positive-feedback, 819–820
 - predrivers, 864
- quality factor, 63
- T-lines, 477
- transformers, 470–475
- varactors, 483–490
- VCOs. *See* Voltage-controlled oscillators (VCOs)

- Capacitive coupling
 - active mixers, 397, 403–404
 - divide-by-2 circuits, 692
 - integer-N synthesizers, 692, 700, 704
 - LNA feedback paths, 304
 - LO interface, 576–577
 - power amplifiers, 865
 - substrate loss, 450–452, 457–458, 466
 - transformers, 470–471, 474–475
 - VCOs, 527, 574, 871–872
- Capacitively-degenerated differential pairs, 591
- Carrier amplifiers, 811
- Carrier feedthrough
 - active mixers, 420–421
 - passive mixers, 413–416
- Carrier frequency, 91
- Carrier leakage
 - direct-conversion transmitters, 232–234
 - heterodyne transmitters, 244
- Carrier power in phase noise, 539
- Cartesian feedback, 786–787
- Cascade image rejection, 225
- Cascaded loops and modulators, 730–732
- Cascaded stages
 - low-IF receivers, 222
 - noise figure, 52–56
 - nonlinear, 29–33
 - transceiver filters, 158
- Cascode stages
 - LNAs, 284–286
 - common-gate, 277–279
 - design procedure, 291–296
 - differential, 318–321
 - gain switching, 310–311
 - noise factor, 287–291
 - pad capacitance, 286–287
 - power amplifiers, 776–779, 815–819
- CCI (co-channel interference), 120
- CCK (complementary code keying), 150
- CDMA (code-division multiple access), 126
 - direct-conversion transmitters, 232–233
 - direct sequence, 126–129
 - IS-95, 137–139
 - wideband, 139–143
- Cellular systems, 119–120
 - antenna diversity, 122
 - co-channel interference, 120
 - delay spread, 122–123
 - hand-offs, 120–121
 - interleaving, 123
 - path loss and multipath fading, 121–122
 - transmitters, 91
- Center frequency in LC VCOs, 571
- CG (common-gate) stage in LNAs, 272–277
 - cascode stage, 277–279
 - design procedure, 279–284
 - gain switching LNAs, 306
 - variants, 296–300
- CG differential LNAs, 315–318
- Chang-Park-Kim dividers, 878, 880
- Channel charge injection, 631
- Channel-length modulation
 - charge pumps, 633–634
 - LNA common-gate stage, 275
- Channel selection
 - vs. image rejection, 166–168
 - transceiver architectures, 157–159
- Channelization standards, 130
- Channels
 - attenuation, 92
 - integer-N synthesizers, 656, 661, 664
 - mixer bandwidth, 500
 - mobile RF communications, 119
 - overlapping frequencies, 150
- Characteristic impedance
 - coplanar lines, 482
 - microstrips, 479–482
 - striplines, 483
- Charge-and-hold output in charge pumps, 616
- Charge equations for varactors, 487
- Charge injection, 630–632
- Charge pumps, 614–615
 - channel-length modulation, 633–634
 - charge injection and clock feedthrough, 630–632
 - CPPLLs, 615–620, 622–625
 - fractional-N synthesizers, 733–738
 - integer-N synthesizers, 883–884
 - regulated cascodes, 634–635
 - VCOs, 522, 525
- Chips, CDMA, 127–128
- Chireix's cancellation technique, 808–809
- Circuit simulators
 - integer-N synthesizers, 884–886
 - power amplifiers, 757
 - varactors, 487
- Circular inductors, 435
- Clapp oscillators, 517
- Class A power amplifiers
 - with harmonic enhancement, 771–772
 - overview, 760–764
- Class-AB latches, 691
- Class AB power amplifiers, 767
- Class B power amplifiers, 764–767
- Class C power amplifiers, 768–770

- Class E power amplifiers, 772–775
- Class F power amplifiers, 775–776
- Clock feedthrough, 630–632
- Close-in phase noise, 539–540
- Closed-loop control
 - IS-95 CDMA, 138
 - polar modulation, 793
- Closed-loop transfer functions
 - integer-N synthesizers, 666
 - PLLs, 607, 619
- CML (current-mode logic), 683–687
- CMOS technology, 2–3
 - LNA common-gate stage, 275
 - oscillator frequency range, 498
 - ring oscillators, 507
- Co-channel interference (CCI), 120
- Code-division multiple access (CDMA), 126
 - direct-conversion transmitters, 232–233
 - direct sequence, 126–129
 - IS-95, 137–139
 - wideband, 139–143
- Cognitive radios, 199
- Coherent detection
 - IS-95 CDMA, 137
 - QPSK, 110
- Collector efficiency in power amplifiers, 755, 761, 766
- Colpitts oscillators, 517
- Common-gate (CG) stage in LNAs, 272–277
 - cascode stage, 277–279
 - design procedure, 279–284
 - gain switching LNAs, 306
 - variants, 296–300
- Common-mode current in mixers, 373–374
- Common-mode input in LOs, 349
- Common-mode noise
 - active downconversion mixers, 383
 - active mixers with low flicker noise, 405
- Common-mode stability in power amplifiers, 866–867
- Common-source stages
 - LNAs
 - with inductive degeneration, 284–296
 - with inductive load, 266–269
 - with resistive feedback, 269–272
 - memoryless systems, 12
- Communication concepts, 91
 - analog modulation, 93–99
 - considerations, 91–93
 - digital modulation. *See* Digital modulation
 - DPSK, 151–152
 - mobile RF, 119–123
 - multiple access techniques, 123–130
 - spectral regrowth, 118–119
 - wireless standards. *See* Wireless standards
- Compact inductor model, 458
- Comparators in power amplifiers, 824
- Compensation in fractional-N synthesizers, 718
- Complementary code keying (CCK), 150
- Compression
 - gain, 16–20
 - LNAs, 851–852
 - in mixer linearity, 388–392
 - power amplifiers, 757–758, 863–864
 - receivers, 856
 - upconverters, 868–869
 - wideband CDMA, 140
- Concentric cylinders model, 457
- Conduction angles, 764, 768–769
- Constant capacitors, 490–495
- Constant-envelope modulation, 112
- Constant-envelope waveforms, 802
- Constellations
 - dense, 114–115
 - signal, 105–112
- Continuous-time (CT) approximation
 - charge pumps, 616
 - type-II PLLs, 622–623
- Continuous tuning, VCOs with, 524–532
- Conversion gain
 - Hartley receivers, 253
 - LO, 349, 501
 - Miller dividers, 701–703
 - mismatches, 226
 - mixers
 - current-source helpers, 393
 - downconversion, 339, 348, 350–356, 368–382
 - linearity, 388–391
 - noise, 357–362, 408, 567
 - power amplifiers, 790
 - upconversion, 409–410, 414, 416, 868
- Conversions
 - additive noise to phase noise, 550–552, 554
 - AM/AM, 757–758
 - AM/PM
 - concepts, 33–35
 - polar modulation, 794–795, 799–801
 - power amplifiers, 757–758
 - current and voltage, 368–369
 - series-to-parallel, 63–65
- Convolution in phase noise, 560–561
- Coplanar lines, 482–483
- Cosine signals in image-reject receivers, 200
- Cost trends, 2
- Counters in pulse swallow dividers, 674–676
- Coupled oscillators, 583–589

- Coupling
 - between bond wires, 430
 - capacitance. *See* Capacitive coupling
 - magnetic. *See* Magnetic coupling
 - quadrature oscillators, 581, 590
 - CPPLLs (charge-pump PLLs), 615–620
 - continuous-time approximation, 622–623
 - frequency-multiplying, 623–625
 - Cross-coupled oscillators, 511–517
 - open-loop model, 545, 547–548
 - phase noise computation, 555
 - power amplifiers, 820
 - tail noise, 565–566
 - time-varying resistance, 553
 - Cross-coupled pairs
 - active mixers with low flicker noise, 406
 - Norton noise equivalent, 548–549
 - VCOs, 530–531
 - Cross modulation
 - description, 20–21
 - wideband CDMA, 140–141
 - Cross-talk, 229
 - Crystal oscillators
 - integer-N synthesizer design, 881
 - phase noise, 644
 - CT (continuous-time) approximation
 - charge pumps, 616
 - type-II PLLs, 622–623
 - Current crowding effect, 448–450
 - Current domain in single-balanced mixers, 356
 - Current-driven passive mixers, 366–368
 - Current impulse
 - oscillators, 509
 - in phase noise, 557–559
 - Current mirroring
 - active mixers, 395–396
 - DACs, 741
 - divide-by-2 circuits, 692
 - VCOs, 874–876
 - Current-mode DAC implementation, 741
 - Current-mode logic (CML), 683–687
 - Current sources
 - helpers, 393–394
 - offset cancellation by, 186
 - power amplifiers, 752
 - Current-steering
 - cross-coupled oscillators, 517
 - divider design, 683–689
 - LO interface, 499, 577
 - mixer linearity, 388
 - prescalers, 682
 - Current-to-voltage (I/V) characteristic of charge pumps, 883–884
 - Current-to-voltage (I/V) conversion, 368–369
 - Currents, nonlinear, 81–85
 - Cyclostationary noise, 552–553, 565
- D**
- D flipflops in phase/frequency detectors, 613
 - DACs (digital-to-analog converters)
 - direct-conversion receivers, 185–187
 - direct-conversion transmitters, 233–234
 - feedforward, 738–742
 - upconversion mixer interfaces, 409
 - Damping factor
 - class E power amplifiers, 773–774
 - divide-by-2 circuits, 693
 - integer-N synthesizers, 665–666, 883
 - PLL transfer functions, 608
 - Dangling bonds, 44
 - Data rates, 130, 136–137
 - dBm, 8–9
 - DC offsets
 - active mixers with high IP_2 , 398–400
 - AGC, 859
 - direct-conversion receivers, 181–187
 - port-to-port feedthrough, 340–341
 - DCOs (digitally-controlled oscillators), 536
 - DCRs. *See* Direct-conversion receivers
 - DCS1800 standard, 132
 - Decibels (dB), 7–9
 - Degenerated differential pairs, 332–333
 - Degenerated LNA common-source stages
 - inductive degeneration, 284–296
 - nonlinearity calculations, 325–329
 - Degeneration capacitors, 403–404, 591
 - Delay spread in cellular systems, 122–123
 - Delayed replicas in IS-95 CDMA, 138
 - Delays
 - divider design, 681, 709–712
 - fractional-N synthesizers, 723–724
 - integer-N synthesizers, 665–667
 - OFDM, 115–117
 - PFD/CP, 629
 - polar modulation, 793–794, 801
 - Delta modulators (DMs), 824–825
 - Demodulation, 92
 - IS-95 CDMA, 137
 - QPSK, 110
 - Demultiplexers in QPSK, 107
 - Dense constellations, 114–115
 - Desensitization, 19
 - Design
 - active upconversion mixers, 421–424
 - basic concepts. *See* Basic design concepts
 - dividers. *See* Dividers
 - LNA cascode CS stage with inductive degeneration, 291–296

- LNA common-gate stage, 279–284
- oscillators, 571–575
- power amplifier. *See* Power amplifiers (PAs)
- transceiver example. *See* Transceivers
- type-II PLLs, 646–647
- Despreading in CDMA, 128
- DET (double-edge-triggered) flipflops, 742–743
- Detectability, 92
- Detection, 92
 - IS-95 CDMA, 137
 - PFDs. *See* Phase/frequency detectors (PFDs)
 - phase detectors, 597–600
 - polar modulation, 794, 799–800, 826
 - power amplifier linearization, 789–790
 - QPSK, 110
- Deterministic mismatches
 - fractional-N synthesizers, 737
 - up and down current, 637
- Device noise
 - bipolar transistors, 46
 - MOS transistors, 43–46
 - resistors, 40–43
- Differential circuits, symmetric inductors in, 460–461, 463–464
- Differential LNAs, 314–315
 - baluns, 317, 321–324
 - common-gate, 315–318
 - common-source, 318–321
- Differential LO phases
 - mixers, 348, 372, 374, 386
 - oscillators, 501
- Differential mixers, 402
- Differential noise, 406, 853
- Differential oscillators, 518, 585, 589
- Differential pairs
 - charge pumps, 632
 - current-steering circuits, 683
 - downconversion mixers, 500
 - input/output characteristics, 12–13
 - LNAs, 331–332
 - oscillators, 507–508, 591
- Differential power amplifiers, 758–760
- Differential PSK (DPSK), 151–152
- Digital modulation
 - GMSK and GFSK, 112–113
 - intersymbol interference, 101–104
 - OFDM, 115–118
 - overview, 99–100
 - QAM, 114–115
 - quadrature, 107–112
 - signal constellations, 105–107
- Digital-to-analog converters (DACs)
 - direct-conversion receivers, 185–187
 - direct-conversion transmitters, 233–234
 - feedforward, 738–742
 - upconversion mixer interfaces, 409
- Digitally-controlled oscillators (DCOs), 536
- Dimensions of inductors, 433–434
- Diode-connected devices
 - active mixers with low flicker noise, 405–406
 - power amplifiers, 816–817
 - VCOs, 525–526
- Direct-conversion mixers, 344
- Direct-conversion receivers, 179
 - DC offsets, 181–187
 - even-order distortion, 187–191
 - flicker noise, 191–194
 - I/Q mismatch, 194–199
 - LO leakage, 179–184
 - mixing spurs, 199
 - noise figure, 346–348
- Direct-conversion transmitters, 227–229
 - carrier leakage, 232–234
 - I/Q mismatch, 229–232
 - mixer linearity, 234–235
 - mixers, 339–342
 - modern, 238–243
 - noise, 238
 - oscillator pulling, 237–238
 - TX linearity, 235–236
- Direct sequence CDMA, 126–129
- Direct sequence SS (DS-SS) communication, 127
- Discrete-time (DT) systems, 622–623
- Discrete tuning in VCOs, 532–536
- Distortion
 - direct-conversion receivers, 187–191
 - duty-cycle, 398
 - harmonic. *See* Harmonics and harmonic distortion
 - intersymbol interference, 101–104
 - outphasing, 808
 - power amplifier linearization, 787–788
- Distributed capacitance
 - dividers, 694
 - inductors, 440
 - LNA common-source stage, 293
 - varactors, 488–489
- Distributed inductor model, 458
- Distributed resistance in varactors, 487–489
- Dithering in fractional-N synthesizers, 728
- Diversity
 - antenna, 122
 - IS-95 CDMA, 138
- Divide-by-1.25 circuits, 746
- Divide-by-1.5 circuits, 743
- Divide-by-2 circuits, 878–880
 - designing, 689–697
 - direct-conversion transmitters, 239–240
 - dual-modulus dividers, 677

- Divide-by-2 circuits (*Contd.*)
 - heterodyne receivers, 175
 - Miller dividers, 706–707
 - pulse swallow dividers, 675–676
 - true single-phase clocking, 697–698
- Divide-by-2/3 circuits
 - dual-modulus dividers, 679
 - pulse swallow dividers, 676–677
- Divide-by-3 circuits
 - dual-modulus dividers, 677–678
 - Miller dividers, 706–707
- Divide-by-3/4 circuit, 680, 881–882
- Divide-by-4 circuits, 177–178
- Divide-by-8/9 circuit, 680
- Divide-by-15/16 circuit, 681–682
- Dividers, 673–674
 - divide-by-2 circuit, 878–880
 - divider delay and phase noise, 709–712
 - dual-modulus, 677–682, 880–881
 - frequency multiplication, 609–611
 - injection-locked, 707–709
 - LO path, 499
 - logic styles, 683
 - current-steering circuits, 683–689
 - divide-by-2 circuits, 689–697
 - true single-phase clocking, 697–699
 - Miller, 699–707
 - PLLs, 611, 672
 - prescaler modulus, 682–683
 - pulse swallow, 673–677
- DMs (delta modulators), 824–825
- Doherty power amplifiers, 811–813, 818–819
- Double-balanced mixers, 348–350
 - active downconverters, 369–370
 - active upconverters, 416
 - capacitive degeneration, 403–404
 - input offset, 399–400
 - Miller dividers, 700
 - noise, 362–363, 381
 - passive downconverters, 351–352
 - passive upconverters, 411, 414
 - polar modulation power amplifiers, 826
 - sampling, 356
 - voltage conversion gain, 377
- Double-edge-triggered (DET) flipflops, 742–743
- Double-quadrature downconversion
 - low-IF receivers, 224–226
 - Weaver architecture, 213
- Double-sideband (DSB) mixers, 867
- Double-sideband (DSB) noise figure, 344, 853
- Double-transformer topology, 822
- Down currents and pulses
 - charge pumps, 614–615, 630–633, 635–637
 - fractional-N synthesizers, 733–734
 - integer-N synthesizers, 883
 - PLL higher-order loops, 625, 627
 - quantization noise, 739
- Down skew in PFD/CP, 627–630
- Downbonds, 285
- Downconversion and downconversion mixers, 339
 - active, 368–369
 - conversion gain, 370–377
 - double-balanced, 369–370
 - linearity, 387–392
 - noise, 377–387
 - design, 851–856
 - heterodyne receivers, 160–164, 168–170
 - image-reject receivers, 206, 210
 - LO ports, 500
 - low-IF receivers, 219–221, 224–226
 - noise figures, 343
 - passive, 350
 - current-driven, 366–368
 - gain, 350–357
 - input impedance, 364–367
 - LO self-mixing, 357
 - noise, 357–364
 - phase noise, 540–541
 - and self-corruption of asymmetric signals, 173–175
 - Weaver architecture, 213
- Downlinks, 119
- DPSK (differential PSK), 151–152
- DR (dynamic range), 60–62
- Drain capacitance in large-signal impedance matching, 780
- Drain current
 - LNA common-gate stage, 280
 - power amplifiers, 768, 771, 773, 776
- Drain efficiency in power amplifiers, 755
- Drive capability of oscillators, 498–499
- DS-CDMA power control, 128–129
- DSB (double-sideband) mixers, 867
- DSB (double-sideband) noise figure, 344, 853
- DT (discrete-time) systems, 622–623
- Dual downconversion, 168–170
- Dual-gate mixers, 374
- Dual-modulus dividers, 677–682, 880
- Dual-modulus prescalers, 674–675
- Dummy switches for charge pumps, 631
- Duplexer filters
 - FDD systems, 124
 - offset PLLs, 671
- Duplexers and duplexing methods
 - antennas, 130
 - time and frequency division duplexing, 123–124
 - transceivers, 158–159
- Duty cycle distortion, 398

- Dynamic dividers, 699–702
 - with inductive load, 702–705
 - moduli with, 705–707
- Dynamic logic in divide-by-2 circuit, 878
- Dynamic nonlinearities, 28
- Dynamic range (DR), 60–62
- Dynamic systems, 14

- E**
- Eddy currents in inductors, 448–449, 452–455, 466
- EDGE (Enhanced Data Rates for GSM Evolution) systems
 - description, 136–137
 - polar modulation, 801–802
- Edge-triggered devices
 - DET flipflops, 742–743
 - phase/frequency detectors, 612–613
- EER (envelope elimination and restoration), 790–793
- Efficiency
 - modulation, 93
 - power amplifiers, 755–756
 - class A, 760–764, 771–772
 - class AB, 767
 - class B, 764–767
 - class C, 768–771
 - class E, 772–775
 - class F, 775–776
- 8-PSK waveforms, 136–137
- Electrostatic discharge (ESD) protection devices, 280
- Embedded spirals
 - high-IP₂ LNAs, 323–324
 - transformers, 471
- Encoding operations in DS-CDMA, 127
- End points in fractional-N synthesizers, 736
- Enhanced Data Rates for GSM Evolution (EDGE)
 - description, 136–137
 - polar modulation, 801–802
- Enhanced transconductance, active mixers with, 394–397
- Envelope-controlled loads, 793
- Envelope detection
 - polar modulation, 794, 799–800, 826
 - power amplifier linearization, 789–790
- Envelope elimination and restoration (EER), 790–793
- Envelopes
 - polar modulation, 793, 795, 825–826
 - power amplifier linearization, 788–790
 - QPSK, 110
- Error cancellation loops, 783
- Error vector magnitude (EVM)
 - description, 106–107
 - receivers, 838
- ESD (electrostatic discharge) protection devices, 280
- Even-order harmonics, 15, 187–191
- EVM (error vector magnitude)
 - description, 106–107
 - receivers, 838
- Excess frequency, 95
- Excess phase in VCOs, 581
- Excessive noise coefficient, 43
- Exclusive-NOR (XNOR) gates, 152
- Exclusive-OR (XOR) gates
 - current-steering circuits, 685–686
 - phase detectors, 598–599
 - PLLs, 603
 - reference doubling, 743
- Expansive characteristic, 17
- Extrapolation, intermodulation, 27

- F**
- Fading, multipath, 121–123
- Far-out phase noise
 - description, 539–540
 - offset PLLs, 672
- Faraday's law
 - inductors, 448
 - magnetic coupling to substrate, 452
- Fast Fourier Transform (FFT), 391
- FDD (frequency-division duplexing), 123–124
- FDMA (frequency-division multiple access), 125
- Feedback
 - direct-conversion transmitters, 232–233
 - dividers. *See* Dividers
 - fractional-N synthesizers, 716, 718–720, 722–723, 725
 - integer-N synthesizers, 661
 - LNAs
 - common-gate, 296–297
 - gain switching, 311
 - noise-cancelling, 300–301
 - resistance, 851
 - offset cancellation by, 185
 - oscillators, 502–508, 513, 582–584
 - polar modulation, 793, 798–800
 - power amplifiers, 759, 783, 786–787
 - VCO phases, 601
- Feedforward
 - common-gate LNAs, 298–300
 - gain switching LNAs, 311
 - power amplifier linearization, 783–786
 - quantization noise, 738–742
- Feedthrough, mixer
 - active upconversion, 420–421
 - passive upconversion, 413–416
 - port-to-port, 339–343

- FFT (Fast Fourier Transform), 391
- FH (frequency hopping) in CDMA, 129–130
- Field simulations for inductors, 439
- Figure of merit (FOM) of VCOs, 570–571
- Filters, 101
 - active mixers with high IP_2 , 402
 - Bluetooth, 143–144
 - differential LNAs, 315
 - direct-conversion receivers, 179, 184
 - duplexer, 124
 - FDD, 123–124
 - fractional-N synthesizers, 716, 738
 - front-end band-pass, 124
 - Gaussian, 112, 143–144
 - heterodyne transmitters, 244–245
 - image-reject, 166, 206
 - integer-N synthesizers, 665
 - LNAs with high- IP_2 , 323–324
 - low-IF receivers, 217–224
 - low-pass, 101
 - Miller dividers, 699–701, 705
 - noise, 37–40, 58
 - PLLs, 603, 606, 625–627, 671
 - polar modulation, 824–826
 - power amplifier linearization, 790
 - Q, 157
 - transceivers, 157–159
 - transmitter overview, 156
 - VCOs, 601, 875–876
- First-order dependence in AM/PM conversion, 34
- First-order $\Sigma\Delta$ modulators, 726
- Flat fading, 123
- Flat phase noise profiles, 644
- Flicker noise, 44–45
 - active mixers
 - with current-source helpers, 394
 - downconversion, 385–387
 - low, 405–408
 - direct-conversion receivers, 191–194
 - low-IF receivers, 215
 - passive downconversion mixers, 366
 - phase, 563–564, 566
 - quadrature oscillators, 591–592
 - receiver design, 853–854
 - VCOs, 642
- Floating resonators in VCOs, 531
- Floating switches in VCOs, 535, 870
- FM (frequency modulation), 95–96
 - frequency synthesizer spurs, 843–844
 - heterodyne receivers, 173
 - narrowband approximation, 96–98
- FNSs. *See* Fractional-N synthesizers (FNSs)
- FOM (figure of merit) in VCOs, 570–571
- Forward channels, 119
- Four-level modulation schemes, 92
- Fourier coefficients
 - cascode output stages, 776
 - power amplifiers, 770
- Fourier series
 - AM/PM conversion, 34, 569
 - flicker noise, 563–564
 - LO waveforms, 368
 - reference doubling, 743–744
 - VCOs, 580
- Fourier transforms
 - fractional-N synthesizers, 716–717
 - mixer gain, 352–353
 - mixer impedance, 364
 - power spectral density, 37
 - quantization noise, 748–749
 - VCO sidebands, 628
 - Volterra series, 77–81
- Fractional bandwidth
 - IF, 176
 - LNA systems, 262
- Fractional dividers, 742–743
- Fractional-N synthesizers (FNSs), 715
 - basic concepts, 715–718
 - basic noise shaping, 722–728
 - charge pump mismatch, 733–738
 - higher-order noise shaping, 728–732
 - modulus randomization, 718–721
 - out-of-band noise, 732–733
 - quantization noise, 738–749
- Fractional spurs, 716
- Free-running VCOs, 655
- Frequencies. *See also* Bandwidth
 - cellular system reuse, 119–120
 - divide-by-2 circuits, 693–694
 - injection-locked dividers, 709
 - integer-N synthesizers, 664, 881
 - LNAs, 259
 - bandwidth, 261–263
 - cascode stage, 294–296
 - common-gate stage, 278–279
 - Miller dividers, 704
 - mixers. *See* Mixers
 - oscillators, 497–498, 503–507, 514, 517
 - phase detectors, 597–598, 612
 - phase noise, 537–538, 566
 - PLLs, 605–606
 - polar modulation, 794
 - system-level considerations, 844–848
 - VCOs, 519–520, 526, 532, 571, 600
 - wireless standards, 130
- Frequency-dependent phase shift, 504, 507
- Frequency-dependent values, 73
- Frequency detectors (FDs) in PLLs, 602

- Frequency deviation, 95
 - Frequency diversity
 - cellular systems, 122
 - IS-95 CDMA, 138
 - Frequency division, multiphase, 745–748
 - Frequency-division duplexing (FDD), 123–124
 - Frequency-division multiple access (FDMA), 125
 - Frequency hopping (FH), 129–130
 - Frequency-locked loops (FLLs), 602
 - Frequency modulation (FM), 95–96
 - frequency synthesizer spurs, 843–844
 - heterodyne receivers, 173
 - narrowband approximation, 96–98
 - Frequency multiplication, 609–611, 623–625
 - Frequency noise, 732
 - Frequency responses
 - LNA systems, 262
 - oscillators, 512
 - VCO phase noise, 645
 - Frequency-selective fading, 123
 - Frequency shift keying (FSK), 100
 - direct-conversion receivers, 184, 197–198
 - noise, 105–106
 - PLLs, 605–606
 - Frequency synthesizers, 498
 - fractional-N. *See* Fractional-N synthesizers (FNSs)
 - integer-N. *See* Integer-N synthesizers
 - system-level considerations, 840–844
 - Friis' equation
 - LNAs, 264
 - noise, 54–55, 57–58
 - Fringe capacitance in inductors, 439–440, 461, 463
 - Fringe capacitors
 - parallel-plate capacitors, 495
 - VCOs, 529–530
 - Front-end band-pass filters, 124
 - Front-end band-select filters, 158
 - FSK (frequency shift keying), 100
 - direct-conversion receivers, 184, 197–198
 - noise, 105–106
 - PLLs, 605–606
 - Full-duplex LNA systems, 260–261
 - Full scale in dynamic range, 60
 - Fully-integrated power amplifiers, 770
 - Fundamentals in harmonic distortion, 15, 34
- G**
- Gain
 - AGC
 - design, 856–861
 - range, 836–837
 - conversion. *See* Conversion gain
 - current-steering circuits, 686
 - LNAs, 257–258, 304, 850–852
 - Miller dividers, 703
 - oscillators, 504–507
 - PLLs, 597, 601–602, 604
 - power amplifiers, 790, 863
 - transmitter, 838–839
 - VCOs, 518, 601–602, 604
 - Gain compression, 16–20, 388–392
 - Gain error in DACs, 741
 - Gain mismatch
 - direct-conversion receivers, 196
 - direct-conversion transmitters, 231–232, 241
 - image-reject receivers, 209
 - Gain switching
 - LNAs, 305–312
 - receivers, 837
 - Gap capacitance, 466–467
 - Gate capacitance
 - divide-by-2 circuits, 692
 - power amplifiers, 815
 - Gate-induced noise current, 43–44
 - Gate-referred noise voltage, 256
 - Gate switching in PLLs, 636
 - Gaussian distribution, 122
 - Gaussian filters
 - Bluetooth, 143–144
 - impulse response, 112
 - Gaussian frequency shift keying (GFSK)
 - Bluetooth, 143
 - description, 112–113
 - direct-conversion transmitters, 234–235
 - Gaussian minimum shift keying (GMSK)
 - Bluetooth, 143
 - description, 112–113
 - direct-conversion transmitters, 234–235
 - Generic transmitter upconversion requirements, 408
 - Gilbert cell in upconversion mixers, 418
 - Global System for Mobile Communication (GSM)
 - adjacent-channel interference, 135
 - blocking requirements, 133–134
 - description, 132–133
 - EDGE, 136–137
 - intermodulation requirements, 134–135
 - transmitters, 135–136, 670
 - G_m oscillators, 516–517
 - GMSK (Gaussian minimum shift keying)
 - Bluetooth, 143
 - description, 112–113
 - direct-conversion transmitters, 234–235
 - Ground inductances in LNAs, 260, 281
 - Grounded shield inductors, 435, 466–467
 - GSM. *See* Global System for Mobile Communication (GSM)
 - GSM/EDGE mask margins, 801

H

Hand-offs
 cellular systems, 120–121
 IS-95 CDMA, 139

Handheld units, 119

Hard transistors, 776

Harmonics and harmonic distortion, 14–16
 AM/PM conversion, 34
 class A power amplifiers, 771–772
 class E power amplifiers, 775
 class F power amplifiers, 775–776
 direct-conversion transmitters, 241
 heterodyne transmitters, 244–246
 narrowband systems, 25
 phase noise, 564–565

Hartley architecture
 calibration, 213
 image-reject receivers, 205–210
 low-IF receivers, 215–216

Heterodyne receivers, 160–161
 dual downconversion, 168–170
 high-side and low-side injection, 164–166
 image problem, 161–164
 image rejection, 166–168
 mixers, 342
 sliding-IF, 174–178
 zero second IFs, 171–174

Heterodyne transmitters, 244
 carrier leakage, 244
 mixing spurs, 245–248

HFSS simulator for inductors, 439

High currents in power amplifiers, 754–755

High-efficiency power amplifiers, 770
 class A, 771–772
 class E, 772–775
 class F, 775–776

High IP_2 , mixers with, 397–405

High- IP_2 LNAs, 313–314
 differential, 314–315
 baluns, 317, 321–324
 common-gate, 315–318
 common-source, 318–321
 improvement methods, 323–324

High-pass filters (HPFs)
 direct-conversion receivers, 184
 image-reject receivers, 203, 206
 LNAs with high- IP_2 , 323–324
 mixers with high IP_2 , 402

High-side injection, 164–166

Higher harmonics in phase noise, 564–565

Higher-order noise shaping, 728–732

Higher-order PLL loops, 625–627

Hilbert transform
 image-reject receivers, 201, 203–206
 low-IF receivers, 215–217

Hold-mode noise, 359–362

Homodyne architecture, 179

HPFs. *See* High-pass filters (HPFs)

HSPICE simulator for varactors, 487

I

I/Q mismatches
 frequency planning, 848
 receivers, 194–199, 837–838
 transmitters, 229–232, 241, 244, 839–840

I/V (current-to-voltage) characteristic of charge pumps, 883–884

I/V (current-to-voltage) conversion, 368–369

IEEE802.11a/b/g standard, 147–151

IF (intermediate frequency)
 heterodyne receivers, 160–162, 168–169
 low-IF receivers, 214–217
 zero second, 171–178

IF ports, 337

IIP3 (input third intercept points), 26

ILDs (injection-locked dividers), 707–709

IM. *See* Intermodulation (IM)

Image issues
 heterodyne receivers, 161–164, 166–168
 low-IF receivers, 224–225

Image-reject receivers (IRRs), 200, 838
 90° phase shift, 200–205
 calibration, 213
 Hartley architecture, 205–210
 low-IF, 215–217
 Weaver receivers, 210–213

Image-to-signal ratio, 208

Impedance, 9
 charge pumps, 634–635
 coplanar lines, 482
 current sources, 634–635
 divide-by-2 circuits, 692–693
 downconversion mixers, 500
 large signals, 780–781
 LNAs, 258–260, 263
 common-gate, 276, 296–298
 common-source, 267, 284–285
 gain switching, 307, 309
 matching networks, 69
 microstrips, 479–482
 mixers, 357, 364–367, 856
 and noise, 48, 52, 54–56
 oscillators, 503, 510
 PLLs, 634, 668
 power amplifiers, 780–782, 809, 812–813, 821
 T-lines, 478

Impedance transformation
 passive, 62–63

- matching networks, 65–71
 - quality factor, 63
 - series-to-parallel conversions, 63–65
 - power amplifiers, 753
 - Impulse sensitivity function in phase noise, 559, 563
 - IMT-2000 air interface, 139–143
 - In-band blockers in GSM, 133
 - In-band interferers, 158
 - In-band loss, 158
 - In-band noise in fractional-N synthesizers, 728
 - In-channel IP₃, 835
 - In-loop PLL modulation, 667–669
 - In-phase coupling, 582, 585, 588, 592
 - Incident waves, 71–73
 - Inductance and inductors
 - basic structure, 431–434
 - capacitive coupling to substrate, 450–452, 457–458
 - cross-coupled oscillators, 514
 - divide-by-2 circuits, 692–696
 - equations, 436–439
 - geometries, 435
 - with ground shields, 466–467
 - LNAs
 - common-gate, 281
 - common-source, 266–269, 291, 294
 - differential, 320–322
 - noise-cancelling, 301, 305
 - parasitic, 260
 - loss mechanisms, 444–455
 - magnetic coupling to substrate, 452–455, 457–458
 - metal resistance, 444–448
 - Miller dividers, 702–705
 - mixers
 - active upconversion, 416, 422
 - enhanced transconductance, 396–397
 - passive upconversion, 412–413
 - modeling, 455–460
 - off-chip, 430–431
 - one-port oscillators, 511
 - outphasing, 808–810
 - parasitic capacitances, 439
 - power amplifiers, 752–755, 765–767, 815, 817
 - skin effect, 448–450
 - stacked, 467–470
 - symmetric, 460–466
 - T-lines, 477
 - VCOs, 520–521, 523, 571
- Inductive degeneration in LNAs, 284–296, 310
 - Industrial-scientific-medical (ISM) band, 130
 - Infradyne system, 164
 - Injected noise, 562–563
 - Injection-locked dividers (ILDs), 707–709
 - Injection-locked power amplifiers, 820–821
 - Injection locking in quadrature oscillators, 592–593
 - Injection pulling between oscillators, 237, 589
 - Input capacitance
 - cross-coupled oscillators, 514
 - LNAs, 301, 303, 851
 - power amplifiers, 754, 819, 864
 - Input impedance, 9
 - LNAs, 258–260, 263
 - common-gate, 276, 296–298
 - common-source, 267, 284–285
 - gain switching, 307, 309
 - mixers, 364–367, 856
 - one-port oscillators, 510
 - PLL-based modulation, 668
 - Input level range in wireless standards, 131
 - Input matching
 - LNAs, 263–266
 - common-gate, 299
 - common-stage, 287, 292–294
 - gain switching, 307, 310
 - noise-cancelling, 304
 - power amplifiers, 814
 - Input/output characteristics of Doherty power amplifiers, 811
 - Input-referred noise
 - active downconversion mixers, 381–384, 390
 - LNAs, 256–257
 - modeling, 46–48, 50
 - sampling mixers, 359, 362–363
 - Input reflection coefficient, 74
 - Input resistance in LNAs, 308, 851
 - Input return loss in LNAs, 258–259
 - Input third intercept points (IIP₃), 26
 - Instantaneous frequency, 95
 - Integer-N synthesizers, 655, 869
 - basic, 659–661
 - considerations, 655–659
 - dividers. *See* Dividers
 - loop design, 882–886
 - PLL-based modulation, 667–673
 - settling behavior, 661–664
 - spur reduction techniques, 664–667
 - VCO design, 869–877
 - Integration trends, 2
 - Integrators
 - DAC, 739–740
 - fractional-N synthesizers, 723–724, 728
 - VCOs, 581
 - Inter-spiral capacitance in inductors, 468–469
 - Interference
 - adjacent-channel, 135
 - co-channel, 120
 - intersymbol, 101–104, 115–116

- Interferers
 - with compression, 18–19
 - with cross modulation, 20–21
 - direct-conversion receivers, 187
 - high-IP₂ LNAs, 324
 - integer-N frequency synthesizers, 657
 - with intermodulation, 21–23
 - mixers, 341
 - transceivers, 156–158
- Interleaving in cellular systems, 123
- Intermediate frequency (IF)
 - heterodyne receivers, 160–162, 168–169
 - low-IF receivers, 214–217
 - zero second, 171–178
- Intermodulation (IM)
 - in cascades, 30–33
 - GSM requirements, 134–135
 - integer-N frequency synthesizers, 658
 - overview, 21–25
 - power amplifiers, 757
 - between receiver blockers, 835
- Intermodulation tests
 - Bluetooth, 146
 - wideband CDMA, 142
 - wireless standards, 131–132
- Intersymbol interference (ISI), 101–104, 115–116
- Interwinding capacitance in inductors, 440–442, 461–463
- Inverse Laplace transform, 621
- Inverter delay, 614, 629
- IP₂ (second intercept points), 188
- IP₃ (third intercept points), 25–27
- IRR (image rejection ratio), 208–209, 212
- IRRs. *See* Image-reject receivers (IRRs)
- IS-95 CDMA, 137–139
- ISI (intersymbol interference), 101–104, 115–116
- ISM (industrial-scientific-medical) band, 130
- Isolation
 - LNAs, 260
 - outphasing, 809
 - reverse, 72
- J**
- Jitter in divider design, 711
- L**
- L-section topologies, 67–68
- Laplace transform
 - charge pumps, 615–617
 - PLL transient response, 621
- Large-signal impedance matching, 780–782
- Latches
 - current-steering circuits, 686–689
 - divide-by-2 circuits, 878–879
 - Latchup in mixers, 406–407
- Lateral-field capacitors, 529
- Lateral substrate currents, 452
- Layout parasitics in divide-by-2 circuit, 879
- LC oscillators
 - cross-coupled, 511–517
 - LO swings, 366
 - open-loop Q, 545–546
 - phase noise, 501
 - tuning ranges, 438, 498
 - VCOs, 519, 571–575
- Leakage
 - direct-conversion receivers, 179–184
 - direct-conversion transmitters, 232–234
 - heterodyne transmitters, 244
 - LNA systems, 261
 - mixers, 341–342, 357
 - polar modulation, 802
- Least mean square (LMS) algorithm, 234
- Leeson's Equation, 547
- Lenz's law, 452
- L'Hopital's rule, 769
- Limit cycles in fractional-N synthesizers, 728
- Limiting stage in polar modulation, 794–795
- Line-to-line inductor spacing, 463
- Linear amplification with nonlinear components (LINC), 802–803
- Linear drain capacitance, 780
- Linear model of oscillators, 548–549
- Linear power amplifiers, 110
- Linear systems, 9
- Linearity and linearization
 - LNAs, 260–261
 - mixers, 338–339, 387–392
 - nonlinearity. *See* Nonlinearity
 - power amplifiers, 756–758, 782–783
 - Cartesian feedback, 786–787
 - Class A, 761–762
 - envelope detector, 794
 - envelope feedback, 788–790
 - feedforward, 783–786
 - predistortion, 787–788
- LMS (least mean square) algorithm, 234
- LNAs. *See* Low-noise amplifiers (LNAs)
- LO. *See* Local oscillator (LO)
- Load capacitance
 - divide-by-2 circuits, 696
 - oscillators, 498, 571
- Load design for class E power amplifiers, 772
- Load inductors in divide-by-2 circuits, 696
- Load-pull tests, 781–782
- Load switching in LNAs, 311
- Local envelope feedback, 793
- Local oscillator (LO)

- Cartesian feedback, 787
- coupling in power amplifiers, 760
- direct-conversion receivers, 179–184
- direct-conversion transmitters, 237–240
- drive capability, 499
- frequency synthesizers, 656–657, 660, 840
- heterodyne receivers, 160–164, 170–172, 176–177
- heterodyne transmitters, 244–246
- ideal waveforms, 349–350
- interface, 575–577
- leakage, 179–184, 341–342, 357
- LO-IF feedthrough, 340
- mixers
 - buffers, 413
 - downconversion, 368, 374–387
 - with high IP_2 , 398
 - with low flicker noise, 407–408
 - single-balanced and double-balanced, 348–350
 - upconversion, 413–416
- off-chip inductors, 430–431
- offset PLLs, 673
- on-off keying transceivers, 248–249
- outphasing mismatches, 805
- output waveforms, 501
- phase noise, 540–542
- polar modulation, 798
- ports
 - Miller dividers, 700, 703
 - mixers, 337–338, 500
- pulling, 846
- self-mixing, 181, 357
- swings, 366
- VCO phases, 746
- Lock range in injection-locked dividers, 707–709
- Lock time in integer-N synthesizers, 658–659, 885–886
- Logic styles in divider design
 - current-steering circuits, 683–689
 - divide-by-2 circuits, 689–697
 - true single-phase clocking, 697–699
- Loops
 - integer-N synthesizers, 663, 881–886
 - oscillator gain, 504–507
 - phase-locked. *See* Phase-locked loops (PLLs)
 - VCO phase gain, 601–602, 604
 - VCO phase noise, 645–646
- Losses
 - inductors, 444–455
 - matching networks, 69–71
 - microstrips, 480–482
- Lossy circuits, noise in, 42, 56–58
- Lossy oscillatory systems, Q in, 459
- Lossy tanks in one-port oscillators, 509–510
- Low-frequency beat in active mixers, 402–403
- Low-frequency components in phase noise, 569
- Low-IF receivers, 214–217
 - double-quadrature downconversion, 224–226
 - polyphase filters, 217–224
- Low-noise amplifiers (LNAs), 255
 - band switching, 262, 312–314
 - bandwidth, 261–263, 304
 - common-gate stage. *See* Common-gate (CG) stage in LNAs
 - common-source stage
 - with inductive degeneration, 284–296
 - with inductive load, 266–269
 - with resistive feedback, 269–272
 - design, 849–852
 - gain, 257–258, 850–852
 - gain switching, 305–312
 - heterodyne receivers, 166, 169, 174–175
 - high- IP_2 . *See* High- IP_2 LNAs
 - input matching, 263–266
 - input return loss, 258–259
 - linearity, 260–261
 - mixer design, 853, 856
 - noise-cancelling, 300–303
 - noise computations, 49–51
 - noise figure, 255–257
 - nonlinearity calculations, 325
 - degenerated common-source stage, 325–329
 - degenerated differential pairs, 332–333
 - differential and quasi-differential pairs, 331–332
 - undegenerated common-source stage, 329–330
 - power dissipation, 263
 - reactance-cancelling, 303–305
 - stability, 259–260
- Low-noise VCOs, 573–575
- Low-pass filters, 101
 - direct-conversion receivers, 179
 - fractional-N synthesizers, 716
 - image-reject receivers, 203, 206
 - Miller dividers, 699–701, 705
 - noise, 40
 - PLLs, 603, 606
 - polar modulation, 824–826
 - power amplifier linearization, 790
 - VCOs phase, 601, 875–876
- Low-pass signals in direct-conversion receivers, 189–190
- Low-side injection
 - heterodyne receivers, 164–166
 - image-reject receivers, 211–212
- Lumped capacitance
 - inductors, 441, 462, 468–469
 - interwinding, 462
 - substrate, 453
 - transformers, 472

- Lumped model
 - inductors, 439, 455, 458
 - MOS capacitors, 491
 - MOS varactors, 487–489
 - MOSFETs, 44
- Lumped resistance of varactors, 487–488
- M**
- Magnetic coupling
 - along axis of symmetry, 465
 - and coupling capacitance, 475
 - eddy currents, 466
 - plots, 433–434
 - to substrate, 452–455, 457–459
 - transformers, 470–472, 474
- Make-before-break operations, 139
- MASH architecture, 732
- Matching networks, 62–63. *See also* Mismatches
 - losses, 69–71
 - passive impedance transformation, 65–69, 752–753
 - power amplifiers, 752–753, 814
 - high currents, 755
 - large-signal, 780–782
 - power combining, 821
- Mathematical model for VCOs, 577–581
- MATLAB for power amplifiers, 757
- Memoryless systems, 12
- Metal losses in inductor modeling, 455
- Metal-plate capacitors, 493–495
- Metal resistance in inductor Q, 444–448
- Metastability in divider design, 711
- Microstrips, 479–482
- Microwave theory, 71
- Miller dividers, 699–702
 - with inductive load, 702–705
 - moduli with, 705–707
- Miller multiplication, 291–292
- Mirror symmetry in inductors, 464
- Mismatches
 - active mixers with high IP_2 , 400
 - antenna/LNA interface, 258–259
 - fractional-N synthesizers, 733–738
- I/Q
 - frequency planning, 848
 - receivers, 194–199, 837–838
 - transmitters, 229–232, 241, 244, 839–840
- image-reject receivers, 209
- integer-N synthesizers, 883
- LNAs, 263–266
- multiphase frequency division, 746–747
- outphasing, 805
- passive upconversion mixers, 414
- PFD/CP, 627–630
- PLL higher-order loops, 625
- polar modulation, 793–794
- quadrature oscillators, 588–590
- receivers, 837–838
- up and down current, 632–633, 637, 733–734
- Mixers, 11, 337
 - active. *See* Active mixers
 - considerations, 337–338
 - design, 851–856
 - direct-conversion receivers, 187–189
 - direct-conversion transmitters, 234–235, 240–243
 - double-balanced. *See* Double-balanced mixers
 - downconversion. *See* Downconversion and downconversion mixers
 - as envelope detector, 789–790
 - gain. *See* Conversion gain
 - harmonic distortion, 15–16
 - heterodyne receivers, 160–164, 168–170
 - high- IP_2 LNAs, 324
 - injection-locked dividers, 708
 - and LNA noise, 257
 - Miller dividers, 699–704, 706
 - noise and linearity, 338–339
 - noise figures, 343–348
 - oscillators. *See* Local oscillator (LO)
 - passive. *See* Passive mixers
 - performance parameters, 338–343
 - phase noise, 566
 - PLLs, 672–673
 - polar modulation, 826
 - port-to-port feedthrough, 339–343
 - single-balanced. *See* Single-balanced mixers
 - upconversion. *See* Upconversion and upconversion mixers
- Mixing spurs, 338
 - direct-conversion receivers, 179, 199
 - heterodyne receivers, 170–171
 - heterodyne transmitters, 245–248
- Mobile RF communications, 119
 - antenna diversity, 122
 - cellular systems, 119–120
 - co-channel interference, 120
 - delay spread, 122–123
 - hand-offs, 120–121
 - interleaving, 123
 - path loss and multipath fading, 121–122
- Mobile stations, 131
- Mobile telephone switching offices (MTSOs), 120–121
- Modeling
 - inductors, 455–460
 - transformers, 475–476
- Modems, 92

- Modulation, 92–93
 - AM. *See* Amplitude modulation (AM)
 - analog, 93–99
 - channel-length, 275, 633–634
 - cross, 20–21, 140–141
 - digital. *See* Digital modulation
 - direct-conversion receivers, 184
 - FM, 95–96
 - frequency synthesizer spurs, 843–844
 - heterodyne receivers, 173
 - narrowband approximation, 96–98
 - image-reject receivers, 200
 - intermodulation, 21–29
 - phase, 95–99
 - PLL-based, 667–673
 - polar. *See* Polar modulation power amplifiers
 - wireless standards, 130
 - Modulation index, 93
 - Modulus
 - dividers, 673–676, 705–707
 - dual-modulus, 677–682, 880–881
 - multi-modulus, 732
 - prescaler, 682–683
 - fractional-N synthesizers, 718–721
 - frequency multiplication, 610–611
 - MOS capacitors, 491–493
 - MOS switches, 600
 - MOS transistors, 43–46
 - MOS varactors, 485–490, 519–520
 - MTSOs (mobile telephone switching offices), 120–121
 - Multi-carrier spectrum in OFDM, 117
 - Multi-modulus dividers, 732
 - Multipath fading, 121–123
 - Multipath propagation, 115–116
 - Multiphase frequency division, 745–748
 - Multiple access techniques
 - CDMA, 126–130
 - FDMA, 125
 - TDMA, 125–126
 - time and frequency division duplexing, 123–124
 - Multiplexers (MUX)
 - fractional dividers, 742
 - frequency planning, 846–847
 - multiphase frequency division, 745–746
 - VCOs, 877
 - Mutual injection pulling between oscillators, 589
- N**
- NAND gates
 - current-steering circuits, 683–684
 - divide-by-2 circuits, 676
 - divide-by-2/3 circuits, 680
 - phase/frequency detectors, 614
 - single-phase clocking, 698
 - Narrowband FM approximation, 96–98
 - Narrowband noise, 551
 - Natural frequency
 - divide-by-2 circuits, 693
 - oscillator mismatches, 588
 - PLLs, 608
 - Near/far effect in CDMA, 129
 - Negative feedback systems
 - noise-cancelling LNAs, 303
 - oscillators, 502–503
 - power amplifier linearization, 783
 - VCO phase in PLLs, 601
 - Negative-Gm oscillators, 516
 - Negative resistance
 - cross-coupled oscillators, 516
 - LNA systems, 268
 - one-port oscillators, 509–510
 - Nested feedforward architecture, 785
 - 90° phase shift
 - image-reject receivers, 200–205
 - low-IF receivers, 215–216
 - NMOS devices
 - transconductance, 282
 - transit frequency, 3
 - VCO cross-coupled pairs, 530
 - Noise and noise figure (NF), 35–36
 - AGC, 859
 - bipolar transistors, 46
 - cascaded stages, 52–56
 - CDMA, 127
 - direct-conversion receivers, 190–191, 346
 - direct-conversion transmitters, 238
 - flicker. *See* Flicker noise
 - fractional-N synthesizers. *See* Fractional-N synthesizers (FNSs)
 - frequency planning, 846
 - frequency synthesizers, 840–843
 - FSK signals, 105–106
 - IEEE802.11, 149
 - input-referred, 46–48
 - LNAs. *See* Low-noise amplifiers (LNAs)
 - lossy circuits, 56–58
 - mixers
 - with current-source helpers, 393–394
 - in design, 853–854
 - with high IP₂, 399, 402
 - linearity, 387–392
 - noise figures, 343–348
 - overview, 338–339
 - qualitative analysis, 377–381
 - quantitative analysis, 381–387
 - RZ, 357–359

- Noise and noise figure (NF) (*Contd.*)
 - sampling, 359–364
 - upconversion vs. downconversion, 409
 - modulus randomization, 718–721
 - MOS transistors, 43–46
 - offset PLLs, 670–671
 - oscillators, 501, 503, 546–548
 - overview, 48–52
 - phase. *See* Phase noise
 - polar modulation, 802
 - PSK signals, 105
 - quadrature oscillators, 591–592
 - quantization. *See* Quantization noise
 - as random process, 36–37
 - receivers, 92, 834
 - direct-conversion, 191–194
 - heterodyne, 169
 - low-IF, 215
 - representation in circuits, 46–58
 - resistors, 40–43
 - and sensitivity, 59–60
 - spectrum, 37–39
 - transfer function, 39–40
 - VCOs, 532, 871–875
 - Noise-cancelling LNAs, 300–303
 - Noise floor, 59
 - Non-delaying integrators, 728
 - Non-return-to-zero (NRZ) mixers, 352
 - Nonlinear power amplifiers, 93
 - Nonlinear systems, 10, 75–77
 - Nonlinearity
 - AM/PM conversion, 33–35
 - cascaded stages, 29–33
 - cross modulation, 20–21
 - drain capacitance in impedance matching, 780
 - gain compression, 16–20
 - harmonic distortion, 14–16
 - intermodulation, 21–29
 - LNAs, 312, 325
 - degenerated common-source stage, 325–329
 - degenerated differential pairs, 332–333
 - differential and quasi-differential pairs, 331–332
 - undegenerated common-source stage, 329–330
 - noise relationship to, 387–388
 - overview, 12–14
 - PFD/CP, 735–736
 - receivers, 834–835
 - Volterra series currents, 81–85
 - Nonmonotonic error, 736
 - NOR gates
 - current-steering circuits, 683–684, 689
 - dual-modulus dividers, 677–679
 - synthesizer design, 883
 - Norton noise equivalent, 40, 548–549
 - NRZ (non-return-to-zero) mixers, 352
 - Number of turns factor
 - metal resistance inductors, 445–446
 - spiral inductors, 432–434, 436–437, 441–442
 - transformers, 471, 473
- O**
- Octagonal inductors, 435
 - Odd symmetry, 12, 15
 - OFDM. *See* Orthogonal frequency division multiplexing (OFDM)
 - OFDM channelization in IEEE802.11, 147–148
 - Off-chip devices
 - baluns, 323, 767, 810
 - image-reject filters, 166
 - inductors, 429–431
 - Offset frequency
 - mixers, 853–855
 - VCOs, 871, 874–876
 - Offset PLLs, 670–673
 - Offset QPSK (OQPSK), 110
 - Offsets
 - active mixers with high IP_2 , 398–400
 - AGC, 859
 - direct-conversion receivers, 181–187
 - passive upconversion mixers, 414–415
 - port-to-port feedthrough, 340–341
 - On-chip devices
 - ac coupling, 183
 - baluns, 323, 767
 - high-pass filters, 214
 - inductors, 179, 320–322, 694, 770
 - low-pass filters, 179
 - passive. *See* Passive devices
 - transformers, 299–300, 821, 826
 - transmission lines, 829
 - On-off keying (OOK), 100, 248–249
 - 1–1 cascades, 731
 - 1-dB compression point, 17–18
 - 1/f noise, 44–46
 - One-port view of oscillators, 508–511, 584
 - One-sided spectra, 38
 - OOK (on-off keying), 100, 248–249
 - Open-loop control
 - IS-95 CDMA, 138
 - polar modulation, 793
 - Open-loop model of cross-coupled oscillators, 545, 547–548
 - Open-loop modulation, 667
 - Open-loop Q, 459, 544–545
 - Opposite signs in sidebands, 97–98
 - OQPSK (offset QPSK), 110
 - OR gates
 - current-steering circuits, 684, 689

- divide-by-2/3 circuits, 679
 - divide-by-15/16 circuits, 681
 - dual-modulus divider, 880
- Orthogonal frequency division multiplexing (OFDM)
 - average power, 235
 - for delay spread, 147–148
 - flicker noise, 854
 - I/Q mismatch, 198
 - overview, 115–118
 - in transceiver design, 835, 837–838, 854
- Orthogonal messages, 126
- Orthogonal phasors, 585
- Oscillators, 497
 - cross-coupled. *See* Cross-coupled oscillators
 - design procedure, 571–575
 - drive capability, 498–499
 - feedback view, 502–508
 - frequency range, 497–498
 - integer-N synthesizer design, 881
 - linear model, 548–549
 - LO. *See* Local oscillator (LO)
 - one-port view, 508–511, 584
 - output voltage swing, 498
 - performance parameters, 497–501
 - phase/frequency detectors, 613
 - phase noise. *See* Phase noise
 - pulling in direct-conversion transmitters, 237–238
 - Q in, 459, 545–570
 - quadrature. *See* Quadrature oscillators
 - three-point, 517–518
 - tuning ranges, 438, 498
 - VCOs. *See* Voltage-controlled oscillators (VCOs)
- Out-of-band blocking
 - Bluetooth, 146
 - GSM, 133
 - transceivers, 157–158
 - wideband CDMA, 140
- Out-of-band noise, 732–733
- Out-of-channel IP₃, 835
- Outphasing power amplifiers
 - basics, 802–804
 - design, 826–829
 - issues, 805–810
- Output capacitance
 - AM/PM conversion, 795, 799
 - divide-by-2 circuits, 696
 - mixers, 376
 - power amplifiers, 819
- Output impedance
 - common-gate LNAs, 298
 - current sources, 634–635
 - large signals, 780–781
 - matching networks, 69
 - mixers, 357, 366
 - and noise, 48, 52, 54–56
 - PLLs, 634
 - power amplifiers, 809
- Output matching networks, 69, 814
- Output power control, 820
- Output voltage swing, 9
 - flicker noise, 566
 - mixers, 391, 423–424
 - oscillators, 498
 - power amplifiers, 756, 762, 778, 792, 816, 861–863
 - VCOs, 531, 571–572
- Output waveforms for RF oscillators, 501
- Overdrive voltage, 413
- Overlap for blind zones, 536
- Overlapping spectra
 - CDMA, 127–128
 - IEEE802.11, 150
- P**
- Packages
 - coupling between pins, 430
 - power amplifier parasitics, 755
- Pad capacitance, 281, 286–287, 291–293
- PAE (power-added efficiency), 756
- Parallel inductors, 435
- Parallel-plate capacitors, 493–495, 529
- Parallel resistance
 - ideal capacitors, 63
 - inductor modeling, 455–456
- Parameters, scattering, 71–75
- Parasitics
 - active mixers, 396–397
 - class E power amplifiers, 772
 - cross-coupled oscillators, 514
 - divide-by-2 circuits, 694, 879
 - inductors, 439–444, 694
 - LNAs, 260, 313
 - parallel-plate capacitors, 494
 - power amplifiers, 755, 765
 - VCOs, 528–529, 535, 870
- PARs (peak-to-average ratio) in OFDM, 117–118
- Partial channel selection, 168
- PAs. *See* Power amplifiers (PAs)
- Passband signals, 91–92
- Passive devices, 429
 - considerations, 429–431
 - constant capacitors, 490–495
 - inductors. *See* Inductance and inductors
 - modeling issues, 431
 - transformers. *See* Transformers
 - transmission lines. *See* Transmission lines (T-lines)
 - varactors, 483–490
- Passive filters, 158

- Passive impedance transformation, 62–63
 - matching networks, 65–71
 - quality factor, 63
 - series-to-parallel conversions, 63–65
- Passive mixers, 350, 867
 - carrier feedthrough, 413–416
 - current-driven, 366–368
 - gain, 350–357
 - input impedance, 364–367
 - LO self-mixing, 357
 - Miller dividers, 704–705
 - noise, 357–364
 - upconversion, 409–413
- Path loss, 121–122
- Patterned ground shields, 466
- PCS1900, 132
- PDs (phase detectors) in phase-locked loops, 597–600
- Peak detection, 790
- Peak-to-average ratio (PARs) in OFDM, 117–118
- Peak-to-peak voltage swing, 8–9
- Peak value, 18
- Peaking amplifiers, 811
- Performance
 - high-speed dividers, 690
 - mixers, 338–343, 408–409
 - oscillators, 497–501
 - power amplifier linearization, 787
 - trends, 2
- Periodic impulse response, 559
- Periodic waveforms, low-pass filters with, 101
- Periods in phase noise, 536
- Perpendicular resultants in FM signals, 97
- PFDs. *See* Phase/frequency detectors (PFDs)
- Phase detectors (PDs) in PLLs, 597–600
- Phase-domain models for PLLs, 607
- Phase errors
 - GSM, 135
 - PLLs, 600–601, 603–606, 608, 611, 615
 - QPSK, 108
- Phase feedback in polar modulation, 798–799
- Phase/frequency detectors (PFDs)
 - charge pump capacitive cascades, 615–618
 - fractional-N synthesizers, 718, 734–737
 - nonidealities, 627
 - channel-length modulation, 633–634
 - charge injection and clock feedthrough, 630–632
 - circuit techniques, 634–638
 - up and down current mismatches, 632–633
 - up and down skew and width mismatch, 627–630
 - voltage compliance, 630
 - reset pulses, 737
- Phase-locked loops (PLLs), 597
 - charge-pump, 615–620
 - continuous-time approximation, 622–623
 - design, 646–647
 - frequency multiplying CPPLLs, 623–625
 - higher-order loops, 625–627
 - in-loop modulation, 667–669
 - loop bandwidth, 645–646
 - offset, 670–673
 - PFD/CP nonidealities. *See* Phase/frequency detectors (PFDs)
 - phase detectors, 597–600
 - phase noise, 638–644
 - polar modulation, 798, 800, 802, 825
 - transient response, 620–622
 - type-I. *See* Type-I PLLs
 - type-II. *See* Type-II PLLs
- Phase-locked phase noise profiles, 841
- Phase margin of PLLs, 625, 647–651
- Phase mismatches
 - direct-conversion receivers, 196
 - direct-conversion transmitters, 241
 - multiphase frequency division, 746–747
- Phase modulation (PM)
 - AM/PM conversion, 33–35
 - overview, 95–99
 - power amplifiers, 757
 - tail noise, 567, 569–570
- Phase modulation index, 95
- Phase noise
 - divider design, 709–712
 - frequency planning, 846
 - frequency synthesizers, 720–723, 732–733, 840–843
 - offset PLLs, 672
 - oscillators, 501, 536
 - additive noise conversions to, 550–552, 554
 - basic concepts, 536–539
 - bias current source, 565–570
 - computation, 554–555
 - current impulse, 557–558
 - cyclostationary, 552–553, 565
 - effects, 539–543
 - flicker, 563–564
 - higher harmonics, 564–565
 - injected, 562–563
 - linear model, 548–549
 - noise shaping, 546–548
 - Q, 544–546
 - tail capacitance, 555–557
 - time-variant systems, 559–561
 - time-varying resistance, 553–554

- reference, 643–644
- type-II PLLs, 638–644
- VCOs, 570–572, 638–643, 871–875
- Phase shift
 - Miller dividers, 702
 - offset PLLs, 673
 - oscillators, 504–505, 507, 512, 591
 - polar modulation, 794
 - power amplifier linearization, 787
- Phase shift keying (PSK)
 - quadrature PSK, 107–112
 - signal constellation, 105–106
 - spectrum, 103
 - waveforms, 100
- Phases
 - charge pumps, 616
 - phase/frequency detectors, 612
 - polar modulation, 791, 802, 826
 - QPSK, 109–110
 - VCOs, 579, 581
- Phasor diagrams, 550
 - anti-phase coupling, 585–586
 - in-phase coupling, 585
 - quadrature oscillators, 587
- Piecewise-linear waveforms, 383
- Planar transformers, 470, 473–474
- PLL-based modulation
 - in-loop modulation, 667–669
 - offset PLLs, 670–673
- PLLs. *See* Phase-locked loops (PLLs)
- PM (phase modulation)
 - AM/PM conversion, 33–35
 - overview, 95–99
 - power amplifiers, 757
 - tail noise, 567, 569–570
- PMOS devices
 - channel-length modulation, 633
 - charge pumps, 629
 - cross-coupled pairs, 530–531
 - dividers, 878
 - LNAs, 271, 307, 310, 312
 - mixers, 405, 422
 - noise, 573, 852
 - oscillators, 576, 592
 - PLLs, 636
 - surface states, 44
- PN-junction varactors, 484–486
- Polar modulation power amplifiers, 790
 - basic idea, 790–793
 - design, 824–826
 - improved, 796–802
 - issues, 793–796
- Polyphase filters, 217–224
- Port-to-port feedthrough, 339–343
- Ports, mixer, 337–338
- Positive feedback in oscillators, 504
- Positive-feedback power amplifiers, 819–821
- Power-added efficiency (PAE), 756
- Power amplifiers (PAs), 93, 755–756
 - cascode output stages, 751, 776–779
 - class A, 760–764, 771–772
 - class AB, 767
 - class B, 764–767
 - class C, 768–770
 - class E, 772–775
 - class F, 775–776
 - considerations, 751–754
 - design, 814–815, 861–864
 - cascode examples, 815–819
 - common-mode stability, 866–867
 - outphasing, 826–829
 - polar modulation, 824–826
 - positive-feedback, 819–821
 - power combining, 821–824
 - predrivers, 864–865
- Doherty, 811–813
- efficiency, 755–756
- high currents, 754–755
- large-signal impedance matching, 780–782
- linearity. *See* Linearity and linearization
- OFDM, 117
- outphasing
 - basic idea, 802–804
 - design, 826–829
 - issues, 805–810
 - polar modulation. *See* Polar modulation power amplifiers
 - single-ended and differential, 758–760
- Power combining in power amplifiers, 821–824
- Power consumption trends, 2
- Power control
 - direct-conversion transmitters, 232–233
 - DS-CDMA, 128–129
 - IS-95 CDMA, 138
 - polar modulation, 801
 - power amplifiers, 820
- Power conversion gain in mixers, 339
- Power dissipation
 - LNAs, 263
 - oscillators, 501
 - VCOs, 571
- Power efficiency, 93
- Power gain, 7–9
- Power spectral density (PSD) noise, 37, 44–45
- Predistortion, 787–788
- Predrivers, 864–865, 867
- Prescaler modulus, 674–675, 682–683
- Primary inductances in power amplifiers, 765–767

- Primary turns in transformers, 473–474
 - Program counters in pulse swallow dividers, 674–675
 - Programmable AGC gain, 859
 - Propagation
 - mismatches, 625
 - multipath, 115–116
 - PSD (power spectral density) noise, 37, 44–45
 - Pseudo-random noise, 127
 - PSK (phase shift keying)
 - quadrature PSK, 107–112
 - signal constellation, 105–106
 - spectrum, 103
 - waveforms, 100
 - Pulse shaping, 103–104, 227
 - Pulse-swallow counters, 880, 881
 - Pulse-swallow dividers, 673–677
 - Pulsewidth modulation, 386
- Q**
- Q. *See* Quality factor (Q)
 - QPSK (quadrature PSK) modulation, 107–112
 - EDGE, 136
 - phase noise, 542–543
 - Quadrature amplitude modulation (QAM), 114–115
 - Quadrature downconversion
 - heterodyne receivers, 174–175
 - low-IF receivers, 219–221
 - Weaver architecture, 213
 - Quadrature LO phases, 746
 - Quadrature mismatches, 195
 - Quadrature oscillators, 581
 - basic concepts, 581–584
 - coupled oscillators, 584–589
 - feedback model, 582–584
 - improved, 589–592
 - one-port model, 584
 - simulation, 592–593
 - Quadrature phase separation, 216
 - Quadrature PSK (QPSK) modulation, 107–112
 - EDGE, 136
 - phase noise, 542–543
 - Quadrature upconverters, 227
 - GMSK, 113
 - heterodyne transmitters, 247–248
 - I/Q mismatch, 230–231
 - outputs, 422–424, 844
 - passive mixers in, 411
 - polar modulation, 797–798
 - Qualitative analysis of mixer noise, 377–381
 - Quality factor (Q)
 - definitions, 459–460
 - and frequency, 454
 - inductors
 - differential, 463
 - ground shields, 466–467
 - metal resistance, 444–447
 - T-line, 478, 480
 - passive impedance transformation, 63
 - phase noise, 544–546
 - polar modulation, 796
 - quadrature oscillators, 588
 - varactors, 484, 487, 489, 522–524
 - VCOs, 534–535
 - Quantitative analysis of mixer noise, 381–387
 - Quantization noise, 719–721
 - basic noise shaping, 722–728
 - charge pump mismatch, 736–737
 - DAC feedforward for, 738–742
 - fractional dividers, 742–743
 - higher-order noise shaping, 728–732
 - multiphase frequency division, 745–748
 - out-of-band, 732–733
 - reference doubling, 743–745
 - spectrum, 748–749
 - Quasi-differential pairs
 - active mixers with high IP_2 , 401–402
 - active upconversion mixers, 416–417
 - LNAs, 331–332
 - Quasi-static approximation, 757
- R**
- Radiation resistance, 42, 49–50
 - Rail-to-rail operation
 - LO, 366, 577, 852–853, 867–868
 - PLLs, 636
 - TSCP, 697, 699
 - VCOs, 877–878
 - Raised-cosine spectrum, 104
 - Rake receivers, 138
 - Random bit streams in low-pass filters, 101
 - Random mismatches
 - fractional-N synthesizers, 737
 - up and down current, 637
 - Random process, noise as, 36–37
 - Randomization, modulus, 718–721
 - Rapp model, 758, 838
 - Ratioed logic, 878
 - Rayleigh distribution, 122
 - RC-CR networks
 - image-reject receivers, 203, 209–210
 - low-IF receivers, 215–217
 - Reactance-cancelling LNAs, 303–305
 - Receive bands, 157
 - Receiver/demodulators, 92
 - Receivers (RX), 848
 - AGC design, 856–861
 - AGC range, 836–837

- Bluetooth characteristics, 145–147
 - direct-conversion. *See* Direct-conversion receivers
 - front ends, 156
 - heterodyne. *See* Heterodyne receivers
 - image-reject. *See* Image-reject receivers (IRRs)
 - input level range, 131
 - LNA design, 849–852
 - LNA leakage, 261
 - low-IF, 214–217
 - double-quadrature downconversion, 224–226
 - polyphase filters, 217–224
 - mixer design, 851–856
 - noise, 92, 238, 834
 - nonlinearity, 834–835
 - sensitivity, 131
 - simple view, 4–5
 - system-level considerations, 834–838
 - tolerance to blockers, 131
 - wideband CDMA requirements, 140–143
 - Receiving antenna thermal noise, 42
 - Reciprocal mixing
 - frequency synthesizers, 657–658, 840
 - phase noise, 540
 - Reconstructed error in quantization noise, 738–739
 - Reference cycles in fractional-N synthesizers, 716–718
 - Reference doubling in quantization noise, 743–745
 - Reference frequency in integer-N synthesizers, 656, 660, 664
 - Reference phase noise in PLLs, 643–644
 - Reference sidebands in integer-N synthesizers, 663
 - Reflected waves, 71–73
 - Regeneration mode current-steering circuits, 686–688
 - Regulated cascodes, 634–635
 - Regulator noise in oscillators, 501
 - Replicas, IS-95 CDMA, 138
 - Representation of noise, 46–58
 - Reset pulses in phase/frequency detectors, 613
 - Resettable D flipflops, 613
 - Resistance and resistors
 - cross-coupled oscillators, 516
 - ideal capacitors, 63
 - inductor modeling, 455–456
 - inductor Q, 444–448
 - microstrips, 482
 - noise in, 36, 40–43, 873–874
 - one-port oscillators, 509–511
 - power amplifier loads, 752–753
 - radiation, 42, 49–50
 - skin effect, 448–450
 - T-lines, 477
 - time-varying, 553–554
 - varactors, 487–489
 - Resistance-free coupling with inductors, 470
 - Resistive-feedback LNAs, 269–272, 849–851
 - Resistive termination for LNAs, 264
 - Resolution of ADCs, 837, 858–859
 - Resonance frequency
 - inductor equations, 438
 - VCOs, 519
 - Response decays in PLLs, 621
 - Restoration force in phase noise, 544
 - Retiming flipflops in integer-N synthesizers, 667
 - Return paths in T-lines, 478
 - Return-to-zero (RZ) mixers
 - noise, 357–359
 - passive downconversion, 350
 - passive upconversion, 410
 - Reverse channels, 119
 - Reverse isolation, 72, 260
 - RF chokes (RFC), 752
 - RF design hexagon, 3
 - RF-IF feedthrough, 341, 343
 - RF-LO feedthrough, 341–343
 - Ring oscillators
 - divide-by-2 circuits as, 690–691
 - injection-locked, 709
 - waveforms, 507
 - Ripple
 - charge pumps, 619, 632
 - fractional-N synthesizers, 738
 - integer-N synthesizers, 665, 883, 885–886
 - PLLs, 603, 611, 625–627, 638
 - power amplifiers, 759
 - Roaming in cellular systems, 120–121
 - Roll-off factor, 104
 - RZ (return-to-zero) mixers
 - noise, 357–359
 - passive downconversion, 350
 - passive upconversion, 410
- S**
- S (scattering) parameters, 71–75
 - S/P (serial-to-parallel) converters, 107
 - Sampling filters in fractional-N synthesizers, 665, 738
 - Sampling mixers, 352–354
 - noise, 359–364
 - passive upconversion, 409–410
 - Scattering (S) parameters, 71–75
 - Second intercept points (IP₂), 188
 - Second-order 1-bit $\Sigma\Delta$ modulators, 729
 - Second-order nonlinearity, 29
 - Second-order parallel tanks, Q in, 460
 - Secondary images in image-reject receivers, 212
 - Secondary inductances in power amplifiers, 765–767
 - Secondary turns in transformers, 473–474

- Self-corruption
 - asymmetric signals, 173–175
 - direct-conversion receivers, 179, 190
- Self-mixing LO, 181, 357
- Self-oscillation in divide-by-2 circuits, 691
- Self-resonance frequency of inductor capacitance, 442
- Sense mode for current-steering circuits, 686–687
- Sensitivity
 - overview, 59–60
 - VCOs, 518
 - wireless standards, 131
- Sequence-asymmetric polyphase filters, 221
- Serial-to-parallel (S/P) converters, 107
- Series inductance in LNA common-source stage, 291
- Series inductors, 435
- Series peaking in divide-by-2 circuits, 694–696
- Series resistance
 - ideal capacitors, 63
 - inductor modeling, 455–456
- Series-to-parallel conversions, 63–65
- Servo amplifiers in PLLs, 636
- Settling behavior in integer-N synthesizers, 661–664
- 7-cell reuse pattern, 120
- SFDR (spurious-free dynamic range), 60–62
- Shannon's theorem, 155
- Shift-by-90° operation in image-reject receivers, 200–205
- Shot noise, 46
- Shunt peaking in divide-by-2 circuits, 694–695
- Shunt tail noise in low-noise VCOs, 573
- Sidebands
 - direct-conversion transmitters, 240–243
 - fractional-N synthesizers, 716
 - frequency-multiplying PLLs, 624
 - heterodyne transmitters, 245
 - integer-N synthesizers, 657, 663
 - opposite signs in, 97–98
 - VCO, 628
- $\Sigma\Delta$ modulators
 - fractional-N synthesizers, 726–730, 733, 736–738
 - VCO phases, 748
- Signal cancellation loops, 783
- Signal constellations, 105–112
- Signal-to-noise ratio (SNR). *See* Noise and noise figure (NF)
- Signs in sidebands, 97–98
- Simulators
 - integer-N synthesizers, 884–886
 - power amplifiers, 757
 - varactors, 487
- Sinc pulses, 103–104
- Single-balanced mixers, 348–350
 - active, 369–370, 373
 - input impedance, 365
 - noise, 362, 384
 - passive, 351
 - sampling, 355–356
 - voltage conversion gain, 377
- Single-ended power amplifiers, 758–760
- Single-ended stage in differential LNAs, 315–317
- Single-ended to differential LNA conversion, 320
- Single-sideband (SSB) mixing
 - direct-conversion transmitters, 240–243
 - heterodyne transmitters, 247–248
 - Miller dividers, 706
 - noise figure, 344
- Single-sideband (SSB) transmitters in image-reject receivers, 206
- 16QAM constellation
 - description, 114
 - phase noise, 543
 - spectral regrowth, 118
- 64QAM constellation, 115
- Skin effect in inductors, 448–450, 457
- Sliding-IF receivers, 174–178
- Slope of I/O characteristic, 17
- SNR (signal-to-noise ratio). *See* Noise and noise figure (NF)
- Soft hand-offs in IS-95 CDMA, 139
- Software-defined radios, 199
- Sonnet simulator, 439
- Source-bulk capacitance in LNA common-source stage, 293
- Source impedance in noise figure, 50
- Source switching in charge pumps, 631
- Space diversity in cellular systems, 122
- Spectra
 - amplitude modulation, 94
 - noise, 37–39
 - overlapping, 127–128, 150
- Spectral masks, 130–131
- Spectral regrowth, 118–119
- Spiral inductors
 - equations, 436–439
 - geometries, 435
 - high-IP₂ LNAs, 323–324
 - number of turns factor, 432–434, 436–437, 441–442
 - overview, 431–434
 - stacking, 467
 - transformers, 471
 - VCOs, 520–521
- Split reset pulses, 737
- Spread spectrum (SS) communications, 127
- Spreading sequence code, 127
- Spurious-free dynamic range (SFDR), 60–62

- Spurs, 338
 - direct-conversion receivers, 179, 199
 - fractional, 716
 - frequency synthesizers, 843–844
 - heterodyne receivers, 170–171
 - heterodyne transmitters, 245–248
 - integer-N synthesizers, 664–667
 - Square-wave LOs, 170
 - SS (spread spectrum) communications, 127
 - SSB (single-sideband) mixing
 - direct-conversion transmitters, 240–243
 - heterodyne transmitters, 247–248
 - Miller dividers, 706
 - noise figure, 344
 - SSB (Single-sideband) transmitters in image-reject receivers, 206
 - Stability
 - LNAs, 259–260
 - power amplifiers, 866–867
 - Stacked inductors, 467–470
 - Stacked metal layers in microstrips, 482
 - Stacked spirals
 - high-IP₂ LNAs, 323–324
 - transformers, 473–474
 - Stacked transformers
 - description, 474–475
 - power amplifiers, 821
 - Standards, wireless, 130–132
 - Bluetooth, 143–147
 - GSM, 132–137
 - IEEE802.11a/b/g, 147–151
 - IS-95 CDMA, 137–139
 - wideband CDMA, 139–143
 - State diagrams for phase/frequency detectors, 612
 - Static phase errors in PLLs, 603, 605
 - Static systems, 12
 - Step symmetry of inductors, 464
 - Stern stability factor, 259
 - Striplines, 483
 - Subcarriers in OFDM, 117
 - Substrate
 - capacitive coupling to, 439–440, 450–452, 457–458
 - magnetic coupling to, 452–455, 457–459
 - Superdyne system, 164
 - Supply sensitivity of oscillators, 501
 - Surface states, 44
 - Swallow counters, 674–676, 682, 880, 881
 - Switch on-resistance of VCOs, 535
 - Switch parasitics in band switching LNAs, 313
 - Switch transistors
 - class E power amplifiers, 772–773
 - phase noise, 538
 - VCOs, 534
 - Switchable stages in polar modulation, 824
 - Switched capacitors for VCOs, 533, 872
 - Switching pair current in active mixers, 405, 407
 - Switching power amplifiers, 772–773
 - Symbols in QPSK, 107
 - Symmetric inductors, 435, 460–466, 520–521
 - Symmetrically-modulated signals, 172
 - Synchronous AM detectors, 790
 - Synchronous operation of dual-modulus dividers, 680
 - Synthesizers
 - fractional-N. *See* Fractional-N synthesizers (FNSs)
 - integer-N. *See* Integer-N synthesizers
 - PLLs, 611
 - System-level design considerations, 833
 - frequency planning, 844–848
 - frequency synthesizers, 840–844
 - receivers, 834–838
 - transmitters, 838–840
 - System specifications for oscillators, 497
- ## T
- T-lines (transmission lines), 476–478
 - coplanar, 482–483
 - microstrips, 479–482
 - striplines, 483
 - Tail capacitance
 - flicker noise, 387, 405
 - phase noise, 555–557
 - Tail current
 - cross-coupled oscillators, 513–515
 - passive upconversion mixers, 412
 - phase noise, 556
 - time-varying resistance, 554
 - VCOs, 525–526, 531–532, 874–875
 - Tail noise
 - cross-coupled oscillators, 513, 565–566
 - low-noise VCOs, 573, 575
 - phase noise, 565–570, 708
 - Tails coupling in quadrature oscillators, 589
 - Tapered stages in power amplifiers, 754
 - TDD (time division duplexing), 123–124
 - TDMA (time-division multiple access), 125–126
 - Temperature. *See* Thermal noise
 - Terminals in mobile RF communications, 119
 - Terminating resistors in LNAs, 264
 - Thermal noise, 36
 - direct-conversion receivers, 191
 - MOS transistors, 43–46
 - phase, 566, 568
 - resistors, 40–43
 - Thevenin equivalent of divide-by-2 circuits, 695
 - Thevenin model of resistor thermal noise, 40, 57

- Third intercept points (IP₃), 25–27
- Third-order characteristic, 13
- Third-order intermodulation, 22, 31
- Three-point oscillators, 517–518
- Time constants in PLL transient response, 621
- Time-contracted simulation of integer-N synthesizer loops, 884
- Time diversity
 - cellular systems, 122
 - IS-95 CDMA, 138
- Time division duplexing (TDD), 123–124
- Time-division multiple access (TDMA), 125–126
- Time-variant systems
 - overview, 9–12
 - passive downconversion mixers, 366
 - phase noise, 559–561
- Time-varying resistance in phase noise, 553–554
- Time-varying voltage division in outphasing, 808
- Timing errors in class E power amplifiers, 773
- Tones
 - fractional-N synthesizers, 727–728
 - power amplifiers, 756–757
- Top-biased VCOs, 525–526
- Top current in phase noise, 568–569
- Total frequency, 95
- Total noise power in phase noise, 541
- Total phase
 - modulation, 95
 - VCOs, 579
- Total stored energy in inductor capacitance, 441
- Track-mode noise, 359–361
- Tradeoffs in design, 3
- Transceivers, 92, 119, 155
 - channel selection and band selection, 157–159
 - considerations, 155–157
 - design example, 833
 - integer-N synthesizers, 869–886
 - receivers, 848–861
 - system-level design. *See* System-level design
 - considerations
 - transmitters, 861–869
 - on-off keying, 248–249
 - receivers. *See* Receivers (RX)
 - transmitters. *See* Transmitters (TX)
 - TX-RX feedthrough, 159–160
- Transconductance
 - LNAs
 - common-gate stage, 279–280, 282
 - common-source stage, 288–291
 - differential, 319
 - gain switching, 306
 - mixers, 368, 394–397, 407
 - oscillators, 511
 - quadrature oscillators, 591
 - time-varying resistance, 554
 - VCOs, 875
- Transfer functions
 - fractional-N synthesizers, 722, 724, 728, 732–733
 - integer-N synthesizers, 661–662, 665–666, 669, 693–696, 709
 - integrators, 506
 - LNAs, 277–278, 303
 - noise, 39–41, 544, 569, 638–641, 643
 - oscillators, 544, 547–548, 562
 - PLLs, 606–608, 615, 617–620, 622–623, 649
 - RC-CR networks, 203
 - transformers, 472, 475
- Transformation, passive impedance, 62–63
 - matching networks, 65–71
 - quality factor, 63
 - series-to-parallel conversions, 63–65
- Transformers, 470
 - coupling capacitance, 474–475
 - impedance transforms, 69
 - modeling, 475–476
 - outphasing, 806–807
 - power amplifiers, 753, 767, 821–824
 - structures, 470–475
- Transient response in type-II PLLs, 620–622
- Transistors
 - class E power amplifiers, 772–773
 - cross-coupled oscillators, 514
 - phase noise, 538
 - thermal noise, 43–46
 - VCOs, 534
- Transmission lines (T-lines), 476–478
 - coplanar, 482–483
 - microstrips, 479–482
 - striplines, 483
- Transmission masks in IEEE802.11, 147–148
- Transmit bands, 158–159
- Transmit spectrum masks, 144–145
- Transmitted noise in offset PLLs, 670–671
- Transmitter antenna thermal noise, 42
- Transmitters (TX), 861
 - Bluetooth characteristics, 143–145
 - cell phones, 91
 - considerations, 226–227
 - direct-conversion. *See* Direct-conversion transmitters
 - GSM specifications, 135–136
 - harmonic distortion, 16
 - heterodyne, 244–248
 - LNA leakage, 261
 - outphasing, 804
 - power amplifiers, 861–867
 - in simple view, 4–5
 - system-level considerations, 838–840

- upconverters, 867–869
 - wideband CDMA, 139–140
 - wireless standards, 130–131
 - wireless systems, 156
 - Trends, 2–3
 - True single-phase clocking (TSPC), 697–699
 - Tuned amplifiers, 444, 512
 - Tuning VCOs, 521–522
 - amplitude variation with frequency tuning, 532
 - continuous, 524–532
 - discrete, 532–536
 - range limitations, 521–522
 - Turn-to-turn capacitances in inductors, 441–442
 - Two-level modulation schemes, 92
 - Two-pole oscillators, 504–505
 - Two-sided spectra, 38
 - Two-tone tests
 - active downconversion mixers, 392
 - intermodulation, 22, 24–25, 28
 - power amplifiers, 756–757
 - sensitivity, 61–62
 - TX-RX feedthrough, 159–160
 - Type-I PLLs
 - drawbacks, 611
 - frequency multiplication, 609–611
 - loop dynamics, 606–609
 - simple circuit, 601–606
 - VCO phase alignment, 600–601
 - Type-II PLLs, 611–612
 - charge pumps, 614–620
 - continuous-time approximation limitations, 622–623
 - design procedure, 646–647
 - frequency-multiplying CPPLLs, 623–625
 - higher-order loops, 625–627
 - loop bandwidth, 645–646
 - PFD/CP nonidealities. *See* Phase/frequency detectors (PFDs)
 - phase/frequency detectors, 612–614
 - phase margin, 647–651
 - phase noise, 638–644
 - transient response, 620–622
- U**
- Undegenerated common-source stages, LNA
 - nonlinearity calculations for, 329–330
 - Uniformly-distributed model of inductor capacitance, 441–442
 - Unilateral coupling in quadrature oscillators, 581
 - Units, 7–9
 - Unity-gain voltage buffers, 602, 607
 - Up currents and pulses
 - charge pumps, 614–615, 630–633, 645–647
 - fractional-N synthesizers, 733–734
 - integer-N synthesizers, 883
 - PLL higher-order loops, 625, 627
 - quantization noise, 739
 - Up skew in PFD/CP, 627–630
 - Upconversion and upconversion mixers, 339, 408
 - active, 416–424
 - design, 867–869
 - heterodyne transmitters, 244–248
 - I/Q mismatch, 229–232
 - linearity, 234–235
 - offset PLLs, 671
 - output spectrum, 844
 - passive, 409–416
 - performance requirements, 408–409
 - polar modulation, 797–798
 - power amplifiers, 758
 - quadrature, 113, 227, 230–231
 - scaling up, 230–231
 - Uplinks, 119
- V**
- V/I (voltage-to-current) conversion
 - downconversion, 368–369
 - upconversion, 867–868
 - Varactors
 - overview, 483–490
 - Q, 522–524
 - VCOs, 519–520, 571, 870
 - Variable coding rates in IS-95 CDMA, 139
 - Variable-delay stages in integer-N synthesizers, 665–667
 - Variable-envelope signals in QPSK, 110
 - Variable-gain amplifiers (VGAs), 860
 - Variance, time. *See* Time-variant systems
 - VCOs. *See* Voltage-controlled oscillators (VCOs)
 - Vector modulators, 227
 - VGAs (variable-gain amplifiers), 860
 - V_{n1} and V_{n2} spectrum in mixers, 360–364
 - Voice signals, 91
 - Voltage compliance issues in PFD/CP, 630
 - Voltage-controlled oscillators (VCOs), 485
 - Bluetooth, 144
 - divider design, 673–674, 692
 - figure of merit, 570–571
 - fractional-N synthesizers, 716, 723
 - free-running, 655
 - frequency multiplication, 610
 - FSK, 112
 - integer-N synthesizers, 656, 666, 869–877
 - low-noise, 573–575
 - mathematical model, 577–581
 - multiphase frequency division, 745–748
 - overview, 518–521
 - phase noise, 638–643, 711–712

Voltage-controlled oscillators (VCOs) (*Contd.*)

- PLLs, 603–606
 - offset, 672–673
 - phase alignment, 600–601
 - PLL-based modulation, 667–668
 - polar modulation, 797–798
 - transceiver design, 842, 845–847
 - tuning, 521–522
 - amplitude variation with frequency tuning, 532
 - continuous, 524–532
 - discrete, 532–536
 - range limitations, 521–522
 - varactor Q, 522–524
 - Voltage-dependent capacitors, 483–490
 - Voltage gain, 7–9
 - conversion. *See* Conversion gain
 - LNA common-gate stage, 276
 - Voltage swings, 9
 - flicker noise, 566
 - mixers, 391, 423–424
 - oscillators, 498, 515
 - power amplifiers, 756, 762, 778, 792, 816, 861–863
 - VCOs, 531, 571–572
 - Voltage-to-current (V/I) conversion
 - downconversion, 368–369
 - upconversion, 867–868
 - Voltage-voltage feedback in common-gate LNAs, 296
 - Volterra series
 - nonlinear currents, 81–85
 - overview, 77–81
- W**
- Walsh code, 127
 - Weaver receivers, 210–213

- White noise, 563–564, 642
- Wideband CDMA, 139–143
- Width mismatches in PFD/CP, 627–630
- Wilkinson combiners, 827–829
- Wilkinson dividers, 828
- Wire capacitance and inductors, 441
- Wire resistance and inductors, 444–448
- Wireless communication overview, 1–3
 - big picture, 4–5
 - RF challenges, 3–4
- Wireless standards, 130–132
 - Bluetooth, 143–147
 - GSM, 132–137
 - IEEE802.11a/b/g, 147–151
 - IS-95 CDMA, 137–139
 - wideband CDMA, 139–143
- Wires
 - bond. *See* Bond wires
 - transmission lines. *See* Transmission lines (T-lines)

X

- XNOR (exclusive-NOR) gates, 152
- XOR (exclusive-OR) gates
 - current-steering circuits, 685–686
 - phase detectors, 598–599
 - PLLs, 603
 - reference doubling, 743

Z

- Zero crossings
 - Miller dividers, 701–702
 - mixer flicker noise, 385–386, 407–408
 - phase-modulated signals, 95
 - phase noise, 536–538, 557–558
- Zero-IF architecture, 179
- Zero second IFs in heterodyne receivers, 171–174