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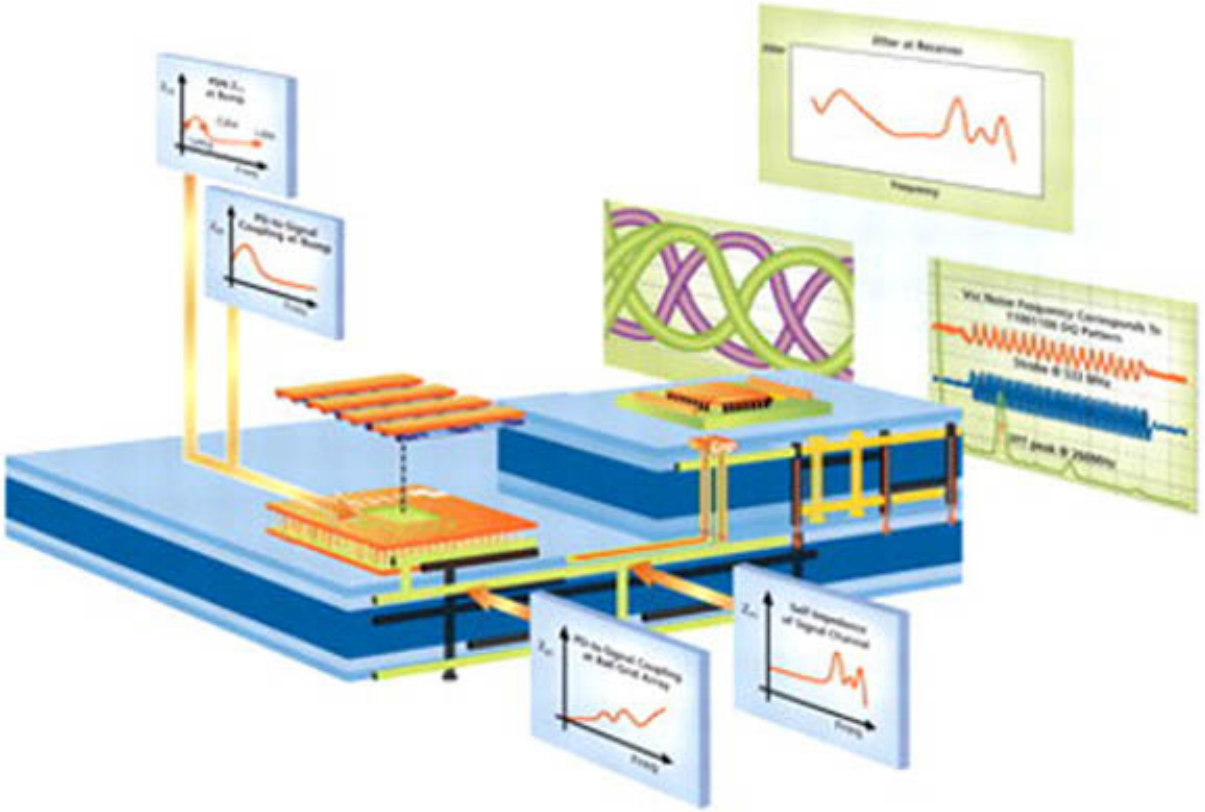
Power Integrity for I/O Interfaces:

With Signal Integrity/Power Integrity Co-Design



Foreword by Joungho Kim

Vishram S. Pandit • Woong Hwan Ryu • Myoung Joon Choi

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Power Integrity for I/O Interfaces

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CONTENTS

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FOREWORD

With recent advancement of the semiconductor technology, microprocessors and System-On-Chip (SoC) products are taking advantage of cheaper production cost and the extended Moore's law. This has reinvigorated more widespread use of personal computing devices and consumer electronics devices. Most of these recent electronics systems are getting faster, smaller, and, are operating at lower power. In addition, the design cycle for products is getting shorter, putting more pressure on efficient design capability while the robust operation of devices is a definite requirement. The issues arising from these trends range from physical design, electromagnetic compatibility, electromagnetic interference, to thermal and power consumption reduction. The designers of the cutting-edge products try to manage all of these problems together while keeping the overall price down as much as possible. Too much over-design tends to make the system lose competitive edge, and under-design apparently makes the system lose its robustness.

Digital design portion of the semiconductor circuit design has advanced significantly since the advent of the transistor CAD design tools. However, for high-speed Input/Output (IO) interfaces, the digital signals pass through power and signal distribution networks, and analog effects become important. The advances in the analog signaling techniques—or more specifically, the advances in the signal and power integrity assurance techniques—had been relatively slow compared with digital design techniques. Electromagnetic effects occurring in the systems were not reflected very accurately in the earlier digital systems. With increase in operating frequencies, it became necessary to consider the transmission line and

electromagnetic effects for signal quality and timing analysis. Availability of more accurate, faster, and more user-friendly electromagnetic simulation tools facilitated the signal integrity analysis.

Power integrity has been catching up with signal integrity in terms of tools, methodologies, and standardized techniques. The initial development of the power integrity techniques in the last decade focused largely on designing for low impedance power distribution networks. Commercial electromagnetic tools to model power networks started to come in the market in late 1990s. With the increase of system speeds and decrease in operating voltages, it was required to design the power network to meet tighter noise tolerances. Simultaneously Switching Output (SSO) noise has become a major noise source, and its analysis and mitigation techniques have been developed. It is necessary to predict the effect of power noise on the receiver jitter. For today's I/O interfaces, operating at multi-Gbps data rates, voltage and timing margins are influenced by the Power Distribution Network (PDN) designs. This book describes a systematic comprehensive methodology for analyzing power integrity, and its impact on the I/O interface performance.

The signal and power integrity is moving faster toward the cheaper and more efficient solution, until the cost of the interference reduction or improved integrity adds up to competitive level. Whatever the means of signal transfer solutions are, the signal and power integrity analysis has been and will dictate significant portion of the system design. With increased system complexity and demand for the low-cost designs, it will become more and more important to analyze power/signal integrity concurrently.

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PREFACE

Power Integrity is becoming increasingly important in today's high-speed digital I/O systems. The cover of this book gives a high-level summary of its system impact. It shows an electronic system with a Printed Circut Board (PCB), a daughter card, and their layer stackup. A driver chip is mounted on the PCB and a receiver chip is mounted on the daughter card. The expanded view of the power grid of the driver chip is also shown. The receiver jitter impact is due to Power Delivery (PD) to signal coupling, and there are different coupling mechanisms. Self impedance response of the PDN at the driver chip shows a resonance in the mid-frequency range. The PD to signal coupling response at the driver chip follows the PDN self impedance response. The jitter at the receiver follows a similar signature at those frequencies when the transmission line effect is negligible. The PD to signal coupling at the package to PCB interface increases as the frequency goes higher. The channel response shows resonances at high frequencies, due to impedance discontinuities. The power to signal coupling noise can get amplified due to the channel effects and resonances. This, in turn, gets translated into jitter at the receiver at high frequencies. Referencing scheme, such as dual referencing, also causes the PD to signal coupling.

Intended audience for this book is Signal Integrity (SI) and Power Integrity (PI) Engineers (On-chip, package, and PCB designers). It can also be used by graduate students who want to pursue careers in these fields. Overall discussion level is beginner to intermediate; however, some advanced topics are also discussed. There may be different designers working on specific components, such as

on-chip or package or PCB. However, this book presents power integrity design techniques along with power-to-signal coupling mechanisms at various stages in the system, such as chip level coupling and interconnect level coupling. This will give the component SI or PI engineers a perspective of system level impact of power integrity, and enable them to proactively design the system to avoid possible problem areas and also to identify the root-cause, in case of any system problems.

Chapter 1, "Introduction," describes digital electronic systems and gives a high-level overview of the PDN and signal network. It describes signal and power integrity effects on system performance and highlights power noise to signal coupling mechanisms. Finally, it addresses the need for concurrent SI/PI design methodology.

Chapter 2, "I/O Interfaces," describes basic Input Output interfaces. The currents in power node generate noise that is basis of power integrity effects for I/O interfaces. This chapter addresses details of single-ended and differential drivers and receivers. Single-ended and differential interfaces produce different current profiles in the PDN, and their dependency on the bit pattern is also different. The PDN current flows are demonstrated with corresponding noise.

Chapter 3, "Electromagnetic Effects," discusses the electromagnetic (EM) theory and how it is important in signal integrity, power integrity and ElectroMagnetic Interference (EMI) analysis. It begins with basic Maxwell's equations, and addresses transmission line theory and interconnect network parameters (Z, Y, S). It also describes Linear Time Invariant (LTI) systems and their properties.

Chapter 4, "System Interconnects," addresses the entire path for power and signal propagation, including the chip, package, and PCB. It gives an overview of the PCB technology and different package types. In the PDN section it describes PCB PDN components (DC/DC converter, PCB capacitors, PCB planes, vias, and so forth), package PDN, and on-chip PDN components (intentional/unintentional capacitors, and power-grid). In the signal network section, it describes PCB signal propagation with microstrip, stripline, and coupled line. It also addresses the package and on-chip signal networks. Then, it states the coupling mechanism from the PDN to signal network. Finally, it addresses modeling tools for the PDN and signal networks.

Chapter 5, "Frequency Domain Analysis," begins with Fourier transform and its properties. It lists the key frequency domain design parameters for signal integrity and power integrity applications. It then addresses frequency domain PDN design with Z_{11} impedance target. It utilizes chip, package, and PCB co-design

approach for the PDN design. Some important frequency domain concepts in the PDN design, such as voltage transfer function, SSO in frequency domain, and power to signal coupling, are illustrated. The next section describes the frequency domain signal network analysis and its correlation. A case study for "crosstalk amplification by resonance" is discussed in detail. The signal network analysis is performed with the PDN and on-chip parameters (on-die termination, pad capacitor, and so on) taken into account. Differential signaling parameters in frequency domain are also presented.

Chapter 6, "Time Domain Analysis," begins with describing the necessary components for the time domain simulations. It addresses various kinds of buffer models used in signal integrity and power integrity analysis. Next, it describes the time domain PDN specifications, and simulation flow to achieve the specifications. Different examples of single ended drivers and differential drivers are presented for AC noise analysis. Next, the concept of chip level driver noise coupling on the signal is discussed. It shows examples of the jitter analysis due to the PDN noise, for single ended and differential interfaces.

Chapter 7, "Signal/Power Integrity Interactions," is devoted to unintended interactions between power/ground and signals, which has become an important consideration for optimizing high-bandwidth I/O signaling scheme. Power noise coupling can be amplified through channel resonance. It describes the power noise amplification mechanism that is due to a combination of three factors: SSO generation, power to signal coupling, and signal channel resonance. Then two case studies are demonstrated: DDR2-800 control bus resonance problem and DDR2-667 Vref bus noise issue. Next, it describes the referencing/stitching/and decoupling effects for single ended and differential interfaces.

Chapter 8, "Signal/Power Integrity Co-Analysis," addresses the eye-margin analysis with SI-PI co-simulations. It describes the basic elements for the co-simulations: buffer models, 3D EM models for package and PCB, on-chip PDN models, and so on. The simulation deck is constructed and the worst case pattern is identified. Full-time domain simulations are performed with ISI, crosstalk, and SSO analysis; and response decomposition techniques are illustrated. The linear interaction indicator between power and signal is defined and evaluated for single ended and differential interfaces.

Chapter 9, "Measurement Techniques," covers the frequency domain and time domain measurement techniques for validating signal/power integrity, in high-speed I/O signaling. The theory and some applications of the enhanced 2-port

VNA technique for low impedance power delivery network characterization are discussed in the first part of this chapter. It also describes the on-chip interconnect and pad capacitance characterization techniques. In addition, it presents S-parameter measurement-based extraction methods to obtain the high-frequency SPICE model, with microwave network analysis and parametric optimization. Next, it describes the time domain characterization techniques. It includes Time Domain Reflectometry (TDR) measurement, PDN noise measurement, SSO coupling measurement, and jitter measurement.

CHAPTER 1

Introduction

In a digital electronic system, when high-speed signals pass through the interconnect network, different unwanted effects such as Inter Symbol Interference (ISI) and crosstalk are produced that degrade the signal integrity. Power integrity is related to noise in the Power Distribution Network (PDN). Various techniques have been developed to model and design the PDN and analyze the noise impact [1, 2]. Simultaneously Switching Output (SSO) noise is produced when charging/discharging currents from the multiple buffers go through the PDN. This noise affects the circuit response and produces timing skews and delays. The power noise is coupled to signals at the chip level and at the interconnect level. It is becoming increasingly essential to determine not only the PDN noise, but also the margin degradation due to the noise coupling to signals. Due to ISI, crosstalk, SSO, and combinations thereof, the signal quality and timing margin becomes degraded at the receiver. System designers need to consider a concurrent design methodology to evaluate power integrity and its effects on signal integrity.

1.1 Digital Electronic System

The digital electronic system comprises a processing unit and an I/O controller unit. Different types of data flow from one part of the system to others in digital format, on different buses. Internal buses communicate within the different components of the system, and external buses communicate with the external devices. Various networking devices communicate with the digital electronic system with different protocols and standards. The I/O controller unit manages various types

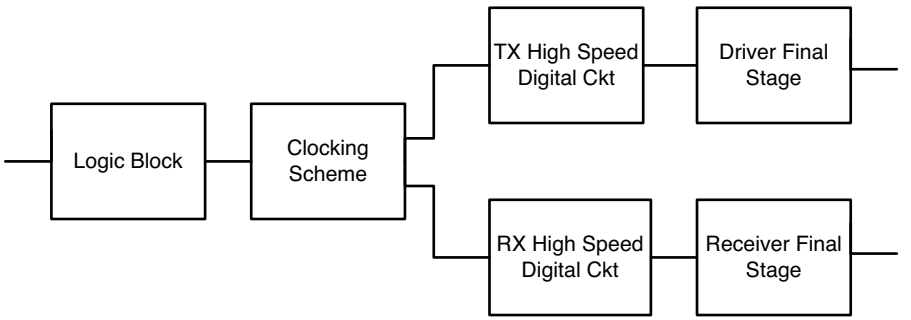

Figure 1.1 Input output interface

of input and output data on the buses and networking devices. The processing unit and the I/O controller unit are on different integrated circuits or chips in a conventional personal computer system, whereas they are on the same chip in a System-on-chip– (SoC) based platform. The I/O controller unit has several I/O interfaces that communicate with different I/Os. Figure 1.1 shows the block diagram of a typical I/O interface in a digital system.

A typical I/O interface has a logic block, clocking scheme, transmitter block, and receiver block. The logic block consists of digital circuits that communicate with the processing unit. The clocking is based on individual interface architecture and provides clocking for transmitter and receiver blocks. It can include Phase Locked Loops (PLLs) or Delay Lock Loops (DLLs). There are two types of I/O interfaces: a single-ended interface and a differential interface. The transmitter unit has high-speed digital circuits and a final stage driver unit. Transmitter high-speed digital circuits can include a predriver, equalizer, multiplexer, and parallel-to-serial converter, and so on, depending on the architecture and interface type. Similarly, the receiver block has high-speed digital circuits and a final stage receiver unit. Receiver high-speed digital circuits can include a sampling amplifier, serial-to-parallel converter, and so on, depending on the interface type and architecture. Single-ended and differential interfaces have different types of drivers, receivers, and high-speed digital circuits.

1.2 I/O Signaling Standards

Examples of the logic families include Transistor Transistor Logic (TTL), Complementary Metal Oxide Semiconductor Logic (CMOS), Emitter Coupled Logic (ECL), and Bipolar Complementary Metal Oxide Semiconductor Logic (Bi-CMOS). Voltage requirements for the I/O signaling are dependent on the semiconductor

process. The I/O standard defines a circuit topology with a logic family. It includes driving current, operating voltage, termination schemes, and switching behaviors [3].

I/O signaling can be in voltage mode or current mode. In voltage-mode circuits, the information processed by the electric network is represented by nodal voltages. In current-mode circuits, information processed is represented by branch currents. The sensing circuit at the destination determines the logic or signal state. The signal state is determined by the voltage value in voltage mode signaling, whereas it is determined by the current value in current mode signaling.

1.2.1 Single-Ended and Differential Signaling

Single-ended and differential signaling is categorized based on how voltages and currents are observed at the driver and the receiver. Figure 1.2 shows a single-ended signaling link. It comprises a driver, a receiver, and a transmission line from the driver to the receiver.

A single-ended driver has one output port and assumes a common ground or power connection as a reference. For a single-ended receiver, there is one input port that assumes a common ground or power connection as a reference. In this chapter and in Chapter 2, "I/O Interfaces," generic nomenclature is used for power (Power) and ground (Gnd) nodes, for the driver as well as the receiver. Power nodes are electrically different from the driver and the receiver due to PDN parasitics. Similarly, the ground nodes are electrically different for the driver and the receiver.

The single-ended signaling scheme with two input terminals at the receiver is shown in Figure 1.3. Similar to the previous scheme, it also has a single output terminal at the driver. This terminal is referenced to common power or ground.

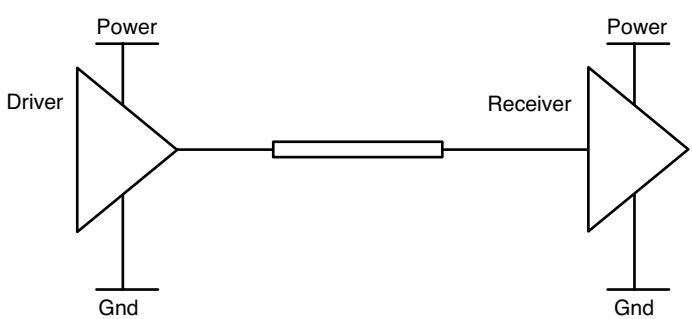

Figure 1.2 Single-ended link

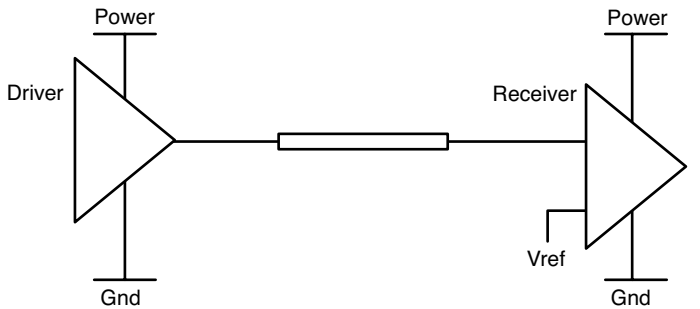

Figure 1.3 Single-ended link with Vref at RX

However, at the receiver end, there is one input terminal along with a locally generated reference voltage (Vref). This receiver has a differential amplifier, so it is similar to a pseudo differential receiver. Overall link is still a single-ended link. This locally generated Vref is on the Printed Circuit Board (PCB) and is primarily used to compensate the DC and low-frequency voltage drop. A single-ended push-pull driver can be designed in a current mode or a voltage mode configuration [4].

A single-ended signal has a power or ground reference or both. The referencing scheme can be identified by the proximity of the signal line to the power or ground domains. The proximity of the signal to the power or ground domain tends to make a return path to the domain in high frequencies, because capacitive coupling makes a low impedance path between the signal and that domain. Frequently, unintentional referencing change occurs in complex multilayer PCBs. When the signal is routed on the board from one layer to the other layer, there may be some regions with signal over void. The signal's reference change due to the vertical structure inside of a rather flat power/ground domain structure works as one of the major sources of unintended radial wave propagation. It contributes to signal noise and power delivery noise when it is captured by other structures inside of the PCB. In addition to referencing change, rather loose coupling of single-ended signaling makes it more susceptible to noise than differential signaling. In general single-ended signaling is preferred in many interfaces including Double Data Rate (DDR) memory signaling because of its rather simpler structure, less pincount, and simpler buffer circuit.

Figure 1.4 shows a differential link. A differential driver can be designed in a current mode or a voltage mode configuration [5]. A differential driver has two ports, which are separate from the power or ground connections. At the driver output, the differential signal is referenced from one of its ports to the other ports. At the driver output, two transmission lines are connected to the output ports. These lines

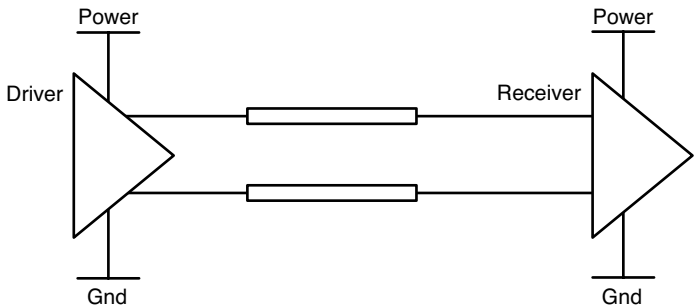

Figure 1.4 Differential link

are coupled lines: tightly coupled or loosely coupled. Tightly coupled differential links typically perform better at higher data rate and are physically smaller than loosely coupled ones. If the reference power or ground plane is far away, then one line has the other line as a reference. However, for most of the practical systems, due to the vicinity of the reference planes, most of the return current goes through the reference planes. At the input of the receiver, there are two ports, which are different than power or ground connections. At the receiver input, the signal is referenced from one port to the other port. Differential signaling can achieve higher data rates and has low susceptibility to noise. The impact of power/ground noise coupling to signal line on differential signaling is less than that on single-ended signaling. However, differential signaling requires twice the number of wires compared to those for single-ended signaling. More number of wires results in a higher cost of the system. The mismatch of the coupled lines causes common mode fluctuations at the receiver; therefore either a well-designed receiver, well-matched coupled lines, or both are needed to fully utilize the advantages of differential signaling.

Chapter 2 describes in details single-ended and differential drivers/receivers with the associated currents in different nodes. When the interface is switching, the current is generated on the power and ground nodes of the circuits. This current produces noise at the chip, which gets coupled to the signal lines.

1.3 Power and Signal Distribution Network

Chapter 4, "System Interconnects," describes the power and signal distribution networks, and their interactions. For a semiconductor I/O interface, the driver and receiver circuits are implemented in the chip. The chip is packaged and then placed on a PCB. The block diagram of the PDN and signal network is shown in Figure 1.5.

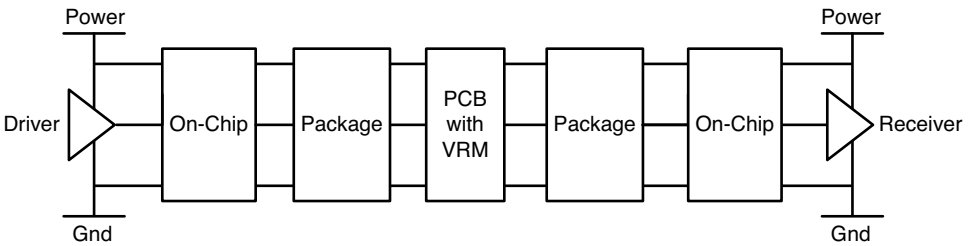

Figure 1.5 Power and signal distribution network

PCB PDN comprises Voltage Regulator Module (VRM), power/ground plane structure, and decoupling capacitors. The VRM converts the input voltage from the power supply to the desired DC output. PCB typically has a multilayer stackup, and power and ground planes form a cavity structure. Package PDN can have a power/ground plane structure and package capacitors. The package connects to the chip at the pad or the bump. The power routes from the bump to the I/O circuit through the on-chip interconnects.

The signal network is routed on the chip, on the package, and then on the PCB. The impedance mismatch at the interface can cause the signal reflections. The two basic types of transmission lines in a package and PCB are microstrip and stripline. Differential signaling utilizes coupled lines. Chapter 4 also describes the details of the on-chip power and signal networks, and Chapter 9, "Measurement Techniques," illustrates the characterization of on-chip components.

1.4 Signal and Power Integrity

The I/O signal integrity addresses two major concerns in the electrical design aspects—the timing and the quality of the signal. Timing is critical in a high-speed digital system. Signal timing pertaining to interconnects depends on the delay caused by the electrical length of the interconnect structure where the electromagnetic energy flows from one end to another. It also depends on the modes of the signal propagation—even and odd modes especially in an inhomogeneous medium, that is, microstrip line. The even mode is the behavior of system when driven with identical signals of the same magnitude and same phase. The signal propagation delay can be increased, for the microstrip line, due to the even mode excitation. By contrast, the odd mode is the behavior of a system when it's driven by identical signals of the same magnitude but with different phase. An odd mode type of excitation would make signals faster for the microstrip line. In summary, signal propagation delay in odd mode is shorter than that in the even mode due to

signal coupling in a microstrip or embedded microstrip. Lowering even/odd mode coupling results in lower timing jitter. We can achieve less mode coupling by using low k and thinner dielectric PCB in the microstrip systems. However, for a homogeneous medium, such as a stripline, the phase velocity of even and odd mode propagation is the same. Furthermore, we need to carefully examine all other coupling mechanisms due to 3-dimentional structures, for example vias, connectors, and so on. Electromagnetic simulation can help determine acceptable levels of coupling. Chapter 3, "Electromagnetic Effects," describes the fundamentals of electromagnetic theory and its applications for the signal and power integrity analysis.

Signal waveform distortions can be caused by many different mechanisms, but three major noise sources exist. The first noise element is the ISI. For multidrop single-ended interfaces, it is primarily caused by reflection noise due to impedance mismatch, stubs, vias, and other interconnect discontinuities causing energy disruption along the signal path. For high-speed differential interfaces, it is primarily due to the PCB losses, having different transfer function at different frequencies. The effect of ISI causes a reduction in the system voltage margin by reducing the peak and causes an ambiguity in the timing information. The second noise element is the crosstalk noise due to electromagnetic coupling between adjacent signal traces and vias. The third noise element is the power/ground noise due to parasitics of the power/ground distribution system during the drivers' SSO. It is sometimes also called ground bounce, Delta-I Noise, or Simultaneous Switching Noise (SSN). In addition to these three kinds of electrical integrity problems, other Electromagnetic Compatibility (EMC) and Electromagnetic Interference (EMI) problems can contribute to the signal waveform distortions. Signal integrity, power integrity, and EMI are all based on the same electromagnetic fundamentals and cannot be separated.

Power integrity for I/O interfaces is related to the voltage variations in the power/ground network due to the noise. The power/ground noise causes various problems in high-speed systems, such as logic failure, EMI, timing delay, and jitter, as shown in Figure 1.6. The power integrity problems can be identified and root-caused based on the electromagnetic Maxwell's equations. The system noise margin requirements may not be satisfied when power integrity problems happen. The power integrity has several impacts to the I/O signaling as follows:

1. **Signal Quality**: Power noise exists on the signals due to the coupling power/ground noise in signal interfaces through signal reference transition.
2. **Timing Delay/Jitter (Lateral SSO push-out or pull-in, slew rate impact)**: The I/O interface has three stages: logic stage, high-speed I/O stage (clocking and other circuitry such as predrivers), and final stage (driver/receiver circuitry).

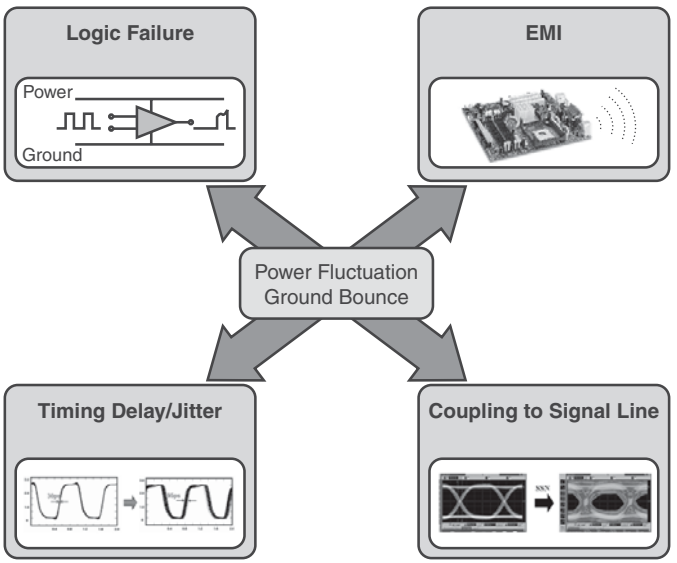

Figure 1.6 Power noise impact on IO signaling

There is a delay associated with the multiple stages of devices the signal needs to pass through from core logic to the I/O output stage. As the rail voltage fluctuates, the delay through each stage increases or decreases. So the time from an edge leaving the core to the time it arrives at the output of the I/O interface can change with power/ground noise. Also, the signal edge will be faster or slower depending on the power/ground noise. All these internal stages may or may not be tied to the same power/ground networks as the final I/O stage (driver, receiver). Noise coupling from other stages need to be considered when determining the supply noise induced timing variations.

3. **Functionality**: Power/ground voltage fluctuations disturb the data in the latch; then logic error, data drop, false switching, or even system failure can occur. This can happen when the noise causes the signal voltage to fall below VIH (input high level) minimum or above VIL (input low level) maximum.

1.5 Power Noise to Signal Coupling

When an I/O interfaces is switching, SSO noise is produced when rapid charging/discharging currents flow through the PDN. The power to the signal coupling can be attributed to two major mechanisms. First is the chip level SSO coupling and the second is the interconnect level SSO coupling.

1.5.1 SSO

SSO or SSN occurs in a system with multiple buffers nearby switching at the same time, as shown in Figure 1.7. Rapid current draws from the buffers leave instantaneous void of electrons in power and ground planes. The instantaneous formation of an electron void may be too fast in a high-speed channel for the electrons from the nearby capacitor to fill in, which shows up as noise in the PDN that should be kept as stable as possible. As a result of the PDN fluctuation, signals of the buffers in the vicinity are affected, so the simultaneous switching impacts not only the PDN but also signal outputs. In this process, inductance in the PDN contributes to the voltage variation of the PDN through Delta-I noise. The term Delta-I refers to the di/dt voltage drop due to the inductance. SSO noise can occur for both single ended and differential drivers [6, 7].

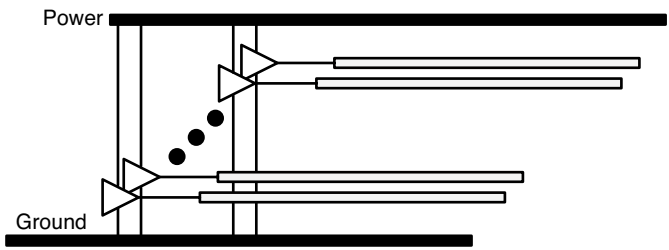

Figure 1.7 Block diagram of multiple buffers switching simultaneously

1.5.2 Chip-Level SSO Coupling

The impact of supply on signaling is dependent on the driver type and the signaling schemes. The power noise at the driver is coupled to the signals at the chip level. SSO noise at the buffer power/ground nodes propagates in the package and the PCB. This noise depends on the impedance of the PDN at the chip level, which is influenced by various stages on the PDN, including on-chip capacitance and package inductance. The chip level power noise to the signal coupling is significant. This coupling is important for single-ended signaling and differential signaling. Chapter 5, “Frequency Domain Analysis,” describes the PDN resonance behavior and the power to signal coupling in frequency domain. Chapter 6, “Time Domain Analysis,” describes the on-chip power noise coupling and its impact on signal performance in the time domain both for single-ended and differential channels. The power noise coupling at the chip results in signaling impact such as jitter.

1.5.3 Interconnect Level SSO Coupling

There are various mechanisms of interconnect level SSO coupling. A PCB power and signal distribution network includes not only planar conductors but also vertical structures, such as vias. A via is a pad with plated hole for electrical connections between conductor traces on different layers. The flat power-ground plane pair becomes a parallel plate wave guide or parallel plate cavity with short dimension along z-axis, as shown in Figure 1.8. The figure shows the ground net vias that are orthogonal to the power and ground plane structure. When the multiple buffers are switching, the excitation applied to the power-ground plane generates dominant radial waves that propagate in between the two planar conductors, as shown in Figure 1.9. Here, higher order waves are usually small in magnitude. The radial waves picked up by structures that are orthogonal to the planar power-ground conductors become unwanted noise. The noise in the power/ground planar cavity is coupled to the power/ground vias as well as signal vias. If there is a signal trace in between the power and ground cavity, the power/ground noise is coupled to the trace.

Sockets, connectors, and adjacent signal/power vias, introduce electromagnetic coupling between PDN and signal nets. In high-speed channel, these vertical structures with adjacent power/ground nets, and signal nets become vulnerable to the unwanted parallel coupling. Crosstalk in sockets' vertical structures often becomes the source of coupling between the signal and power.

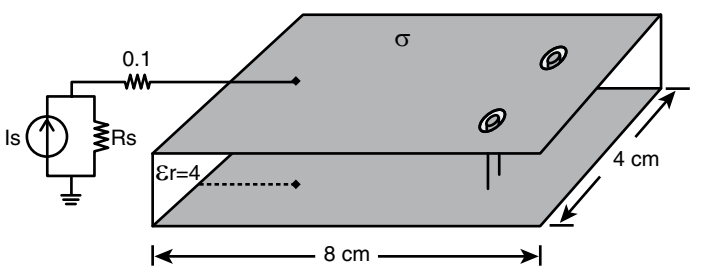

Figure 1.8 Pulse excitation of a power-ground plane pair with 1mm dielectric thickness

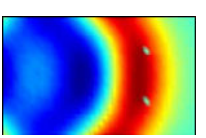

Figure 1.9 Radial wave propagation in power-ground plane pair

Figure 1.10 shows a digital I/O channel with two IC chips: one (MCH) mounted on a PCB and the other (DRAM) mounted on a daughter-card. For the multi-layered high-speed systems, as shown in the figure, Delta-I noise, or SSO generated by I/O buffer switching propagates in the power and ground planes and significantly couples to the interconnects through signal reference transition. The coupled noise can be amplified due to transmission line effect and can cause severe signal integrity problems. In Chapter 7, "Signal/Power Integrity Interactions," various case studies are presented that illustrate the interaction between power and signal integrity including the interconnect level coupling. Chapter 8, "Signal/Power Integrity Co-Analysis," addresses the combined power and signal integrity analysis. It is essential for combined modeling and simulation of signal and power integrity to understand how SSO noise is translated into receiver jitter. Radiated emissions may occur at edge of the printed circuit board (PCB) due to the power/ground noise. Stitching capacitors or vias help mitigate these risks, but the effectiveness of the stitching capacitors appear to deteriorate at speeds higher than a few hundreds MHz.

These types of noise issues and faults are extremely difficult to diagnose and solve after the system is built or prototyped. Understanding and solving these problems before they occur can eliminate having to deal with them further into the project cycle and in turn cut down the development cycle and reduce the cost.

A signaling scheme impacts power integrity and signal integrity because of their coupling differences in various stages of channels. Designing a system with a tight margin necessitates exploring the impact of these signaling options. Generally, differential signaling offers better quality signal at all speeds than single-ended signaling if all the physical conditions are reasonable. Single-ended signaling is usually easier to implement; however, it is usually more susceptible to reference disturbance,

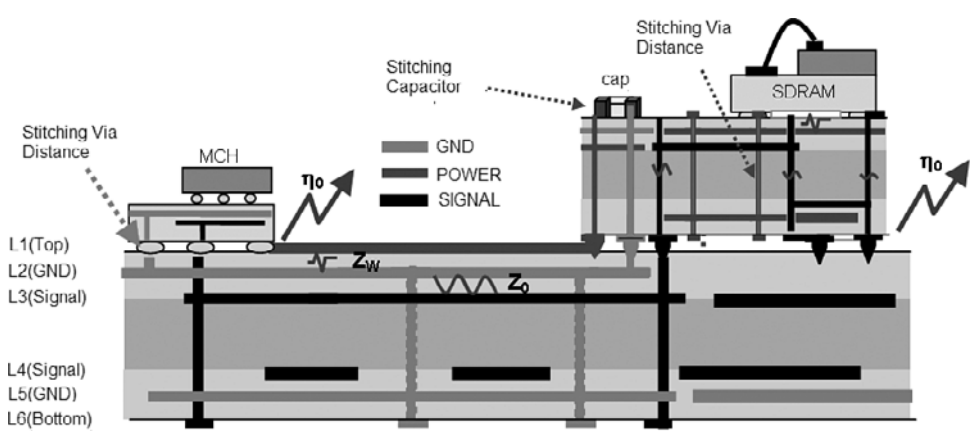

Figure 1.10 Power/ground noise coupling to signal line in a multilayers link

SSO noise, or ground bounce. For single-ended signaling, the impact of power noise coupling at the interconnect level is higher than that for differential signaling. For differential signaling, with lines tightly coupled, common-mode noises affect both lines. Thus at the receiver, the difference between the two lines remains almost constant. Stray transient noise on the two lines will get canceled at the receiver, alleviating the impact due to interconnect level power noise coupling. Chapters 7 and 8 address the power noise coupling to the signal at the interconnect level for single-ended and differential channels. Chapter 9 describes the signal and power integrity measurement techniques, including power to signal coupling characterization.

1.6 Concurrent Design Methodology

Power integrity, signal integrity, and EMC design techniques are inter-related, and their interactions need to be considered. A concurrent design methodology is needed to analyze these interactions [8, 9, 10, 11]. Common mode noise always exists due to power fluctuation and ground bounce. The common mode noise is the main contributor to EMI. The co-design approach considering signal/power integrity and EMC throughout the design, as illustrated in Figure 1.11 (a), is a fundamentally more cost-effective approach compared to a crisis-management approach. If the designer anticipates interactions between signal/power integrity and EMC at the beginning of the design process, and if noise suppression is considered for one stage or subsystem at a time, the noise mitigation techniques are simpler and more straightforward. If the designer proceeds with a disregard of various interactions until the design is close to being finished, mitigation techniques become considerably more costly, less effective, and less available, as shown in Figure 1.11 (b).

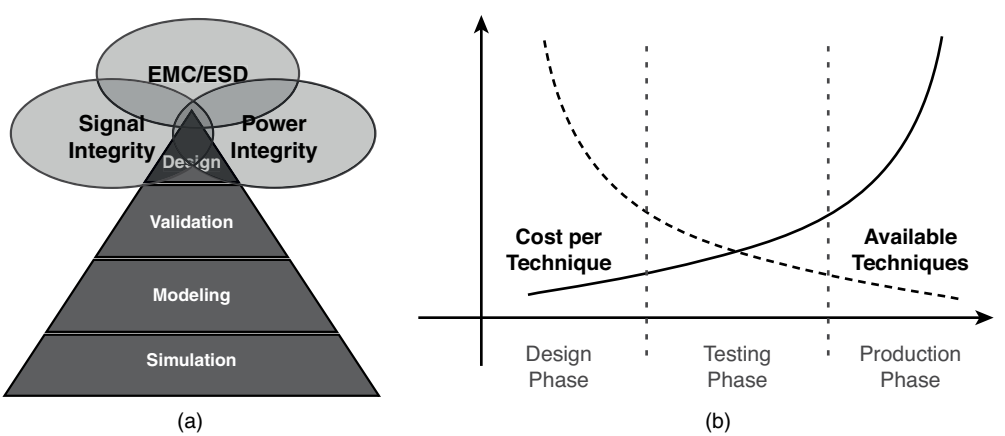

Figure 1.11 Concurrent SI/PI/EMI design

The design methodology proposed in this book is a further unified solution to the co-design of signaling systems by proposing a new metric to unify power integrity and signal integrity designs. In the co-design of signal/power integrity, several sources of coupled noise need to be considered in the signaling system that can degrade the quality of a transmitted signal. As the speed and width of interfaces increase, understanding these signal impediments and designing low-cost solutions become challenging. Signals can contaminate one another through ISI, crosstalk among adjacent signals, and PDN noise. All three items and their interaction need to be closely examined within the signaling system [13]. In summary, this book presents the power integrity design techniques taking into account the effects on signal integrity.

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Numerics

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