Upgrading and Repairing PCs, 15th Anniversary Edition

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Warning and Disclaimer

When reviewing corrections, always check the print number of your book. Corrections are made to printed books with each subsequent printing. To determine the print number of your book, view the copyright page. The print number is the right-most number on the line below the "First Printing" line. For example, the following indicates that this is the 2nd printing of this title and it was printed in August 2003.

First Printing: August 2003

06 05 04 03 4 3 2

First and Second Printing Corrections

Pg	Error	Correction
10	Timeline, left columns 1822 Charles Babbage ~~**conceives**~~ the Difference Engine...	 1822 Charles Babbage **introduces** the Difference Engine...
12	Timeline, right column 1981 Philips and Sony introduce the CD-DA (Compact Disc Digital Audio) ~~**drive. Sony is the first with a CD player on the market.**~~	 1981 Philips and Sony introduce the CD-DA (Compact Disc Digital Audio) **format**. **1982** Sony is the first with a CD player on the market.
15	5th paragraph, 2nd sentence: In 1943, ~~**Alan Turing**~~ completed...	 In 1943, **Tommy Flowers** completed...
18	3rd paragraph, 5th sentence (7th line): Smaller than a thumbnail and packing 2,300 transistors with 10-micron (millionth of a meter) spacing, the $200 chip delivered as much computing ~~**power as the first electronic computer, ENIAC**~~.	 Smaller than a thumbnail and packing 2,300 transistors with 10-micron (millionth of a meter) spacing, the $200 chip delivered as much computing **power as one of the first electronic computers, ENIAC.**
20	1st paragraph after "Birth of the Personal Computer" heading, 3rd sentence: In ~~**late 1973**~~, Intel introduced the 8080 microprocessor,...	 In **April 1974**, Intel introduced the 8080 microprocessor,...

42- 43	Table 3.1: 5th row [386SL], 7th column [Level 1 Cache]: **0KB**[1] 8th row, 1st column: ~~**486SX**~~[2] 12th row, 1st column: ~~**486DX**~~[2] 13th row, 1st column: ~~**486DX**~~[4] 16th row [Pentium 75-200], 14th column [Date Introduced]: ~~**Oct. '94**~~ 18th row [Pentium Pro], 2nd column [CPU Clock]: ~~**2x-3x**~~ 23rd row [Celeron III], 13th column [No. of Transistors]: ~~**28.1M4**~~ 28th row [Pentium II Xeon], 14th column [Date Introduced]: ~~**April '98**~~ 36th row [Itanium 2], 9th column [Level 2 Cache]: ~~**96KB**~~[7] 36th row [Itanium 2], 14th column [Date Introduced]: ~~**June '02**~~	0KB[1] (note the superscript 1; font size is too small in book) **486SX2** **486DX2** **486DX4** **March '94** **2x-4x** **28.1M**[4] [superscript 4] **June '98** **256KB**[7] **July '02**
44	Table 3.2 1st row [AMD K5], 2nd column: ~~**1.5x-1.75x**~~	**1.5x-2x**

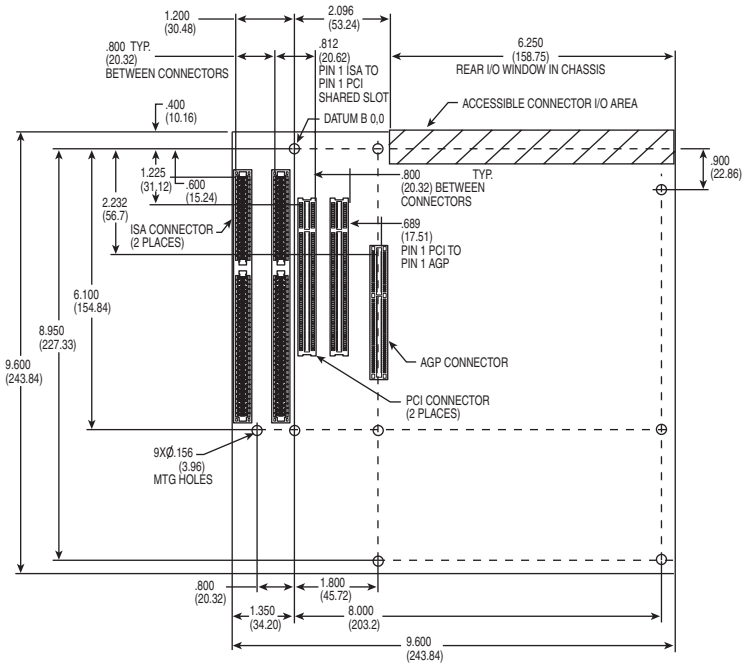
48	2nd paragraph, 1st sentence: More advanced ~~**sixth-generation**~~ processors, such as the Pentium III, Athlon XP, and Pentium 4...	More advanced **sixth- and seventh-generation** processors, such as the Pentium III, Athlon XP, and Pentium 4...
50	5th paragraph: Note that even though Windows Me is based on Windows 98, Microsoft removed ~~**the Startup**~~ menu option in an attempt to further wean us from any 16-bit operation. Windows NT, 2000, and XP also lack the capability ~~**to interrupt the startup in this manner**~~. For these operating systems, you need a Startup Disk (~~**floppy**~~), which you ~~**can create and then use**~~ to boot the system...	Note that even though Windows Me is based on Windows 98, Microsoft removed the **DOS Startup** menu option in an attempt to further wean us from any 16-bit operation. Windows NT, 2000, and XP also lack the capability **to startup DOS in this manner**. For these operating systems, you need a Startup Disk (**CD or floppy**), which you **can use** to boot the system...
54	2nd paragraph, 2nd sentence: For example, a Pentium 4 2.53GHz chip runs at a multiple of 19/4 (4.75x) times the motherboard speed of ~~**533MHz**~~, whereas...	For example, a Pentium 4 2.53GHz chip runs at a multiple of 19/4 (4.75x) times the motherboard speed of **333MHz**, whereas...
70	Table 3.10, 2nd group of bold column headings, last column: ~~**Athlon XP**~~	**Athlon XP**[4] [superscript 4]
71	2nd paragraph, 5th line: universalized and incorporated into ~~**all Pentium**~~ and later processors.	universalized and incorporated into **all 75MHz and faster Pentium** and later processors.

85	Table 3.12 6th row, 1st column: ~~**Socket 62**~~ 9th row, last column: ~~**Aug. '98**~~	 **Socket 6**^{2} [superscript 2] **Nov. '98**
90	2nd paragraph, 2nd sentence: Socket 7, therefore, has 321 pins total in a ~~**21X21**~~ SPGA arrangement.	 Socket 7, therefore, has 321 pins total in a **37X37** SPGA arrangement.
91	4th paragraph, 1st sentence: In ~~**January 1999**~~, Intel introduces a new socket for P6 class processors.	 In **November 1998**, Intel introduces a new socket for P6 class processors.
113	Table 3.17 Delete the 4th row [Banias - duplicate entry] 10th row, last column: Mobile Pentium ~~**4 w/DRAM controller**~~	 Mobile Pentium **3/4 hybrid w/large L2 cache**
115	5th paragraph, 1st sentence: Intel introduced the 8086 processor in ~~**1976**~~. 7th paragraph, 2nd sentence: The 286 chip, first introduced in ~~**1981**~~,...	 Intel introduced the 8086 processor in **1978**. The 286 chip, first introduced in **1982**,...

120	Heading, 3rd column: DX4 (~~**2.5x mode**~~) Speed Heading, 4th column: DX4 (~~**3x mode**~~) Speed Heading, 5th column: ~~**DX4**~~	 DX4 (**2x mode**) Speed DX4 (**2.5x mode**) Speed **DX4** **(3x mode)** **Speed**
125	3rd paragraph, 2nd sentence: The DX2 contains ~~**1.1 million**~~ transistors on a three-layer form.	 The DX2 contains **1.2 million** transistors on a three-layer form.
126	2nd paragraph, 1st line after "AMD 486 (5x86)" heading: The ~~**5x85**~~ offered high-performance...	 The **5x86** offered high-performance...
128	Table 3.19 2nd row, 2nd column: ~~**60, 66, 75, 90, 100, 120, 133, 150, 166, 200MHz (second generation)**~~	 **60/66MHz (first generation), 75/90/100/120/133/150/166/200MHz (second**

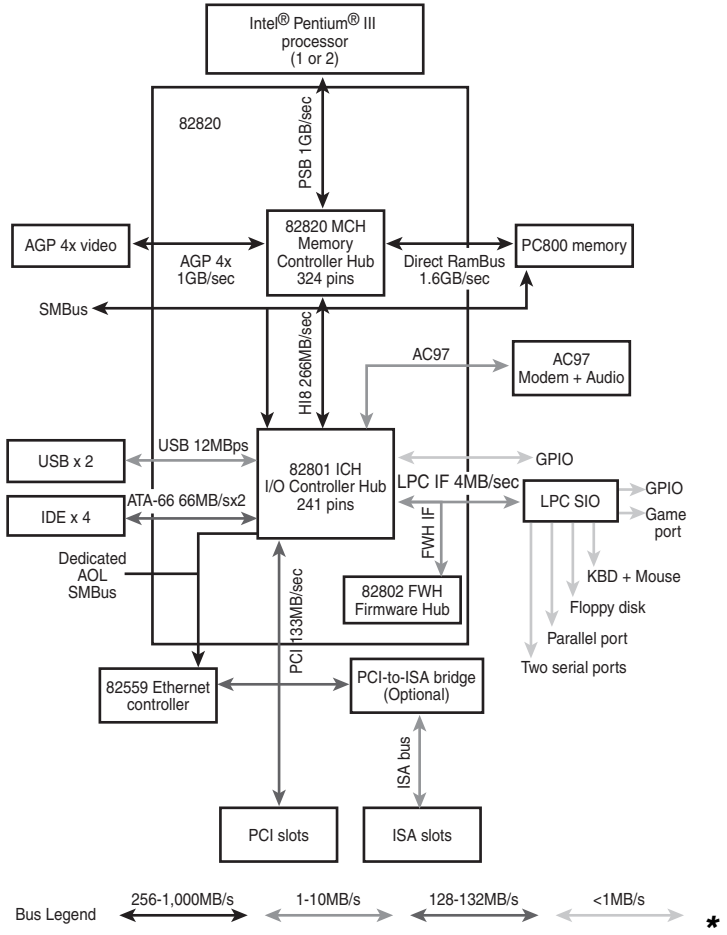
	~~**200MHz (second generation)**~~ 11th row, 2nd column: ~~**3.1 million**~~	**generation)** **3.1 million (first generation), 3.3 million (second generation)**
130	6th paragraph, 1st sentence: ~~**All Pentium**~~ processors are SL enhanced...	**All 75MHz and faster Pentium** processors are SL enhanced...
137	Paragraph after "AMD-K5" heading, 1st sentence: ...available as the PR75, PR90, PR100, PR120, PR133, ~~**and PR-166**~~. Last bulleted item on the page: • Pin-selectable clock multiples of ~~**1.5x and 2x**~~	...available as the PR75, PR90, PR100, PR120, PR133, **PR166, and PR200**. • Pin-selectable clock multiples of **1.5x, 1.75x, and 2x**
141	Table 3.23, third line: CPU ~~**2.5x, 3x**~~	CPU Clock **2x, 2.5x, 3x, 3.5x, 4x**
142	Table 3.24 4th row: Cache~~**8Kx2 L1**~~, 512KB core-speed L2 9th row: Cache memory 8Kx2 ~~**speed L2**~~	Cache**8Kx2 (16KB) L1**, 512KB core-speed L2 Cache memory 8Kx2 **(16KB) L1, 256KB core-speed L2**

142	1st paragraph, after Table 3.24: As you saw in Table ~~**3.5**~~,...	 As you saw in Table **3.4**,...
162	Table 3.30: Remove the last row in the table [1200 133 9x SL5PM...], it is a repeat of a previous row.	
169	3rd paragraph, 1st line: The Athlon is available in speeds from ~~**550MHz**~~ up to...	 The Athlon is available in speeds from **500MHz** up to...
171	Table 3.33: Delete the 9th column [Max. Current (A)]	 Although the figures are taken directly from the AMD datasheet, the max. current x voltage doesn't exactly equal the max. power specs.
171	Table 3.34: Delete the 7th column [Max. Current].	 Although the figures are taken directly from the AMD datasheet, the max. current x voltage doesn't exactly equal the max. power specs.
200	1st paragraph, 6th line: ...and harder to come by. Figure ~~**4.3**~~ shows the onboard features and layout of a late-model Baby-AT motherboard.	 ...and harder to come by. Figure **4.5** shows the onboard features and layout of a late-model Baby-AT motherboard.

212	Figure 4.14, far left side: 9.~~**800**~~ (243.84) [height]	 9.**600** (243.84) [height]
215	4th paragraph, 3rd sentence: In essence, all mini-~~**ATX**~~ boards...	In essence, all mini-**ITX** boards...
220	3rd paragraph, 1st sentence: Note the position of the optional AGP slot shown ~~**previously in Figure 4.13**~~,...	Note the position of the optional AGP slot **shown in Figure 4.20**,...

228	Table 4.7 6th row [Socket 6], 3rd column [Pin Layout]: ~~**1x19 PGA**~~ 12th row [Socket A (462)], 5th column [Supported Processors]: ~~**AMD Athlon/Athlon XP/Duron PGA**~~	 **19x19 PGA** **AMD Athlon/Athlon XP/Duron PGA/FC-PGA**
232	1st paragraph after the table, 3rd line: ...which consisted of two components: the 82443BX North Bridge and the ~~**82371EX**~~ South Bridge.	 ...which consisted of two components: the 82443BX North Bridge and the **82371EB** South Bridge.
235	5th paragraph, last sentence: The LPC bus has a maximum bandwidth of ~~**6.67MBps**~~, which is close to ISA and more than enough to support devices such as ROM BIOS and Super I/O chips.	 The LPC bus has a maximum bandwidth of **16.67MBps**, which is close to ISA and more than enough to support devices such as ROM BIOS and Super I/O chips.
243	Table 4.12, 7th row: Maximum memory ~~**8GB 1GB**~~ 1GB	 Maximum memory **1GB 8GB** 1GB
244	Table 4.14 Heading, 4th column: ~~**815**~~ Heading, 5th column: ~~**815E**~~	 **815**[4] [superscript 4] **815E**[4] [superscript 4]

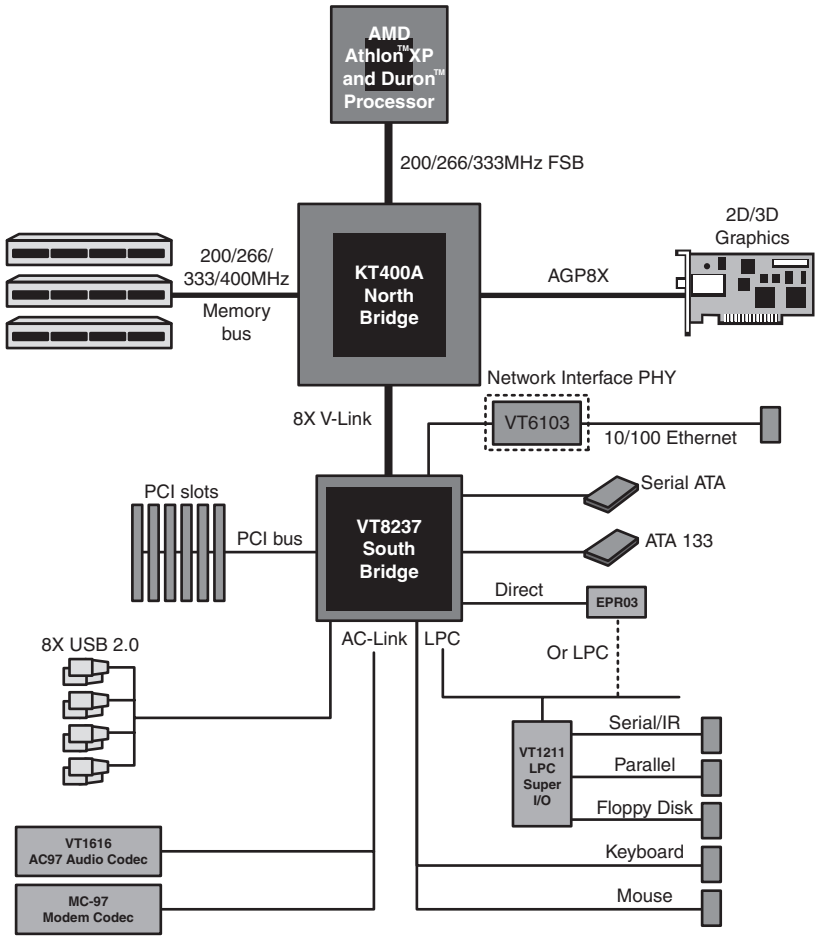
	2nd to last row, last 2 columns: AGP 2~~**x**~~[3] AGP 2~~**x**~~[3] [superscript 3] Footnote 2: 2. The ~~**810**~~ chipsets have integrated...	 AGP **2x**[2] AGP **2x**[2] [superscript 2] 2. These **810/815** chipsets have integrated... 3.
255	1st group of bullet points, 4th bullet: • PC100 or PC133 CL-2 SDRAM (also PC66 with 815G/~~**GE**~~)	 • PC100 or PC133 CL-2 SDRAM (also PC66 with 815G/~~**EG**~~)

258	Figure 4.36, third box in middle of the figure: ~~**82810**~~ ICH I/O Controller Hub 241 pins	 **82801** ICH I/O Controller Hub 241 pins

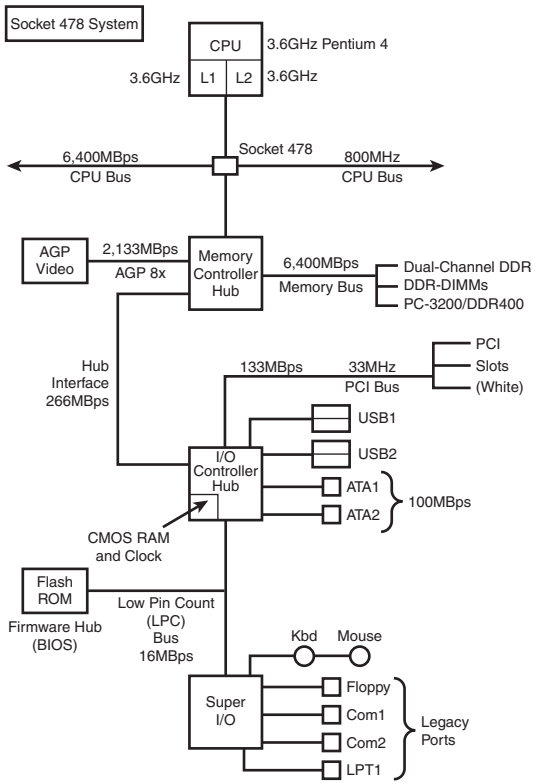
263	6th paragraph, 1st sentence: The VT82C596 South Bridge supports both ACPI and APM and includes an integrated USB controller and dual Ultra ~~**DMA-66 EIDE**~~ ports.	 The VT82C596 South Bridge supports both ACPI and APM and includes an integrated USB controller and dual Ultra DMA-**33 ATA** ports.
263	Second entry of bulleted list: • AGP ~~**1x**~~	 • AGP **2x**
263	Last sentence on the page: The ~~**Apollo Pro consists**~~ of two chips: a VT82C693 North Bridge paired with ~~**either**~~ the VT82C596A ~~**mobile**~~ South Bridge ~~**or the VT82C686A Super South Bridge**~~.	 The **Apollo Pro Plus consists** of two chips: a VT82C693 North Bridge paired with the VT82C596A South Bridge.
264	Table 4.19, heading, 4th column: Apollo ~~**KLE133**~~ (PM601)	 Apollo **PME133** (PM601)
264	Table 4.19 1st row [Part number], 9th column [Apollo Pro 266/266T]: ~~**VT8653**~~	 **VT8633**
264	Table 4.19 13th row [South Bridge], 6th column [Apollo Pro133]: VT82C596B or ~~**VT82C586A**~~ 13th row [South Bridge], 7th column [Apollo Pro133A]: ~~**VT82C686A**~~	 VT82C596B or **VT82C686A** **VT82C596B or VT82C686A**

265	Second section heading and paragraph below it: Apollo ~~**KLE133**~~ The VIA Apollo ~~**KLE133**~~ (previously known as the PM601) chipset is a highly integrated chipset platform designed for the value PC and Internet appliance market. As such, this chipset has a built-in Trident Blade3D graphics engine and 10/100 Ethernet. The ~~**KLE133**~~ is designed for Slot 1 and Socket 370 processors...	Apollo **PLE133** The VIA Apollo **PLE133** (previously known as the PM601) chipset is a highly integrated chipset platform designed for the value PC and Internet appliance market. As such, this chipset has a built-in Trident Blade3D graphics engine and 10/100 Ethernet. The **PLE133** is designed for Slot 1 and Socket 370 processors...
266	First line: The VIA Apollo ~~**KLE133**~~ is a two-chip set consisting of...	The VIA Apollo **PLE133** is a two-chip set consisting of...
272	Table 4.24, 5th column: **ICH4** 828201DB UDMA-100 No No 3C/6P ~~**No**~~	**ICH4** 828201DB UDMA-100 No No 3C/6P **Yes**

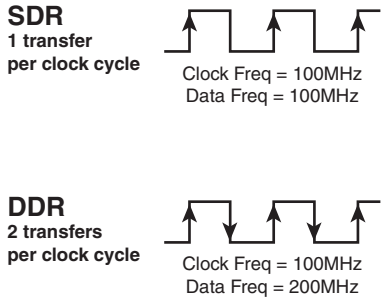
	Yes 2.2 ~~**Mo**~~ Yes SMM/ACPI 2.0 Yes	Yes 2.2 **No** Yes SMM/ACPI 2.0 Yes
281	1st section heading: ~~**M1581**~~/M1563 1st paragraph, 1st sentence: ALi's ~~**M1581**~~/1563 chipset for the Pentium 4 processor brings...	 **M1681**/M1563 ALi's **M1681**/1563 chipset for the Pentium 4 processor brings...
289	Table 4.36 5th row [VT8237], 3rd column [Number of USB ports]: ~~**6**~~	 **8**
290	2nd heading: ProSavage ~~**PM**~~133	 ProSavage **KM**133
290	5th paragraph (below "ProSavage PM133"), 1st sentence: The VIA ProSavage ~~**PM**~~133 integrates...	 The VIA ProSavage **KM**133 integrates...

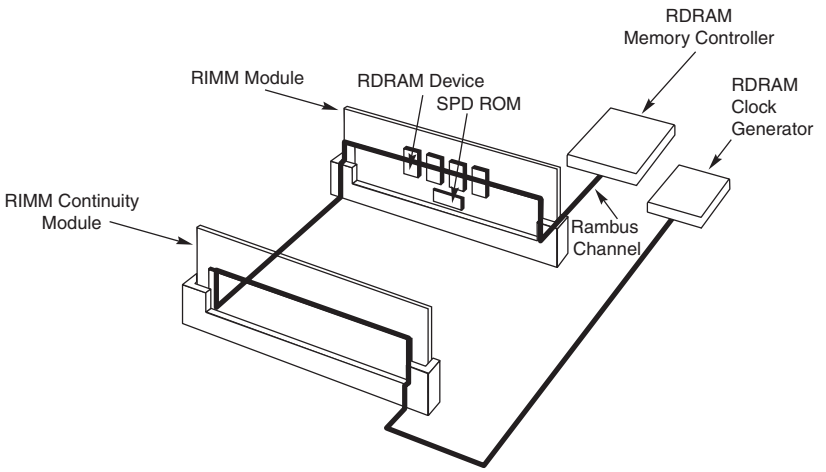
292	Figure 4.44 caption: VIA ~~**VT**~~400A block diagram.	 VIA **KT**400A block diagram.
292	Figure 4.44, text under the second central block (KT400A North Bridge): ~~**6X**~~ V-Link	 **8X** V-Link

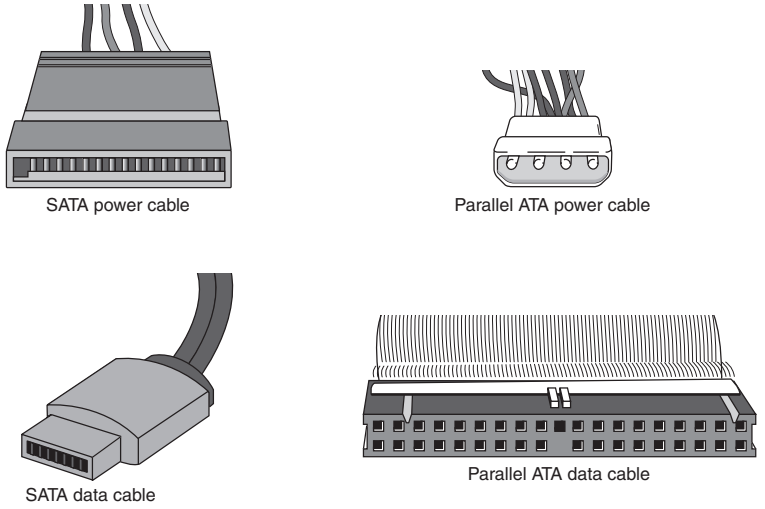
299	Table 4.39 Continued 8th row [HyperTransport Speed], 3rd column [nForce2 IGP]: ~~**400MBps**~~ 8th row [HyperTransport Speed], 4th column [nForce2 SPP]: ~~**400MBps**~~	 **800MBps** **800MBps**
311	Table 4.57 Continued 19th row [USB 2.0], 2nd column [Bus Width]: ~~**2**~~ 19th row [USB 2.0], 3rd column [Bus Speed]: ~~**240**~~	 **1** **480**
317	1st paragraph, 2nd sentence: Note the high-speed CPU bus running up to 333MHz (~~**2,664MBps**~~ throughput) and the use of DDR SDRAM DIMM modules that support a matching bandwidth of ~~**2,664MBps**~~.	 Note the high-speed CPU bus running up to 333MHz (**2,667MBps** throughput) and the use of DDR SDRAM DIMM modules that support a matching bandwidth of **2,667MBps**.

318	Figure 4.55, middle top of figure: Socket ~~423~~	 Socket **478**
319	Paragraph above "The Memory Bus" heading, last sentence: Refer to Table ~~**4.58**~~ for a more complete list of various processor bus bandwidths.	Refer to Table **4.57** for a more complete list of various processor bus bandwidths.

327	Note, 2nd sentence: (In such a case, the local bus-slotted I/O shown in Figure ~~**4.66**~~ would in fact be built-in I/O.)	(In such a case, the local bus-slotted I/O shown in Figure **4.64** would in fact be built-in I/O.)
395	Paragraph above "BIOS Setup Menus," 2nd sentence: Using the Intel ~~**D845PEBT2**~~ ~~**D845PEBT2**~~ motherboard as an example...	Using the Intel **D845PEBT2** motherboard as an example...
400	Table 5.15, 2nd row (PCI Latency Timer), 2nd column (Options): 32(default) ~~**6496**~~ 128 160 192 224 248	32(default) **64** **96** 128 160 192 224 248
405	Table 5.21, 1st row, 1st column [Feature], CHANGE: [blank field]	**Event Log**
433	2nd to last paragraph: Like EDO RAM, your chipset must support this type of memory for it to be usable in your system. Starting in ~~**1997**~~ with the 430VX...	Like EDO RAM, your chipset must support this type of memory for it to be usable in your system. Starting in **1996** with the 430VX...

438	7th paragraph, 1st sentence: Figure 6.1 shows the relationship between clock and data cycles; you can see 5 total clock cycles (each with a falling and a rising edge) and 10 data cycles in the same time.	Figure 6.1 shows the relationship between the DDR (double data rate) clock and data cycles used by RDRAM and DDR SDRAM.
439	Figure 6.1: Replace figure and caption: ***Figure 6.1*** *RDRAM clock and data cycle relationship.*	 ***Figure 6.1*** *SDR (single data rate) versus DDR (double data rate) cycling.*
444	Figure 6.6 caption: ***Figure 6.6*** *A typical **250**-pin DDR2 DIMM. DDR2 modules come in either 64-bit (non-ECC) or 72-bit (ECC) versions.*	***Figure 6.6*** *A typical **240**-pin DDR2 DIMM. DDR2 modules come in either 64-bit (non-ECC) or 72-bit (ECC) versions.*

457	Figure 6.11: replace figure	
471	3rd paragraph, 1st sentence: Adding memory can be an inexpensive solution; at this writing, the cost of memory has fallen to about ~~**half a cent**~~ per megabyte or less.	Adding memory can be an inexpensive solution; at this writing, the cost of memory has fallen to about **12 cents** per megabyte or less.
475	Delete the Note	
477	2nd paragraph: You'll also need to fill in any empty RIMM sockets with a continuity module. Refer to Figure ~~**6.10**~~ for details on adding this module.	You'll also need to fill in any empty RIMM sockets with a continuity module. Refer to Figure **6.11** for details on adding this module.

482	4th paragraph, last sentence: In 32-bit protected mode, the operating systems and applications can access all the memory in the system, up to the maximum limit of the processor (~~**64TB**~~ for most of the Pentium II and later chips).	In 32-bit protected mode, the operating systems and applications can access all the memory in the system, up to the maximum limit of the processor (**64GB** for most of the Pentium II and later chips).
490	1st paragraph under "Extended Memory," 2nd sentence: On a 286 or 386SX system, the extended memory limit is 16MB (16-bit addressing); on a 386DX, 486, Pentium, ~~**Pentium MMX, or Pentium Pro system**~~, the extended memory limit is 4GB (4,096MB, using 32-bit addressing). Systems based on the ~~**Pentium II**~~ and newer processors...	On a 286 or 386SX system, the extended memory limit is 16MB (16-bit addressing); on a 386DX, 486, Pentium, **or Pentium MMX system**, the extended memory limit is 4GB (4,096MB, using 32-bit addressing). Systems based on the **Pentium Pro** and newer processors...
502	Replace Figure 7.1 with:	

518-519	Table 7.6: 6th row [LBA: ATA-1/ATA-5], 2nd column [Total Sectors Calculation]: ~~**228**~~ 7th row [LBA: ATA-6+], 2nd column [Total Sectors Calculation]: ~~**248**~~ 7th row [LBA: ATA-6+], 3rd column [Max. Total Sectors]: ~~**281,474,976,710,655**~~ 7th row [LBA: ATA-6+], 4th column [Maximum Capacity (Bytes)]: ~~**144,115,188,075,855,360**~~ 8th row [LBA: EDD BIOS], 3rd column [Max. Total Sectors]: ~~**18,446,744,073,709,551,600**~~ 8th row [LBA: EDD BIOS], 4th column [Maximum Capacity (Bytes)]: ~~**9,444,732,965,739,290,430,000**~~	 **2^{28}** [superscript 28] **2^{48}** [superscript 48] **281,474,976,710,656** **144,115,188,075,855,872** **18,446,744,073,709,551,616** **9,444,732,965,739,290,427,392**
518-519	Table 7.7, 1st through 7th rows, 5th column [Factor]: 210 220 230 240 250 260 270	 2^{10} 2^{20} 2^{30} 2^{40} 2^{50} 2^{60} 2^{70} [superscripts]

	6th row [10^{18}], 9th column [Value]: ~~**1,152,921,504,606,846,980**~~ 7th row [10^{21}], 9th column [Value]: ~~**1,180,591,620,717,411,300,000**~~	**1,152,921,504,606,846,976** **1,180,591,620,717,411,303,424**
529	5th paragraph, last sentence: Standard CHS addressing is limited to 16 heads and 1,024 cylinders, which provides a limit of ~~**504MB**~~.	Standard CHS addressing is limited to 16 heads and 1,024 cylinders, which provides a limit of **504MiB (528MB)**.
530	5th paragraph, 2nd sentence ...or to be more precise, 9,444,732,965,739,290,~~**430,000**~~ bytes!	...or to be more precise, 9,444,732,965,739,290,**427,392** bytes!
531	1st table, 2nd row [Total Bytes], 2nd column [Max. Values]: 144,115,188,075,855~~**,888**~~	144,115,188,075,855,**872**
531	2nd table, 1st row [Total Sectors], 2nd column [Max. Values]: 18,446,744,073,709,551,~~**600**~~ 2nd row [Total Bytes], 2nd column: 9,444,732,965,739,290,~~**430,000**~~ 3rd row [Megabytes (MB)], 2nd column: 9,444,732,965,739,~~**291**~~ 4th row [Mebibytes (MiB)], 2nd column: 9,007,199,254,740,~~**993**~~	18,446,744,073,709,551,**616** 9,444,732,965,739,290,**427,392** 9,444,732,965,739,**290** 9,007,199,254,740,**992**

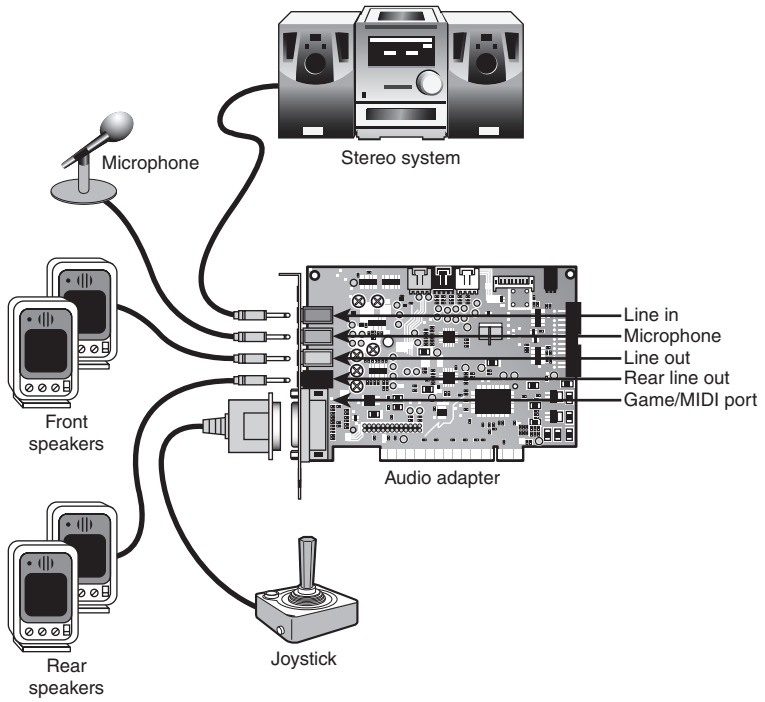
551	Table 8.2, heading, 7th column: Max. No. of ~~**Devices***~~	Max. No. of **Devices**[1]
557	Paragraph after "RAID Arrays," 2nd sentence: RAID (redundant array of ~~**individual drives**~~) technologies are used by both SCSI and ATA drives.	RAID (redundant array of **inexpensive/independent disks**) technologies are used by both SCSI and ATA drives.
576	SCSI Drive table, last row: Average sustained ~~**44.4MBps**~~ transfer rate	Average sustained **43.9MBps** transfer rate
611-612	Table 10.2, 2nd through 13th rows, all columns, CHANGE: 1 598 27.60 306,005 809,241 2 578 26.70 296,107 783,063 3 559 25.81 286,208 756,886 4 540 24.92 276,309 730,709 5 520 24.03 266,411 704,531 6 501 23.13 256,512 678,354 7 482 22.24 246,613 652,177 8 462 21.35 236,715 625,999 9 443 20.46 226,816 599,822 10 424 19.56 216,917 573,645 11 404 18.67 207,019 547,467 12 385 17.78 197,120 521,290 13 366 16.88 187,221 495,113 14 346 15.99 177,323 468,935	1 598 27.61 306,176 809,692 2 579 26.73 296,448 783,966 3 560 25.86 286,720 758,240 4 541 24.98 276,992 732,514 5 522 24.10 267,264 706,788 6 503 23.23 257,536 681,062 7 484 22.35 247,808 655,336 8 465 21.47 238,080 629,610 9 446 20.59 228,352 603,884 10 427 19.72 218,624 578,158 11 408 18.84 208,896 552,432 12 389 17.96 199,168 526,706 13 370 17.08 189,440 500,980 14 351 16.21 179,712 475,254

636	Paragraph below Table 10.7: As you can see, the *true* transfer rate for this drive is between 41.29MBps and 20.64MBps, or an average of about ~~**30.91MBps**~~ —less than one-fourth of the interface transfer rate.	As you can see, the *true* transfer rate for this drive is between 41.29MBps and 20.64MBps, or an average of about **30.97MBps**—less than one-fourth of the interface transfer rate.
644	7th paragraph, 1st sentence: Sony introduced the first 3 1/2" microfloppy drives and disks in ~~**1983**~~.	Sony introduced the first 3 1/2" microfloppy drives and disks in **1981**.
699	last paragraph, 1st sentence: Sony and Philips continued to collaborate on CD standards throughout the decade, and in ~~**1984**~~ they jointly released the Yellow Book CD-ROM standard.	Sony and Philips continued to collaborate on CD standards throughout the decade, and in **1983** they jointly released the Yellow Book CD-ROM standard.
718	4th paragraph, 6th line: ...converted via the 8 to 16 modulation, ~~**320**~~ bits (4 bytes) of synchronization information is added.	...converted via the 8 to 16 modulation, **32** bits (4 bytes) of synchronization information is added.
728	Table 13.8, 4th row, upper section of table: Mib ~~**4,5868,336**~~ 6th row: GiB ~~**4.6 8.3**~~ Lower section of table, 4th row:	Mib **4,4788,140** GiB **4.4 7.9**

	MiB ~~**9,17216,671**~~ 6th row: GiB ~~**9.2 16.7**~~	 MiB **8,95716,281** GiB **8.7 15.9**
728	Table 13.13 heading: Green Book ~~**Mode 1**~~ Sector Format Breakdown	 Green Book **Mode 2** Sector Format Breakdown
805	1st paragraph, 3rd sentence: For ATA hard drives above 528MB (~~**504 megabytes**~~),...	 For ATA hard drives above 528MB (**504 MiB**),
817	step 12, 2nd and 3rd sentences: By default, the new logical drive is formatted with NTFS, but you can choose FAT32 if the logical drive is ~~**32,768MB (32GB)**~~ or less. If the logical drive is ~~**32,769MB or larger, only NTFS can be used to format the drive.**~~	 By default, the new logical drive is formatted with NTFS, but you can choose FAT32 if the logical drive is **34.36GB (32GiB)** or less. If the logical drive is **larger than 32GiB, XP can only format the drive using NTFS.**
846	Table 15.1, last row: WVGA 854X480 ~~**410,240**~~ 1.78	 WVGA 854X480 **409,920** 1.78
864	Table 15.6 17th row [Acer Labs Aladdin TNT2], 3rd column [Supported Processors]:	

	Pentium II/III/Celeron (~~**Slot A and Socket A**~~)	Pentium II/III/Celeron (**Socket 370**)
870	Table 15.9 5th row, 1st column: ~~**800X00**~~ 13th row [1400x1050 16-bit], 4th column [Memory Required]: ~~**8MB**~~ 16th row [1600x1200 16-bit], 4th column: ~~**8MB**~~ 18th row [1600x1200 32-bit], 4th column: ~~**16MB**~~	 **800X600** **4MB** **4MB** **8MB**
871	Table 15.10 1024X768 entry, 5th column [Actual Memory Used] ~~**4.12MB**~~ ~~**5.49MB**~~ 6.75MB 9.00MB 9.00MB 12.00MB	 **4.50MB** **6.00MB** 6.75MB 9.00MB 9.00MB 12.00MB
873	2nd paragraph, 4th & 5th sentences, CHANGE: In **July** 1992, Intel Corporation introduced Peripheral Component Interconnect (PCI) as a blueprint for directly connecting microprocessors and support circuitry. It then extended the design to a full expansion	 In **June** 1992, Intel Corporation introduced Peripheral Component Interconnect (PCI) as a blueprint for directly connecting microprocessors and support circuitry. It then extended the design to a full

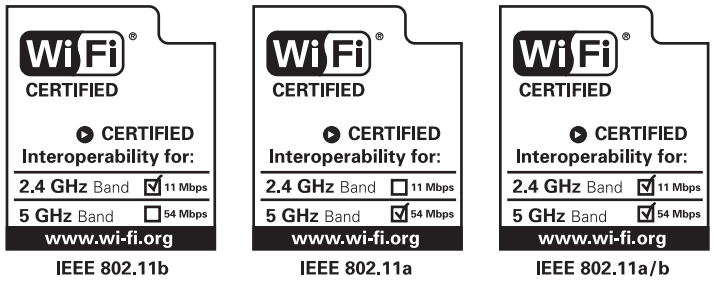
	bus with Release 2 in 1993; the current standard is Release ~~**2.1**~~.	expansion bus with Release 2 in 1993; the current standard is Release **2.3**.
875	Table 15.11, first entry, columns 2-3 ~~**132MBps**~~ ~~**132MBps**~~[1] 533MBps throughput (2X) ~~**1.06GBps**~~ throughput (4X) ~~**2.12GBps**~~ throughput (8X) Footnote 1: 1. At the 66MHz bus speed and 32 bits. Throughput is higher on the 100MHz system bus.	**133MBps** **133MBps**[1] 533MBps throughput (2X) **1,066MBps** throughput (4X) **2,133MBps** throughput (8X) 1. At 33MHz bus speed and 32 bits.

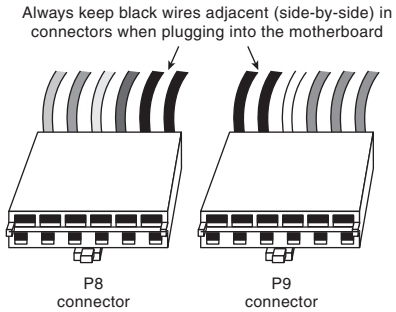
909	Replace Figure 16.1	
946	5th paragraph, 2nd sentence: For example, the top transfer rate possible with EPP/ECP parallel ports is ~~**2MBps**~~,...	For example, the top transfer rate possible with EPP/ECP parallel ports is **2.77MBps**,...
967	Table 17.10, last row: COM4 ~~**2E8-2EFh**~~[1] IRQ3[1]	COM4 **2E8-2EFh**[2] IRQ3[1] [superscript 2]

973	Table 17.13, 3rd column (Transfer Rate) 50KBps 150KBps 150KBps 500KBps-~~**2MBps**~~ 500KBps-~~**2MBps**~~	 50KBps 150KBps 150KBps 500KBps-**2.77MBps** 500KBps-**2.77MBps**
973	Last paragraph, last sentence Transfer rates of up to ~~**2MBps**~~ are possible with EPP.	 Transfer rates of up to **2.77MBps** are possible with EPP.
974	1st paragraph under "Enhanced Capabilities Port" AIn 1992, Microsoft and Hewlett-Packard announced another type of high-speed parallel port is the Enhanced Capabilities Port (ECP).	 In 1992, Microsoft and Hewlett-Packard announced the Enhanced Capabilities Port (ECP), nother type of high-speed parallel port.
975	2nd paragraph, 5th sentence: Using EPP or ECP mode, communications speeds that are as high as ~~**2MBps**~~ can be achieved.	 Using EPP or ECP mode, communications speeds that are as high as **2.77MBps** can be achieved.
976	Last paragraph, last sentence: If both systems use an EPP/ECP port, you can actually communicate at rates of up to ~~**2MBps**~~, which is far faster than the speeds achievable with serial port or infrared (IR) data transfers.	 If both systems use an EPP/ECP port, you can actually communicate at rates of up to **2.77MBps**, which is far faster than the speeds achievable with serial port or infrared (IR) data transfers.

980	2nd to last paragraph, 3rd sentence: With the replacement of the Baby-AT motherboard and its five-pin DIN (~~**an acronym for Deutsche Industrie Norm**~~) keyboard connector...	With the replacement of the Baby-AT motherboard and its five-pin DIN (an acronym for Deutsches Institut für Normung e.V.)...
996	Table 18.2 footnote: DIN = ~~**Deutsche Industrie Norm**~~, a committee that sets German dimensional standards	DIN = **Deutsches Institut für Normung e.V.**, a committee that sets German dimensional standards
1033	1st bullet point, 5th sentence: Maximum downstream speeds are up to ~~**1.6MBps**~~, with up to 640Kbps upstream. 2nd bullet point, 2nd sentence: A slower (1Mbps ~~**upstream**~~) form of DSL that was developed by modem chipset maker Rockwell.	Maximum downstream speeds are up to **9Mbps**, with up to 640Kbps upstream. A slower (1Mbps **downstream**) form of DSL that was developed by modem chipset maker Rockwell.
1034	Table 19.2 5th row [VDSL], 3rd column [Data Rate Downstream; Upstream]: 12.9Mbps 52.8Mbps downstream; 1.5Mbps to 2.3Mbps upstream; 1.6Mbps to 2.3Mbps downstream	12.9Mbps to 52.8Mbps downstream; 1.6Mbps to 2.3Mbps upstream

1046	Note at bottom of page: Because it has become such a familiar term, even to inexperienced computer users, the word *modem* is ~~**frequently**~~ used to describe devices that are, strictly speaking, not modems at all. For example, earlier in this chapter you read about broadband solutions such as ISDN, cable modems, DirecWAY, DSL, and StarBand. Although all these services use devices commonly called "modems" to connect your PC to fast online services, ~~**none**~~ of them ~~**converts**~~ digital information to analog...	Because it has become such a familiar term, even to inexperienced computer users, the word *modem* is **sometimes** used to describe devices that are, strictly speaking, not modems at all. For example, earlier in this chapter you read about broadband solutions such as ISDN, cable modems, DirecWAY, DSL, and StarBand. Although all these services use devices commonly called "modems" to connect your PC to fast online services, **not all** of them **convert** digital information to analog...
1047	1st paragraph, 4th sentence It does this by adding a start bit ~~**before and after**~~ every byte of data...	It does this by adding a start bit **before and a stop bit after** every byte of data,...
1085	Paragraph after "Network Cables," 2nd sentence: Although various types of wireless networks are now on the market, most office and home networks are still based on one of the following ~~**wired topologies**~~:	Although various types of wireless networks are now on the market, most office and home networks are still based on one of the following **media types**:
1098	step-by-step instruction no. 8, 2nd sentence: Verify that the wires are arranged according to the EIA/TIA586B standard *before* you crimp the plug onto the wires (refer to ~~**Table 20.5**~~ and Figure 20.17 earlier in this chapter).	Verify that the wires are arranged according to the EIA/TIA586B standard *before* you crimp the plug onto the wires (refer to **Table 20.5** and Figure 20.17 earlier in this chapter).

1103	Figure 20.24; replace	 Note change from "802.11b/a" to "802.11a/b" in lower right.
1103	Figure 20.24 caption: The Wi-Fi Alliance's certification labels for Wi-Fi-compliant 802.11b hardware (top), 802.11a hardware (middle), and dual-band 802.11b/a hardware (bottom).	Wi-Fi Alliance certification labels for compliant 802.11b hardware (left), 802.11a hardware (middle), and dual-band 802.11a/b hardware (right).
1136	Figure 21.7 caption: SFX-style power supply (with ~~**90mm**~~ top-mounted cooling fan).	SFX-style power supply (with **80mm** top-mounted cooling fan).
1137	last paragraph For systems that require more cooling capability, a version that allows for a larger, ~~**90mm**~~ top-mounted cooling fan also is available.	For systems that require more cooling capability, a version that allows for a larger, **80mm** top-mounted cooling fan also is available.

1138	Figure 21.9 caption: SFX form factor power supply dimensions with an internal ~~**90mm**~~ top-mounted fan.	SFX form factor power supply dimensions with an internal **80mm** top-mounted fan.
1139	Figure 21.11 callout: Always keep black connectors side-by-side when plugging into the motherboard	 Always keep black wires adjacent (side-by-side) in connectors when plugging into the motherboard
1236	Table 23.4, 10th row, 1st column: 2-?-?	2-x-x* (note the asterisk for footnote--the following is the added footnote for after the table, p. 1237: Add the following footnote at the end of the table on page 1237: *2nd and 3rd codes can be 1 through 4 beeps each, indicating different failed bits within the first 64KB of RAM.

1241	Note: Delete entire Note since the 6th edition PDF was not included on the 15th edition DVD.	
1311	Table 24.9 1st row [000h], 4th column [Length]: ~~**446**~~ 9th row [1CAh], 4th column: **1 bytes**	**446 bytes** **4 bytes**
1321	bullet points, 1st bullet, 2nd sentence: The byte containing the flags representing the standard DOS file attributes, using the format shown in ~~**Table 24.18**~~.	The byte containing the flags representing the standard DOS file attributes, using the format shown in **Table 24.20**.
1327	3rd paragraph, 1st sentence FAT16 volumes include 1 sector for the boot record and BPB, two copies of the FAT (default and backup) up to 256 sectors long each, 32 sectors for the root directory, and a data area ~~**with 4,085-65,524**~~ clusters.	FAT16 volumes include 1 sector for the boot record and BPB, two copies of the FAT (default and backup) up to 256 sectors long each, 32 sectors for the root directory, and a data area **with up to 65,524** clusters.
1332	1st paragraph, 1st through 3rd sentences: With FAT32, the cluster numbers range from 00000000h to FFFFFFFFh, which is 0-4,294,967,295 in decimal. Again, some values at the low and high ends are reserved, and	With FAT32, the cluster numbers range from 00000000h to 0FFFFFFFh, which is 0-268,435,455 in decimal. Again, some values at the low and high ends are reserved, and

	only values between 00000002h and FFFFFFF6h are valid, which means values 2-4,294,967,286 are valid. This leaves 4,294,967,284 valid entries, so the drive must be split into that many clusters or less.	only values between 00000002h and 0FFFFFF6h are valid, which means values 2-268,435,446 are valid. This leaves 268,435,445 valid entries, so the drive must be split into that many clusters or less.
1332	Table 24.26 12th row [0000001007], 2nd column [Value]: ~~**FFFFFFFFh**~~ 15th row, 1st column [FAT Cluster #]: ~~**4,294,967,286**~~	 **0FFFFFFFh** **268,435,446**
1334	Caution, 1st sentence: The /Z switch does not override the ~~**65,534**~~-cluster limit on FAT16 partitions,...	 The /Z switch does not override the **65,524**-cluster limit on FAT16 partitions,...
1487	left column: DIN (Deutsche Industrie Norm), 980	 Deutsches Institut für Normung e.V. (DIN), 980
1488	left column: DIN (Deutsche Industrie Norm), 980	 DIN (Deutsches Institut für Normung e.V.), 980

This errata sheet is intended to provide updated technical information. Spelling and grammar misprints are updated during the reprint process, but are not listed on this errata sheet.