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DAQArb™ 5411 User Manual

High-Speed Arbitrary Waveform Generator

June 1997 Edition
Part Number 321558A-01

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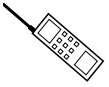
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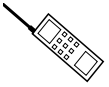
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About This Manual

The *DAQArb 5411 User Manual* describes the features, functions, and operation of the DAQArb 5411. The DAQArb 5411 is a high-speed arbitrary waveform generating device with performance comparable to standalone instruments.

Organization of This Manual

The *DAQArb 5411 User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the DAQArb 5411, lists the optional software and optional equipment, and explains how to unpack your DAQArb 5411.
- Chapter 2, *Installation and Configuration*, describes how to install and configure your DAQArb 5411.
- Chapter 3, *Signal Connections*, describes the I/O connectors, signal connections, and digital interface to the DAQArb 5411.
- Chapter 4, *Arb Operation*, describes how to use your DAQArb 5411.
- Appendix A, *Specifications*, lists the specifications of the DAQArb 5411.
- Appendix B, *Waveform Sampling and Interpolation*, describes the basics of waveform sampling and interpolation.
- Appendix C, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products and manuals.
- The *Glossary* contains an alphabetical list and description of terms used in this manual, including abbreviations, acronyms, metric prefixes, mnemonics, and symbols.
- The *Index* contains an alphabetical list of key terms and topics in this manual, including the page where you can find each one.

Conventions Used in This Manual

The following conventions are used in this manual:

<>	Angle brackets enclose the name of a key on the keyboard (for example, <option>). Angle brackets containing numbers separated by an ellipsis represent a range of values associated with a bit or signal name (for example, DBIO<3..0>).
arb	Arb is a generic term that denotes one or more of the PCI-5411 and AT-5411 arbitrary waveform generating devices.
bold	Bold text denotes the names of menus, menu items, parameters, dialog box, dialog box buttons or options, icons, windows, Windows 95 tabs, or LEDs.
bold italic	Bold italic text denotes a note, caution, or warning.
DAQArb 5411	DAQArb 5411 is a generic term that denotes one or more of the PCI-5411 and AT-5411 arbitrary waveform generating devices.
italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept. This font also denotes text from which you supply the appropriate word or value, as in Windows 3.*x*.
`italic monospace`	Italic text in this font denotes that you must enter the appropriate words or values in the place of these items.
`monospace`	Text in this font denotes text or characters that should literally enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and for statements and comments taken from programs.
	The *Glossary* lists abbreviations, acronyms, metric prefixes, mnemonics, symbols, and terms.

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix C, *Customer Communication*, at the end of this manual.

Chapter 1

Introduction

This chapter describes the DAQArb 5411, lists the optional software and optional equipment, and explains how to unpack your DAQArb 5411.

About Your DAQArb 5411

Thank you for buying a National Instruments DAQArb 5411 device. The DAQArb 5411 family consists of two different devices for your choice of bus: the PCI-5411 for the PCI bus and the AT-5411 for the ISA bus. Your 5411 device has the following features:

- One 12-bit resolution analog output channel
- Up to 16 MHz sine and TTL waveform output
- Software selectable output impedances of 50 Ω and 75 Ω
- Output attenuation levels from 0 to 73 dB
- Phase-locked loop (PLL) synchronization to external clocks
- Sampling rate of 610 S/s to 40 MS/s
- 2,000,000-sample onboard waveform memory
- Waveform linking and looping for arbitrary waveform generation
- Digital and analog filters
- 32-bit direct digital synthesis (DDS) for standard function generation
- External trigger input
- Marker output as trigger output
- 16-bit digital pattern generation with clock
- Real-Time System Integration (RTSI) triggers

All 5411 devices follow industry-standard Plug and Play specifications on both buses and offer seamless integration with compliant systems. If your application requires more than one channel of arbitrary waveform generation, you can synchronize multiple devices on all platforms using

RTSI bus triggers on devices that use the RTSI bus or the digital trigger on the I/O connector.

Detailed specifications of the DAQArb 5411 devices are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use your DAQArb 5411, you will need the following:

- ❑ One of the following DAQArb 5411 devices:
  - PCI-5411
  - AT-5411
- ❑ *DAQArb 5411 User Manual*
- ❑ NI-DAQ for PC compatibles, version 5.0 or later
- ❑ One of the following software packages and documentation:
  - VirtualBench-Arb
  - VirtualBench-Function Generator
  - LabVIEW
  - LabWindows®/CVI
  - Any standard C compiler
- ❑ Cables and accessories
  - SMB to BNC, 50 Ω cable
  - SHC50-68 50-pin to 68-pin cable for pattern generator outputs (optional)
  - SCB-68 terminal block accessory in generic configuration (optional)
- ❑ 16 MB memory module (optional)
- ❑ Your computer

Software Programming Choices

There are several options to choose from when programming your National Instruments DAQ hardware. You can use LabVIEW, LabWindows/CVI, or VirtualBench.

National Instruments Application Software

LabVIEW and LabWindows/CVI are innovative program development software packages for data acquisition and control applications. LabVIEW uses graphical programming, whereas LabWindows/CVI enhances traditional programming languages. Both packages include extensive libraries for data acquisition, instrument control, data analysis, and graphical data presentation.

LabVIEW features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments (VIs) for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

☞ **Note:** ***DAQArb 5411 devices can use only the Advanced Analog Output VIs in LabVIEW for analog output functions.***

LabWindows/CVI features interactive graphics, a state-of-the-art user interface, and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions for using LabWindows/CVI with National Instruments DAQ hardware, is included with the NI-DAQ software kit.

Using LabVIEW or LabWindows/CVI software will greatly reduce the development time for your data acquisition and control application.

VirtualBench is a suite of VIs that allows you to use your data acquisition products just as you use standalone instruments, but you benefit from the processing, display, and storage capabilities of PCs. VirtualBench instruments load and save waveform data to disk in the same forms used in popular spreadsheet programs and word processors. A report generation capability complements the raw data storage by adding timestamps, measurements, user name, and comments.

The complete VirtualBench suite contains VirtualBench-Arb, VirtualBench-Function Generator, VirtualBench-Scope, VirtualBench-DSA, VirtualBench-DMM, and VirtualBench-Logger.

Your DAQArb 5411 kit contains a free copy of VirtualBench-Arb and VirtualBench-Function Generator. VirtualBench-Arb is a turn-key application you can use to generate waveforms as you would with a standard arbitrary waveform generator.

NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ is not packaged with accessory products. NI-DAQ has an extensive library of functions that you can call from your application programming environment.

Whether you are using conventional programming languages, LabVIEW, LabWindows/CVI, or VirtualBench, your application uses the NI-DAQ driver software, as illustrated in Figure 1-1.

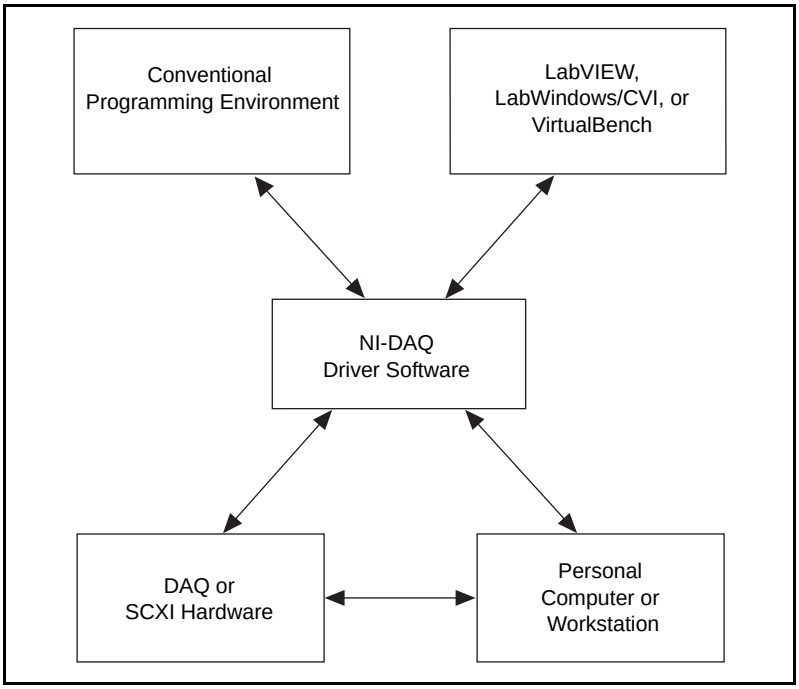


Figure 1-1. The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

Optional Equipment

National Instruments offers a variety of products to use with your DAQArb 5411, including probes, cables, and other accessories, as follows:

- Shielded and unshielded I/O connector blocks (SCB-68, TBX-68, CB-68)
- RTSI bus cables

For more specific information about these products, refer to your National Instruments catalogue or web site, or call the office nearest you.

Cabling

The following list gives recommended part numbers for cables that you can use with your 5411 device:

- BNC male to BNC male, 50 Ω cable from ITT Pomona Electronics (part number BNC-C-*xx*)
- BNC male to BNC male, 75 Ω cable from ITT Pomona Electronics (part number 2249-E-*xx*)
- BNC female to RCA phono plug adapter, from ITT Pomona Electronics (part number 5319)
- BNC 50 Ω feed-through terminator adapter from ITT Pomona Electronics (part number 4119-50)
- BNC female-female adapter from ITT Pomona Electronics (part number 3283)

Unpacking

Your device is shipped in an antistatic package to prevent electrostatic damage to the device. Electrostatic discharge can damage several components on the device. To avoid such damage in handling the device, take the following precautions:

- Ground yourself via a grounding strap or by holding a grounded object.
- Touch the anti-static package to a metal part of your computer chassis before removing the device from the package.
- Remove the device from the package and inspect the device for loose components or any other sign of damage. Notify National Instruments if the device appears damaged in any way. *Do not* install a damaged device into your computer.
- *Never* touch the exposed pins of connectors.

Installation and Configuration

Chapter 2

This chapter describes how to install and configure your DAQArb 5411.

Installation

☞ **Note:** ***You should install your driver software before installing your hardware. Refer to the*** *DAQArb 5411 Read Me First* ***document for software installation information.***

If you have an older version of NI-DAQ already in your system, that software will not work with your device. Install NI-DAQ from the NI-DAQ software CD shipped with your DAQArb 5411.

You can install the PCI-5411 in any PCI slot and the AT-5411 in any ISA slot in your computer. However, for best noise performance, leave as much room as possible between the DAQArb 5411 and other hardware. Before installing your 5411 device, consult your PC user manual or technical reference manual for specific instructions and warnings. Follow these general instructions to install your DAQArb 5411:

1. Write down the DAQArb 5411 serial number on the *DAQArb 5411 Hardware and Software Configuration Form* in Appendix C, *Customer Communication*. You may need this serial number for future reference if you need to contact technical support.
2. Turn off your computer.
3. Remove the top cover or access port to the I/O channel.
4. Remove the expansion slot cover on the back panel of the computer.
5. For the PCI-5411, insert the card into a PCI slot. For the AT-5411, insert the card into a 16-bit ISA slot. It may be a tight fit, but do not force the device into place.
6. Screw the mounting bracket of the DAQArb 5411 to the back panel rail of the computer.
7. Visually verify the installation.

8. Replace the cover.
9. Plug in and turn on your computer.

The PCI-5411 or AT-5411 is now installed.

Hardware Configuration

The DAQArb 5411 is a fully software-configurable, Plug and Play device. Configuration information is stored in nonvolatile memory. The Plug and Play services query the device, read the information, and allocate resources for items such as base address, interrupt level, and DMA channel. After assigning these resources, the operating system enables the device for operation.

Installing the Optional Memory Module

The standard onboard memory for the DAQArb 5411 is 4 MB. You can upgrade to a 16 MB memory module to store large waveform buffers directly on the card. Perform the following steps to install the new memory module:

1. Turn off the computer and remove the top cover or access port to the I/O channel.
2. Unscrew the bracket and remove the DAQArb 5411 from the slot it has been plugged into.
3. Gently place your DAQArb 5411 on a flat surface with the component and memory module side facing up.
4. Unfasten the two screws on the side of the memory module.
5. Gently unplug the memory module from the main board and store the old memory module in an antistatic bag to avoid damage to the components.
6. Properly align the new 16 MB memory module over the connectors and plug it into the connectors.
7. Fasten the two screws you removed in step 4.
8. Follow the regular installation steps described in the *Installation* section earlier in this chapter.

Signal Connections

Chapter 3

This chapter describes the I/O connectors, signal connections, and digital interface to the DAQArb 5411.

I/O Connector

The DAQArb 5411 has four connectors: three SMB connectors and a 50-pin mini-SCSI type connector, as shown in Figure 3-1.

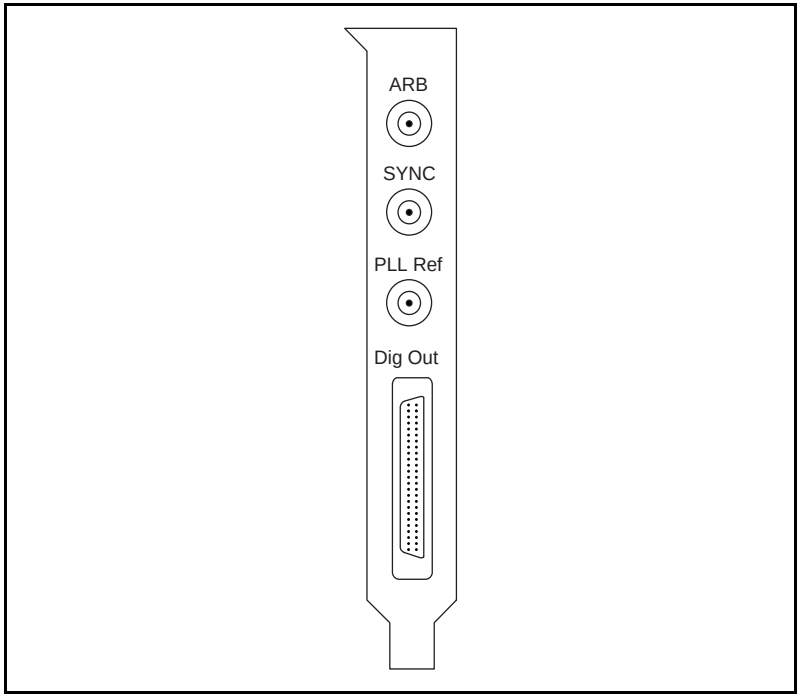


Figure 3-1. DAQArb 5411 I/O Connector

ARB Connector

The ARB connector provides the waveform output. The maximum output levels on this connector depend on the type of load termination. If the output of a DAQArb 5411 terminates into a 50 Ω load, the output levels are ±5 V, as shown in Figure 3-2. If the output of DAQArb 5411 terminates into a high impedance load (HiZ), the output levels are ±10 V. If the output terminates into any other load, the levels are:

$$V_{out} = \pm \frac{R_L}{R_L + R_O} \times 10\ V$$

where V_{out} is the maximum output voltage level, R_L is the load impedance in ohms, and R_O is the output impedance on the DAQArb 5411. By default, R_O = 50 Ω, but the software can also set it to 75 Ω.

☞ **Note:** ***Software will set the voltage output levels based on a 50 Ω load termination.***

For more information on waveform generation and analog output operation, refer to Chapter 4, *Arb Operation*. For specifications on the waveform output signal, see Appendix A, *Specifications*.

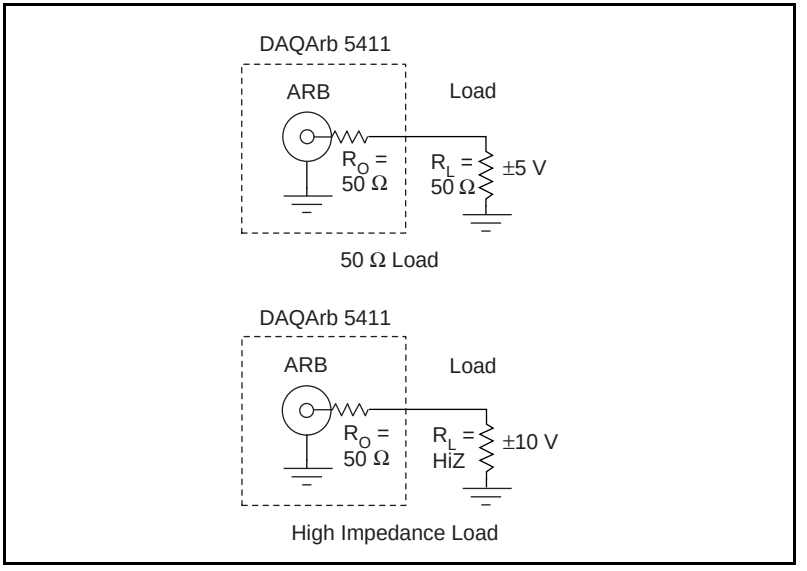


Figure 3-2. Output Levels and Load Termination Using a 50 Ω Output Impedance

SYNC Connector

The SYNC connector is a transistor-transistor-logic (TTL) version of the sine waveform being generated at the output. You can think of the SYNC output as a very high frequency resolution, software-programmable clock source for many applications. You can also vary the duty cycle of SYNC output on the fly by software control, as shown in Figure 3-3. t_p is the time period of the sine wave being generated and t_w is the pulse width of the SYNC output. The duty cycle is $(t_w/t_{p)}$ x 100%.

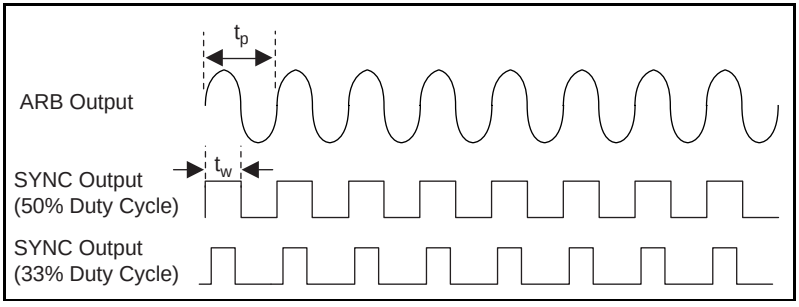


Figure 3-3. SYNC Output and Duty Cycle

You can route the SYNC output to the RTSI lines over the RTSI bus. The SYNC output is derived from a comparator connected to the analog waveform and is intended to be used when the waveform is a sine function. The SYNC output will provide a meaningful waveform only when you are generating a sine wave on the ARB output. For more information on SYNC output, see Chapter 4, *Arb Operation*.

PLL Ref Connector

The PLL Ref connector is a phase-locked loop (PLL) input connector that can accept a reference clock from an external source and phase lock the DAQArb internal clock to this external clock. The reference clock should not deviate more than ±100 ppm of its nominal frequency. The minimum amplitude levels of 1 V_{pp} are required on this clock. You can lock reference clock frequencies of 1 MHz and 5–20 MHz in 1 MHz steps.

☞ **Note:** ***You can also lock the DAQArb 5411 to other National Instruments cards over the RTSI bus using the 20 MHz RTSI clock signal.***

If no external reference clock is available, the DAQArb 5411 will automatically tune the internal clock to the best accuracy possible. For more information on PLL operation, refer to Chapter 4, *Arb Operation*.

Dig Out Connector

Dig Out is a 16-bit digital I/O connector that contains the 16-bit digital pattern outputs, digital pattern clock output, marker output, external trigger input, and power output.

Connector Pin Assignments

Figure 3-4 shows the DAQArb 5411 50-pin digital connector.

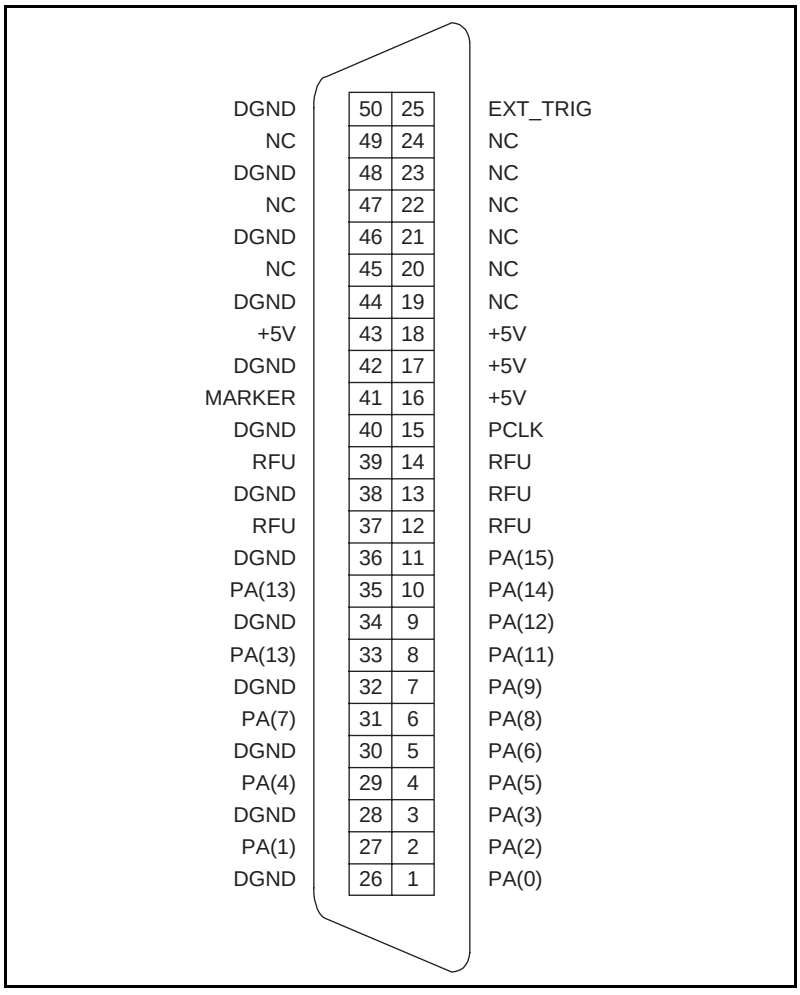


Figure 3-4. DAQArb 5411 50-Pin Digital Output Connector Pin Assignments

Signal Descriptions

Table 3-1 gives the pin names and signal descriptions used on the DAQArb 5411 digital output connector.

Table 3-1. Digital Output Connector Signal Descriptions

Signal Name	Type	Description
DGND	–	Digital ground
EXT_TRIG	Input	External trigger—The external trigger input signal is a TTL-level signal that you can use to start or step through a waveform generation. For more information on trigger sources and trigger mode, see Chapter 4, *Arb Operation*.
MARKER	Output	Marker—A marker is a TTL-level output signal that you can set up at any point in the waveform being generated. You can use this signal to synchronize or trigger other devices at a certain time within waveform generation.
NC	–	Not connected.
PA<0..15>	Output	Digital pattern generator—The 16-bit digital representation of the analog waveform is available as digital pattern outputs along with the clock to which it is synchronized. This data is available directly from the memory after some sample clocks pipeline delay. The digital pattern outputs are available as TTL output levels.
PCLK	Output	Digital pattern clock—The digital pattern clock output synchronizes the digital pattern output. This data is available directly from the memory after some sample clocks pipeline delay. The clock output is available as a TTL output level.
RFU	–	Reserved for future use. Do not connect signals to this pin.
+5V	Output	+5 V power—A +5 V output signal is available on the DAQArb to power external devices. The maximum current you can draw is 100 mA.

SHC50-68 50-Pin Cable Connector

You can use an optional SHC50-68 50-pin to 68-pin cable for pattern generator output. The cable connects to the digital output connector on the DAQArb 5411. Figure 3-5 shows the 68-pin connector pin assignments on the SHC50-68 cable.

☞ **Note:** ***The SHC50-68 connector uses the same signals as the DAQArb 5411 digital output connector, shown in Table 3-1.***

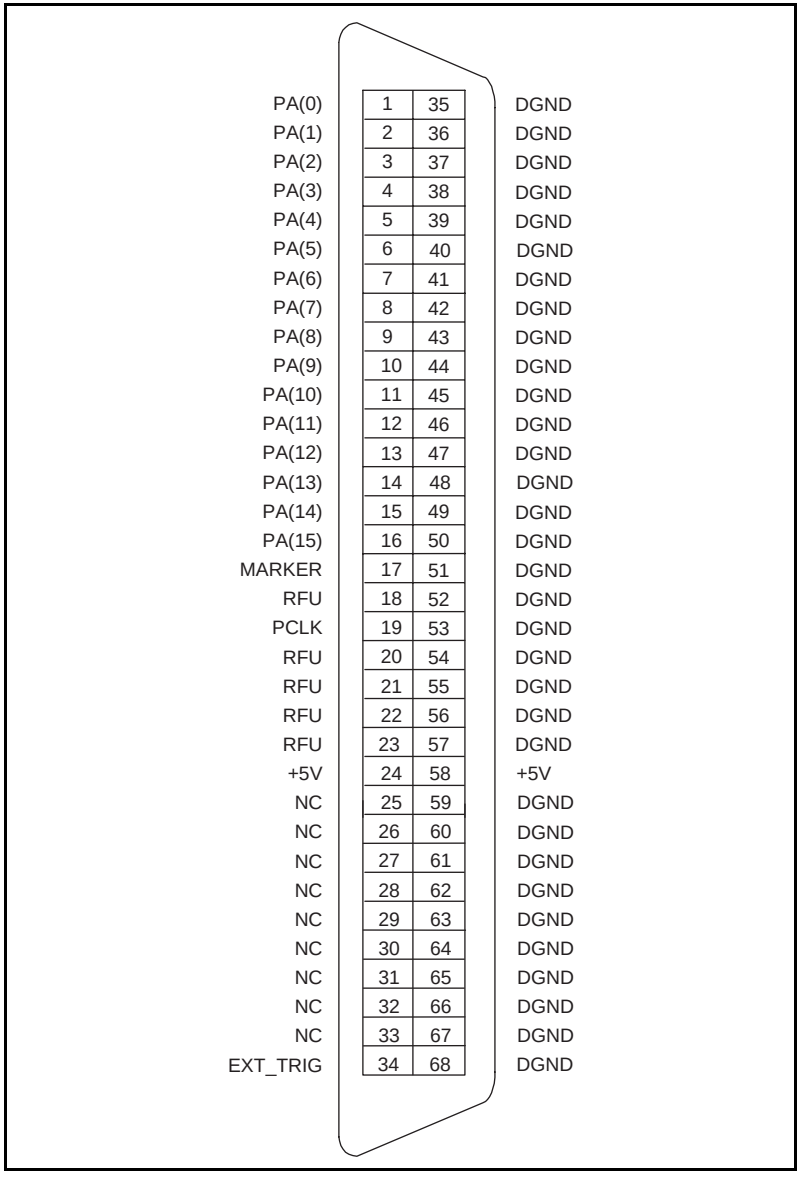


Figure 3-5. SHC50-68 68-Pin Connector Pin Assignments

Power-Up and Reset Conditions

When you power-up your computer, the DAQArb 5411 is in the following state:

- Output is disabled and set to 0 V
- Sample clock is set to 40 MHz
- Trigger mode is set to continuous
- Trigger source is set to automatic (the software provides the triggers)
- Digital filter is enabled
- Output attenuation remains unchanged from previous setting
- Analog filter remains unchanged from previous setting
- Output impedance remains unchanged from previous setting
- Digital pattern generation is disabled

When you reset the board using NI-DAQ or any application software calling NI-DAQ, your DAQArb is in the following state:

- Output is disabled and set to 0 V
- Sample clock is set to 40 MHz
- Trigger mode is set to continuous
- Trigger source is set to automatic (the software provides the triggers)
- Digital filter is enabled
- Output attenuation is set to 0 dB
- Analog filter is enabled
- Output impedance is set to 50 Ω
- Digital pattern generation is disabled
- PLL reference frequency is set to 20 MHz
- PLL reference source is set to internal tuning
- RTSI clock source is disabled
- SYNC duty cycle is set to 50%

Chapter 4

Arb Operation

This chapter describes how to use your DAQArb 5411.

Figure 4-1 shows the DAQArb 5411 block diagram.

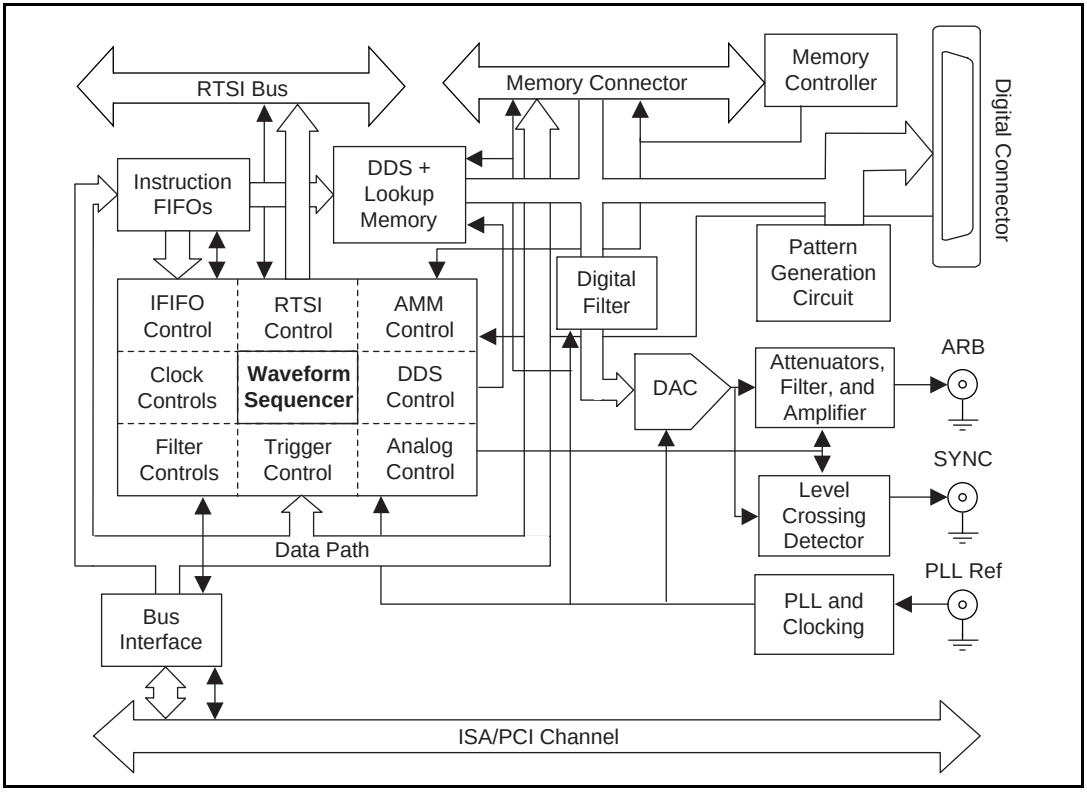


Figure 4-1. DAQArb 5411 Block Diagram

The DAQArb 5411 consists of a bus interface that communicates with the ISA bus for the AT-5411 or the PCI bus for the PCI-5411. The bus interface block handles Plug and Play protocols for assigning resources to the device and providing drivers for the data and address bus that are local to the device. The waveform sequencer performs multiple

functions such as arbitrating the data buses and controlling the triggers, filters, attenuators, clocks, PLL, RTSI switch, instruction FIFO, and direct digital synthesizer (DDS). The memory controller controls the waveform memory on the memory module. The data from the memory is fed to a digital to analog converter (DAC) through a half-band interpolating digital filter. The output from the DAC goes through the filter, amplifiers, attenuators and, finally, to the I/O connector.

Waveform Generation

The DAQArb 5411 can generate waveforms in two modes: Arb and DDS. Use Arb mode for any arbitrary waveform generation, but you can use DDS mode for standard frequency generation such as sine, TTL, square, and triangular waveforms.

In Arb mode, you can define waveforms as multiple buffers. You can *link and loop* these buffers in any order you desire. This mode has more features and is more flexible than DDS mode.

☞ **Note:** ***If you use Virtual Bench software, you must use VirtualBench-Arb for Arb mode.***

DDS mode is more suitable for generating standard waveforms that are repetitive in nature, for example, sine, TTL, square, and triangular waveforms. In DDS mode, you are limited to one buffer, and the buffer size must be exactly equal to 16,384 samples.

☞ **Note:** ***If you use VirtualBench software, you must use VirtualBench-Function Generator for DDS mode.***

Figure 4-2 shows a block diagram representation of the data path for waveform generation. The data for waveform generation can come from either the waveform memory module or DDS lookup memory, depending on the mode of waveform generation. This data is interpolated by a half-band digital filter and then fed to a high-speed DAC. The data has a pipeline delay of 26 update clocks through this digital filter.

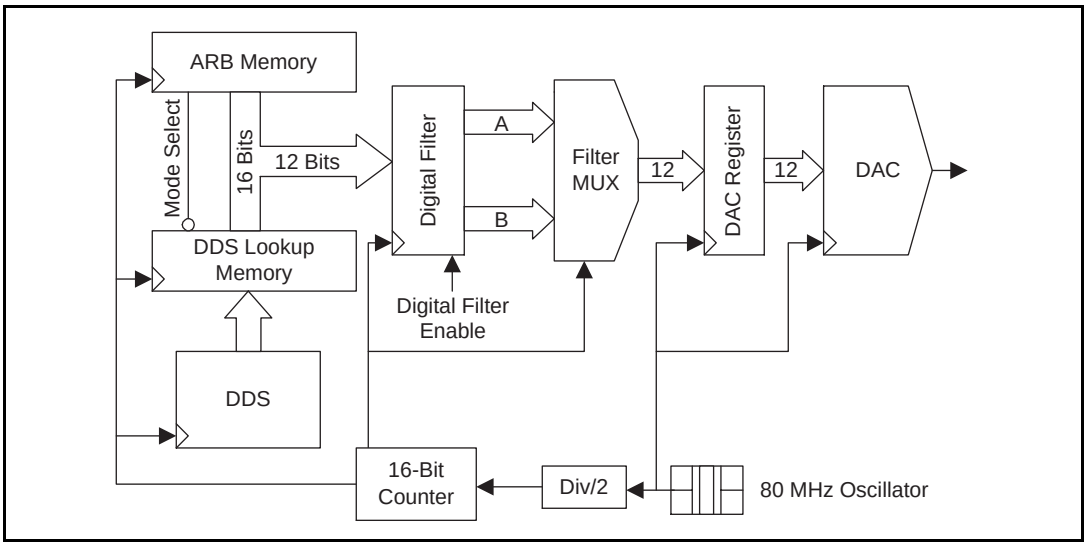


Figure 4-2. Waveform Data Path Block Diagram

Update Rate

On the DAQArb 5411, the high-speed DAC itself is always updated at 80 MHz but the maximum update clock for waveform memory is 40 MHz. The update clock for the waveform memory can be further divided by a 16-bit counter, as shown in Figure 4-2. Therefore, the slowest update rate is 40 MHz divided by 65,536, which is 610.35 Hz.

☞ **Note:** ***For DDS mode, you should always keep the update rate at 40 MHz. Doing this will yield the best performance of the combination of DDS, digital filter, DAC, and analog filter.***

Arb Mode

The Arb mode of waveform generation uses a separate *waveform memory* for storing multiple waveform buffers. This mode also uses a FIFO memory for storing the *staging list,* which contains the buffer linking and looping information. This FIFO is referred to as an *instruction FIFO*.

Waveform Size and Resolution

The DAQArb 5411 stores arbitrary waveforms in memory as 16-bit digital words. Only the 12 most significant bits are sent to the digital filter and the DAC. The following sections describe the waveform memory, the sizes available, and minimum buffer size.

Waveform Memory

The DAQArb 5411 uses a waveform memory16 bits wide. The standard memory size is 2,000,000 samples. This large memory means you can store very long waveforms on the board itself and obtain reliable waveform generation even at full speed. You can upgrade to an 8 million-sample waveform memory by installing the optional 16 MB memory module. See Chapter 2, *Installation and Configuration*, for more information on the memory module.

As shown in Figure 4-3, a 2,000,000-sample waveform memory is organized as eight banks of 256 k by 16-bit memory chips. These eight banks are then shifted serially to achieve a single data stream of 16-bit words at 40 MHz.

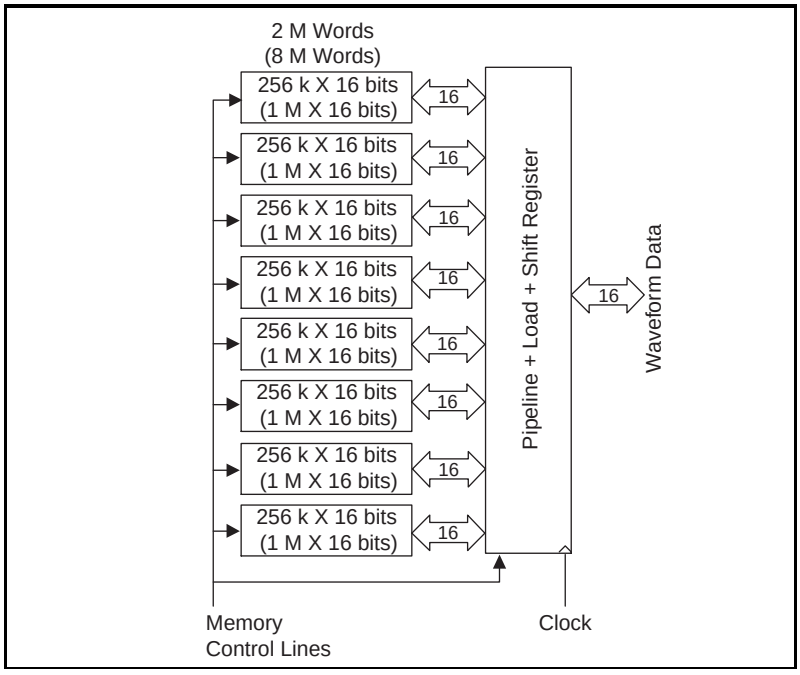


Figure 4-3. Waveform Memory Architecture

Minimum Buffer Size and Resolution

The 5411 device memory architecture imposes certain restrictions on the buffer size and resolution. The minimum buffer size for Arb mode is 256 samples and the buffers must be in multiples of eight samples.

For example, if you request the DAQArb to load a buffer of 257 samples, NI-DAQ will truncate the buffer to 256 samples. The last sample will not be loaded into the memory.

☞ **Note:** ***If the minimum buffer size of 256 samples is not met, NI-DAQ will return an error.***

☞ **Note:** ***If the buffer is not a multiple of eight samples, NI-DAQ will return a warning and truncate the buffer to the nearest multiple of eight samples.***

Waveform Linking and Looping

Before you can start generating waveforms, you have to load the buffers on your DAQArb 5411. Each signal to be generated loads into the memory in the form of 16-bit digital samples. A finite number of these samples makes a waveform *buffer*, sometimes also referred to as a waveform *segment*. You can load multiple buffers in the memory on DAQArb 5411. To generate these buffers, you have to prepare a *staging list*, also known as a *sequence list*, which contains a sequence of *stages*. Each stage specifies the buffer to be generated, the number of loops on that buffer, and the marker position for that buffer.

Figure 4-4 illustrates the concept of waveform samples, buffer, stage, staging list, and looping and linking. Waveform sample A shows the concept of waveform samples used to create a waveform, shown in waveform buffer 1. In this example, the waveform buffer 1 represents a single cycle of a sine wave and the waveform samples in sample A are 16-bit samples. Waveform stage 1 shows a stage created from buffer 1. Stage 1 is buffer 1 with three cycle iterations.

Waveform sample B shows samples for waveform buffer 2, which represents a triangular waveform. Waveform stage 2 is created using two iterations of buffer 2.

Stage 3 is created using a single iteration of buffer 1. These waveforms are linked in a sequence, as shown in Figure 4-4. The concept of using a staging list to generate waveforms is referred to as *waveform linking and looping* or *waveform staging*.

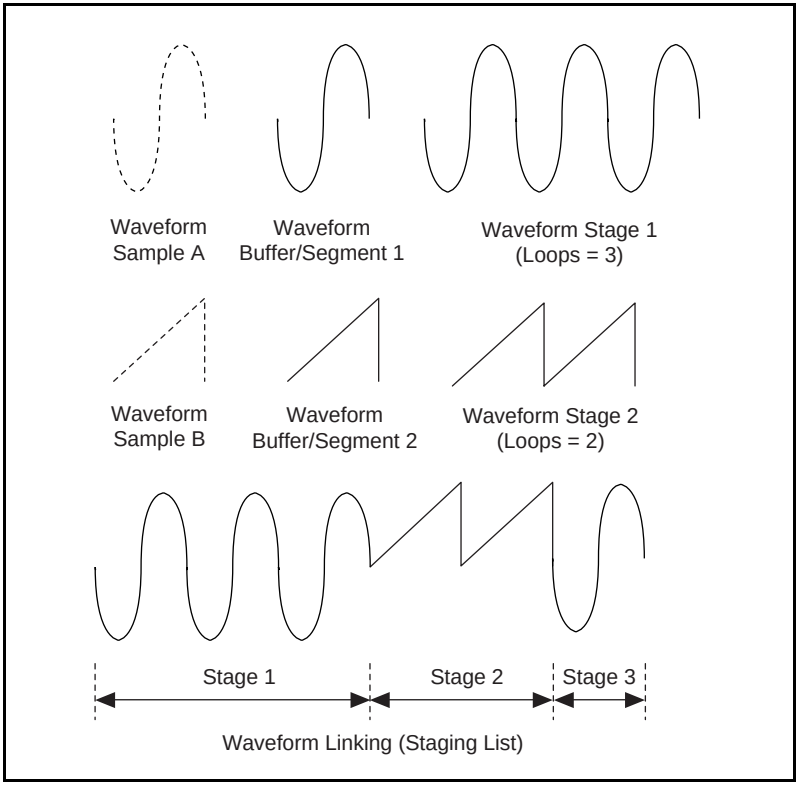


Figure 4-4. Waveform Linking and Looping

Waveform Staging

Figure 4-5 shows waveform staging in hardware. The instruction FIFO contains the staging list, which the DAQArb 5411 sequencer reads for waveform generation.

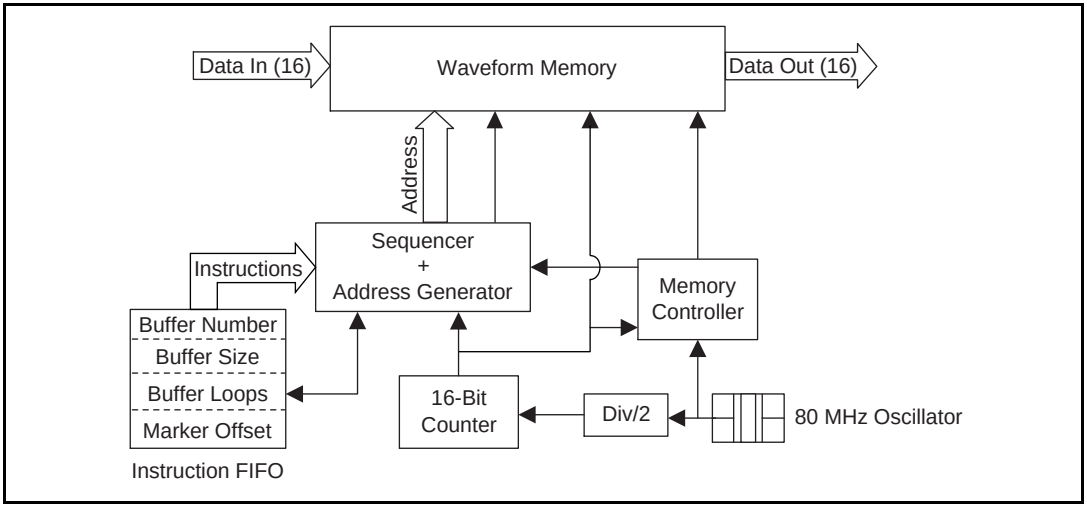


Figure 4-5. Waveform Staging Block Diagram

Each stage is made up of four instructions:

- *Buffer number*—Specifies the buffer number to be generated.
- *Buffer size*—Specifies the total count of the buffer to be generated. This count may be more or less than the actual size of that buffer. If the count is less, only a part of that buffer will be used for that stage. If the count is more than the actual size of that buffer, part of the next sequential buffer will also be used. If the buffer size is set to zero, the software will automatically use the true size of that buffer.
- *Buffer loops*—Specifies the number of times that buffer has to be looped. The maximum number of loops possible is 65,535.
- *Marker offset*—Specifies where the marker has to be generated within that buffer. For more information on markers, see the *Markers* section later in this chapter.

☞ **Note:** ***The maximum number of waveform stages the instruction FIFO can store for Arb mode is 290.***

☞ **Note:** ***For more information on the waveform generation process, refer to your software manuals.***

Figure 4-6 shows a simple case of waveform generation process.

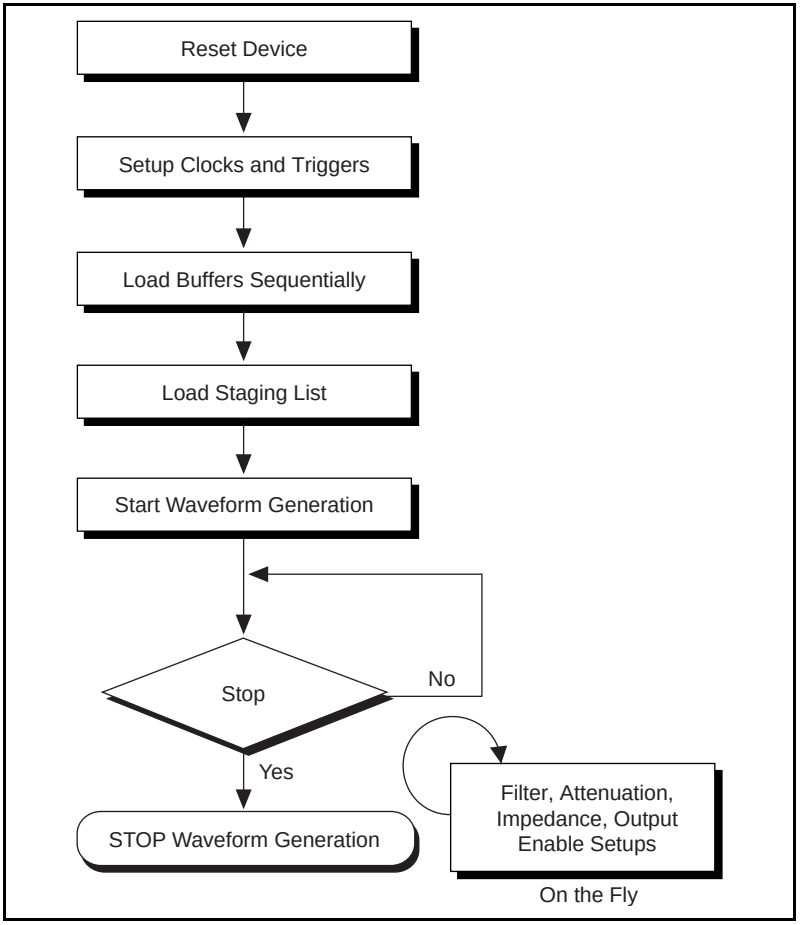


Figure 4-6. Waveform Generation Process

Direct Digital Synthesis (DDS) Mode

Direct digital synthesis (DDS) is a technique for deriving, under digital control, an analog frequency source from a single reference clock frequency. This technique provides high-frequency accuracy and resolution, temperature stability, wideband tuning, and very fast and phase-continuous frequency switching.

The DAQArb 5411 uses a 32-bit, high-speed accumulator with a lookup memory and a 12-bit DAC for DDS-based waveform generation. Figure 4-7 shows the building blocks for DDS-based waveform generation.

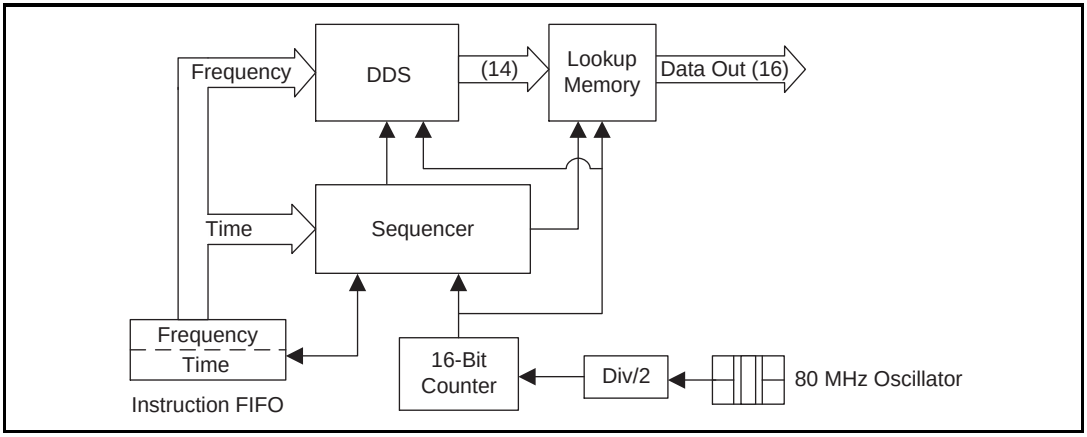


Figure 4-7. DDS Building Blocks

The lookup memory is dedicated to the DDS mode only and cannot be used in Arb mode. You can store one cycle of a repetitive waveform—a sine wave, a triangular wave, a square wave, or an arbitrary wave—in the lookup memory. Then, you can change the frequency of that waveform by sending just one instruction. You can use DDS mode for very fine frequency resolution function generation. You can generate sine waves of up to 16 MHz with a frequency resolution of 10.0 mHz. Because this mode uses an accumulator, waveform generation loops back to the beginning of the lookup memory after passing through the end of the lookup memory.

You should use DDS mode for standard function generation rather than for arbitrary waveform generation.

In this mode, each stage is made up of two instructions: the *frequency*, which specifies the frequency of the waveform to be generated, and *time*, which specifies the time for which the frequency has to be generated.

Frequency Resolution and Lookup Memory

For DDS-based waveform generation, you must first load one cycle of the desired waveform into the lookup memory. The size of the DDS lookup memory is 16,384 samples. Each sample is 16 bits wide.

☞ **Note:** ***One cycle of the waveform buffer loaded into the memory should be exactly equal to the size of the DDS lookup memory.***

F_c = update clock for the accumulator

Set the DAQArb 5411 at F_c = 40 MHz.

F_a = desired frequency of the output signal

N = accumulator size in bits

Set the DAQArb 5411 at N = 32.

FCW = frequency control word to be loaded into the accumulator to generate F_a.

This is calculated using the formula:

$FCW = (2^N * F_a) / F_c$

The frequency resolution is then given by:

frequency resolution = $F_c / 2^N = (40 \times 10^6) / 2^{32}$ = 9.31322 mHz

For example, if you need to generate a frequency of 10 MHz, then the FCW is $(2^{32} * 10E6)/40E6$, which equals 1,073,741,824. If you need to generate a frequency of 1 Hz, then the FCW is $(2^{32} * 1)/40E6$, which equals 107.

☞ **Note:** ***On the DAQArb 5411, the maximum frequency of a sine wave you can generate reliably is limited to 16 MHz. Other waveforms like square or triangular waves are limited to 1 MHz.***

You can also synthesize arbitrary waveforms using DDS. Generating arbitrary waveforms this way will be very limited; you are restricted to a single buffer, and this buffer should be exactly equal to the size of the lookup memory.

To update every next sample of an arbitrary waveform in lookup memory at the maximum clock rate of 40 MHz, write an FCW value of $2^{(N-L)}$, where N is the size of the accumulator and L is the number of address bits of lookup memory (L = 14 bits for the AT-5411 and the PCI-5411). Thus, the FCW value for the DAQArb 5411 equals 262,144.

If you want to update every next sample in lookup memory at an integral subdivision, D, of the maximum clock rate, you should write an FCW value of $2^{(N-L-D+1)}$. In other words, for an effective update rate of every sample at half the maximum clock rate, you should write an FCW value of $2^{(32-14-2+1)}$, which equals 131,072.

Frequency Hopping and Sweeping

You can define a staging list in DDS mode for performing *frequency hops and sweeps*. The entire staging list uses the same buffer loaded into the lookup memory. All stages differ in the frequency to be generated. As shown in Figure 4-7, a stage in DDS mode has a different instruction set than Arb mode.

☞ **Note:** ***The minimum time that a frequency should be generated is at least 2 µs. Therefore, the maximum hop rate from one frequency to the other frequency is limited to 500 kHz.***

☞ **Note:** ***The maximum number of stages that can be stored in the instruction FIFO for DDS mode is equal to 340. For more information on the waveform generation process, refer to your software manuals.***

Triggering

Triggering is a feature by which you can start and step through a waveform generation. The trigger sources and trigger modes are explained in the sections below.

Trigger Sources

Trigger sources are software selectable. By default, the software provides the triggers. You can use also use an external trigger from a pin on the digital I/O connector or from any of the RTSI trigger lines on the RTSI bus. Figure 4-8 shows the trigger sources for the DAQArb 5411.

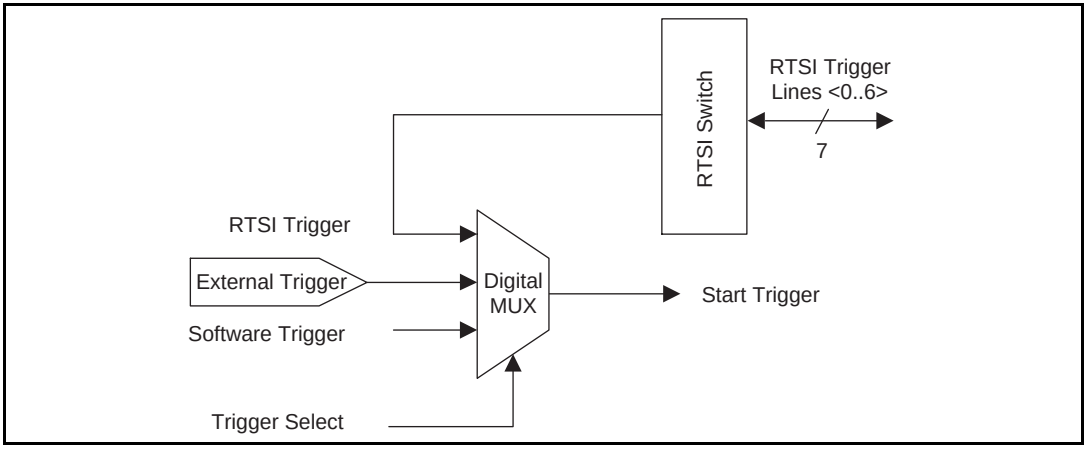


Figure 4-8. Waveform Generation Trigger Sources

If you need to automatically trigger the waveform generation, use software to generate the triggers. A rising TTL edge is required for external triggering. For more information on triggering over RTSI lines, see the *RTSI Trigger Lines* section later in this chapter.

Modes of Operation

DAQArb 5411 functionality is further enhanced by various triggering modes available on it. The available trigger modes are single, continuous, stepped, and burst. These trigger modes are available for both arb and DDS modes.

Single Trigger Mode

The waveform you describe in the sequence list is generated only once by going through the entire staging list. Only one trigger is required to start the waveform generation.

You can use single trigger mode with the both the Arb and DDS waveform generation modes, as follows:

- Arb mode—Figure 4-9 uses the stages 1, 2, and 3 shown in Figure 4-4 to illustrate a single trigger mode of operation for Arb waveform generation mode. After the DAQArb 5411 receives a trigger, the waveform generation starts from the first stage and continues through to the last stage. The last stage is generated repeatedly until you stop the waveform generation.

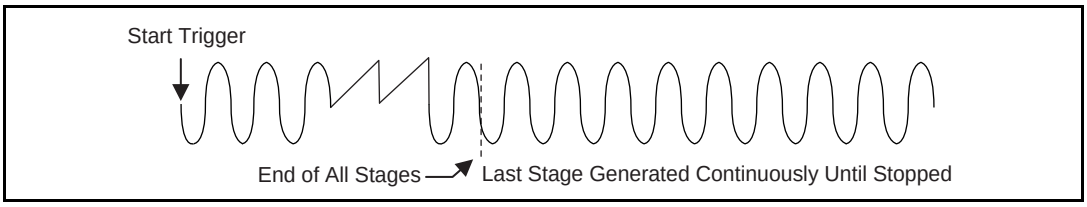


Figure 4-9. Single Trigger Mode for Arb Mode

☞ **Note:** ***You can settle to a predefined state by making the last stage emulate that state.***

- DDS mode—After the DAQArb 5411 receives a trigger, the waveform generation starts from the first stage and continues through to the last stage. The last stage is generated repeatedly until the waveform generation is stopped. Figure 4-10 illustrates a single trigger mode of operation for DDS waveform generation mode.

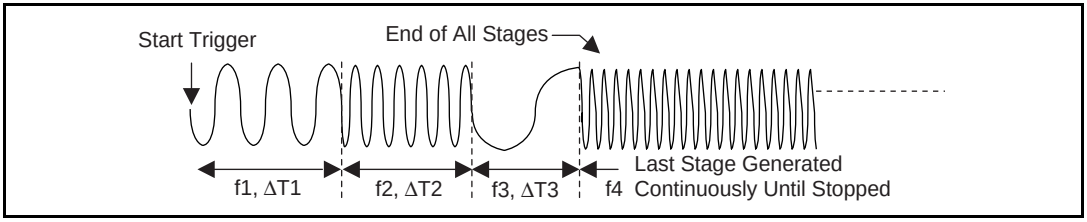


Figure 4-10. Single Trigger Mode for DDS Mode

Assume that one cycle of a sine wave is stored in the DDS lookup memory. For stage 1, f1 specifies the sine frequency to be generated for time ΔT1, f2 and ΔT2 for stage 2, and so on. If there are four stages in the staging list, then f4 will be generated continuously until the waveform generation is stopped.

Continuous Trigger Mode

The waveform you describe in the staging list is generated infinitely by recycling through all the staging list. After a trigger is received, the waveform generation starts from the first stage and continues through to the last stage. After the last stage is completed, the waveform generation loops back to the start of the first stage and continues until it is stopped. Only one trigger is required to start the waveform generation.

You can use continuous trigger mode with the both the Arb and DDS waveform generation modes, as follows:

- Arb mode—Figure 4-11 uses the stages shown in Figure 4-4 to illustrate a continuous trigger mode of operation for Arb waveform generation mode.

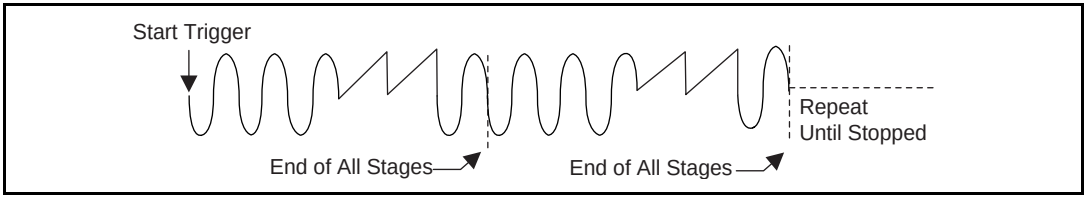


Figure 4-11. Continuous Trigger Mode for Arb Mode

- DDS mode—Figure 4-12 illustrates a continuous trigger mode of operation for DDS waveform generation mode.

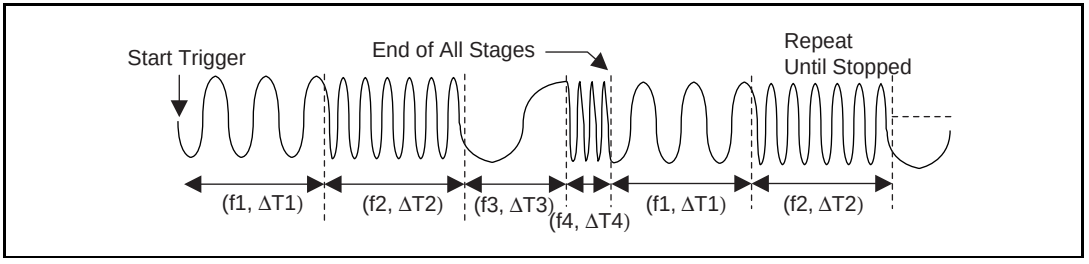


Figure 4-12. Continuous Trigger Mode for DDS Mode

Stepped Trigger Mode

After a start trigger is received, the waveform described by the first stage is generated. Then, the device waits for the next trigger signal. On the next trigger, the waveform described by the second stage is generated, and so on. Once the staging list is exhausted, the waveform generation returns to the first stage and continues in a cyclic fashion.

You can use the stepped trigger mode with the both the Arb and DDS waveform generation modes, as follows:

- Arb mode—Figure 4-13 uses the stages shown in Figure 4-4 to illustrate a stepped trigger mode of operation for the Arb mode. If a trigger is received while a stage is being generated, it will be ignored. A trigger will be recognized only after the stage has been completely generated.

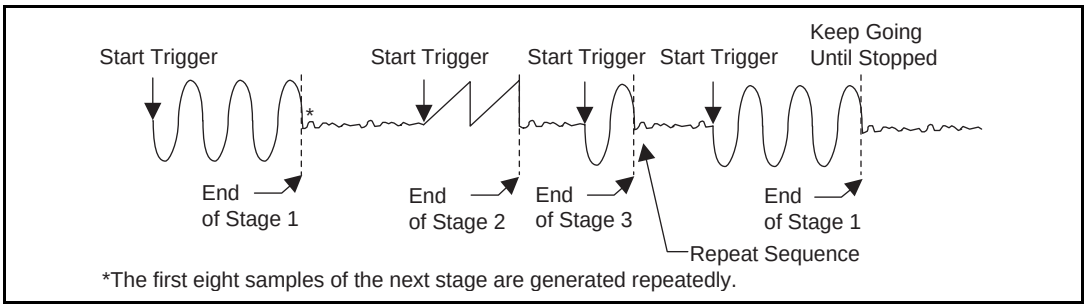


Figure 4-13. Stepped Trigger Mode for Arb Mode

After any stage has been generated completely, the first eight samples of the next stage are repeated continuously until the next trigger is received.

☞ **Note:** ***For stepped trigger mode, you can predefine the state in which a stage ends by making the first eight samples of the next stage represent the state you want to settle.***

- DDS mode—S*tepped trigger mode* and *burst trigger mode* are the same thing for the DDS mode of waveform generation.

Burst Trigger Mode

After a start trigger is received, the waveform described by the first stage is generated until another trigger is received. At the next trigger, the buffer of the previous stage is completed before the waveform described by the second stage is generated. Once the staging list is exhausted, the waveform generation returns to the first stage and continues in a cyclic fashion.

You can use burst trigger mode with the both the Arb and DDS waveform generation modes, as follows:

- Arb mode—Figure 4-14 uses the stages shown in Figure 4-4 to illustrate a burst trigger mode of operation for Arb mode.

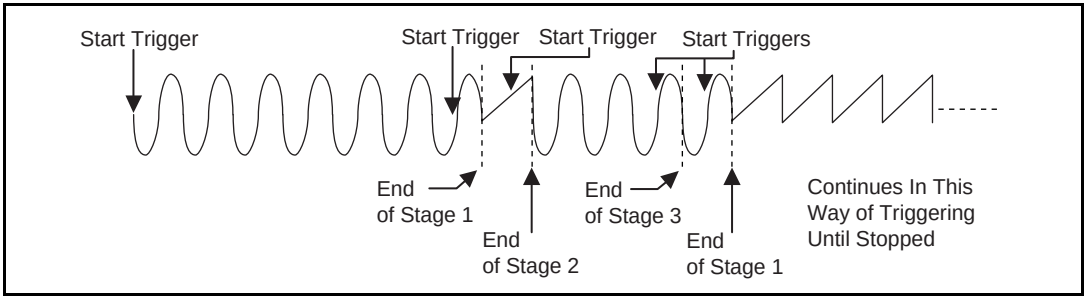


Figure 4-14. Burst Trigger Mode for Arb Mode

- DDS mode—Figure 4-15 illustrates a burst trigger mode of operation for DDS mode. The switching from one stage to the other stage is phase continuous. In this mode the time instruction is not used. The trigger paces the waveform generation from one frequency to the other.

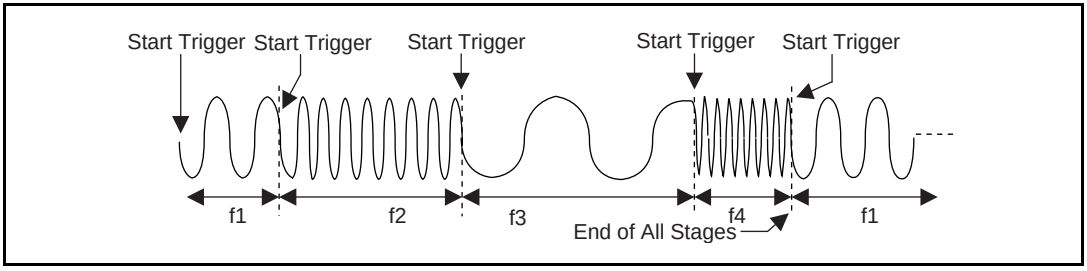


Figure 4-15. Burst Trigger Mode for DDS Mode

Marker Output Signal

A marker is equivalent to a trigger output signal and it is available on a separate pin in the digital I/O connector. You can define this TTL level trigger output signal at any position in the waveform buffer. You can place a marker in every stage; however, only one marker per stage is allowed.

You can specify a marker by giving an offset count (in number of samples) from the start of the waveform buffer specified by the stage. If the offset is out of range of the number of samples in that stage, the marker will not appear at the output. If the buffer is looped multiple times in a stage, the marker will be generated that many times.

☞ **Note:** ***The marker is generated for eight update clocks and the placement resolution of the marker is ±4 samples.***

If you want a marker at an offset of zero from the start of the waveform buffer, the marker will be eight samples long beginning with the first sample. A marker at an offset of seven from the start of the waveform buffer also will be eight samples long beginning with the first sample, as shown in Table 4-1. A marker at an offset of eight will be generated at positions 8–15.

Table 4-1. Generated Marker Positions

Sample Number	Marker Requested	Marker Generated
1	At sample 0 from the beginning of the buffer	Sample position 0–7
2	At sample 1 from the beginning of the buffer	Sample position 0–7
3	At sample 7 from the beginning of the buffer	Sample position 0–7
4	At sample 8 from the beginning of the buffer	Sample position 8–15
5	At sample 255 from the beginning of the buffer	Sample position 248–255

Figure 4-16 shows an analog waveform being generated at one connector and a marker being generated at another I/O connector. Point A shows a marker generated for requested positions 0–7, and point B shows requested positions of 8–15.

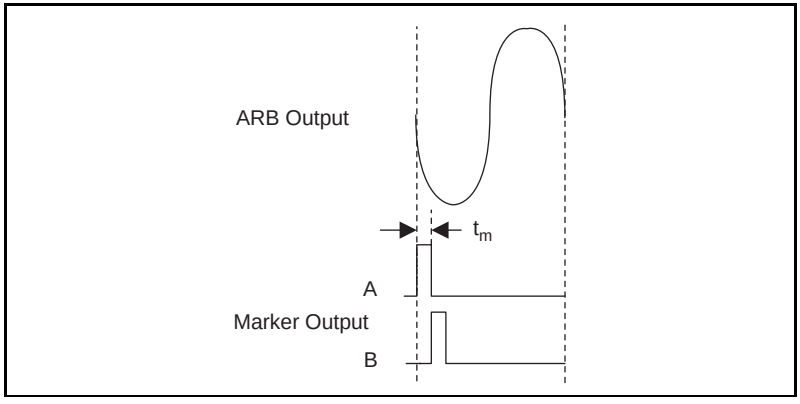


Figure 4-16. Markers as Trigger Outputs

☞ **Note:** ***Marker output signals are an important feature to trigger other instruments or devices at a specified time while a waveform generation is in progress.***

Analog Output

Figure 4-17 shows the essential blocks of analog waveform generation. The 12-bit digital waveform data is fed to a high-speed DAC. A low-pass filter filters the DAC output. This filtered signal is pre-amplified before it goes to a 10 dB attenuator. The DAC output can be fine-tuned for gain and offset. Since the offset is adjusted before the main attenuators and amplifier, it is referred to as *pre-attenuation offset*. This fine-tuning of gain and offset is done using separate DACs. The output from the 10 dB attenuator is then fed to the main amplifier, which can provide ±5 V levels into 50 Ω. An output relay can switch between ground level and the main amplifier. The output of this relay is fed to a series of passive attenuators. The output of the attenuators is fed through a selectable output impedance of 50 or 75 Ω to the I/O connector.

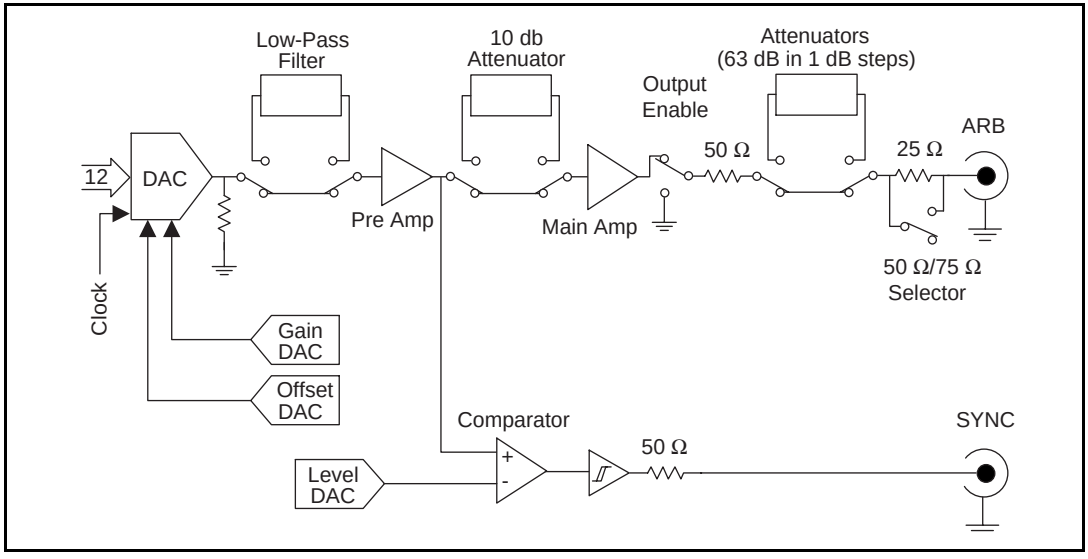


Figure 4-17. Analog Output and SYNC Out Block Diagram

Figure 4-18 shows the timing relationships of the trigger input, waveform output, and marker output. T_{d1} is the pulse width on the trigger signal. T_{d2} is the time delay from trigger to output on Arb

output. T_{d3} is the time between the marker output and Arb output. T_{d4} is the pulse width on marker output. Refer to Appendix A, *Specifications,* for more information on these timing parameters.

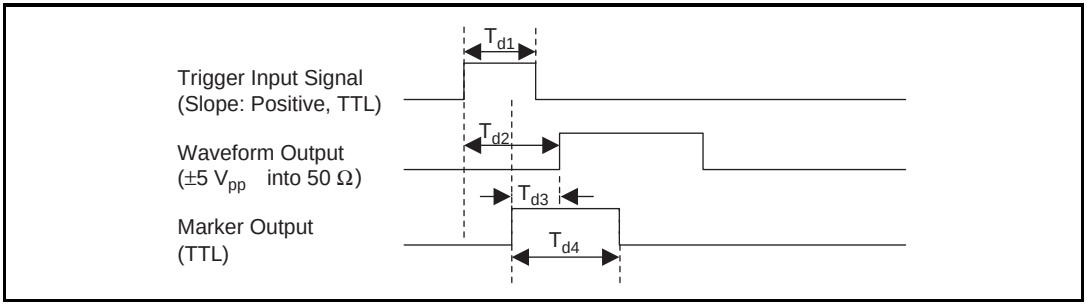


Figure 4-18. Waveform, Trigger, and Marker Timings

☞ **Note:** ***You can switch off the analog low-pass filter at any time during waveform generation.***

SYNC Output and Duty Cycle

The SYNC output is a TTL version of the sine waveform being generated at the output. The signal from the pre-amplifier is sent to a comparator, where it is compared against a level set by the level DAC. The output of this comparator is sent to the SYNC connector through a hysteresis buffer and a 50 Ω series resistor to provide reverse termination of reflected pulses.

You can use the SYNC output as a very high frequency resolution, software-programmable clock source for many applications. You also can vary the duty cycle of SYNC output, on the fly, by changing the output of the *level DAC*. The SYNC output might not carry any meaning for any other types of waveforms being generated.

☞ **Note:** ***You can change the duty cycle of SYNC output at any time during waveform generation.***

Output Attenuation

Figure 4-19 shows the DAQArb 5411 output attenuator chain. The output attenuators are made of resistor networks and may be switched in any combination desired. The maximum attenuation possible on the DAQArb 5411 is 73 dB.

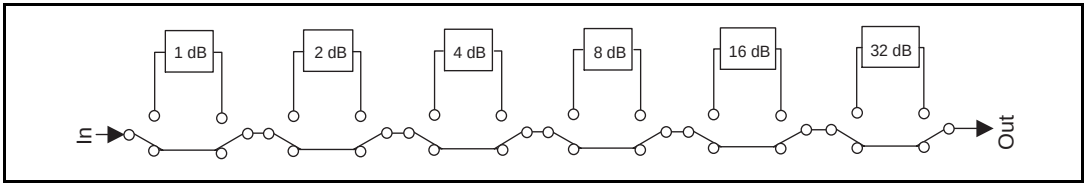


Figure 4-19. Output Attenuation Chain

By attenuating the output signal, you keep the dynamic range of the DAC; that is, you do not lose any bits from the digital representation of the signal because the attenuation is done after the DAC and not before it.

$$\text{attenuation (in decibels)} = -20 \log_{10}(V_o / V_i)$$

where,

V_o = desired voltage level for the output signal

V_i = input voltage level.

☞ **Note:** ***For the DAQArb 5411, V_i = ±5 V for terminated load and ±10 V for unterminated load.***

For example, to change the output level to ±2.5 V into a terminated load, use the following formula:

$$\text{Attenuation} = -20 * \log_{10}(2.5/5) = 6.020 \text{ dB}$$

☞ **Note:** ***You can change the output attenuation at any time during waveform generation.***

Output Impedance

As shown in Figure 4-17, before the signal reaches the output connector, you can select the output impedance to be 50 Ω or 75 Ω. If the load impedance is 50 Ω and all the attenuators are off (that is, an output attenuation of 0 dB), the output levels are ±5 V.

A load impedance of 50 Ω is used for most applications but 75 Ω is required for applications such as testing video devices. If the load is a very high input impedance load (~1 MΩ), you will see output levels up to ±10 V.

☞ **Note:** ***You can change the output impedance at any time during waveform generation.***

Output Enable

You can switch off the waveform generation at the output connector by controlling the output enable relay, as shown in Figure 4-17. When the output enable relay is off, the output signal level goes to ground level.

☞ **Note:** ***Even though the output enable relay is in the off position, the waveform generation process will continue internally on the DAQArb 5411.***

You can use this feature to disconnect and connect different devices, on the fly, to the DAQArb 5411.

☞ **Note:** ***You can change the output enable state at any time during waveform generation.***

Pre-attenuation Offset

Pre-attenuation offset is an offset adjustment to the waveform before the attenuation chain. You can adjust the pre-attenuation offset, provided you have at least 10 dB of attenuation switched in. With a terminated load, you get a ±2.5 V offset adjustment before the attenuation chain.

With less than 10 dB of attenuation switched in, you can also adjust the pre-attenuation offset as much as ±2.5 V (into 50 Ω), provided that the waveform maximum plus offset before attenuation does not exceed ±5 V (into 50 Ω).

☞ **Note:** ***The pre-attenuation offset is also attenuated by the attenuation setting you specify through the software.***

For example, if you have waveform generation into a terminated load with 20 dB attenuation, the output levels are ±0.5 V. If you set up a pre-attenuation offset of +1 V, the actual offset you will see at the output connector is +0.1 V (20 dB of +1 V).

☞ **Note:** ***You can change the pre-attenuation offset at any time during waveform generation.***

Phase-Locked Loops

Figure 4-20 illustrates the block diagram for the DAQArb 5411 PLL circuit. The PLL consists of a voltage controlled crystal oscillator (VCXO) with a tuning range of ±100 ppm. The main clock of 80 MHz is generated by this VCXO. The PLL can lock to a reference clock source from the external connector or a RTSI Osc line on the RTSI bus, or it can be tuned internally using a calibration DAC (CalDAC). This tuning has been done at the factory for the best accuracy possible. The reference clock and the VCXO clock are compared by a phase comparator running at 1 MHz. The error signal is filtered out by the loop filter and sent to the control pin of the VCXO to complete the loop.

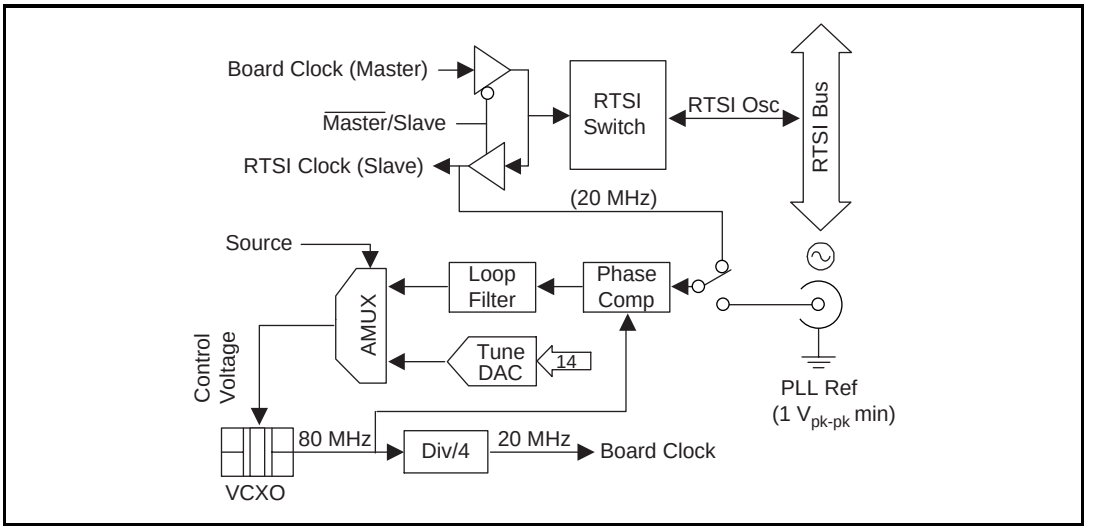


Figure 4-20. Phase-Locked Loop (PLL) Architecture

You can phase lock to an external reference clock source of 1 MHz and from 5–20 MHz in 1 MHz increments. The PLL can lock to a signal level of at least 1 $V_{pk\text{-}pk}$.

Caution: ***Do not increase the voltage level of the clock signal at the PLL reference input connector by more than the specified limit, 5 $V_{pk\text{-}pk}$.***

The VCXO output of 80 MHz is further divided by four, to send a 20 MHz board clock signal to the RTSI bus.

Master/Slave Operation

The DAQArb may be phase locked to other devices or other DAQArb devices in either of two ways, as shown in Figure 4-21. You can use master/slave phase locking to synchronize multiple devices in a test system.

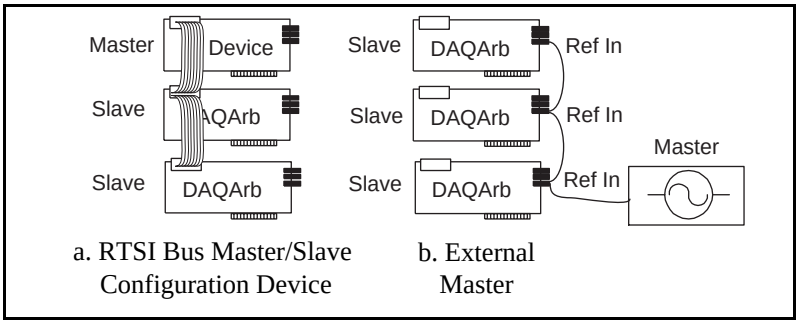


Figure 4-21. Master/Slave Configurations for Phase Locking

Example 1, shown in Figure 4-21a, shows any National Instruments device with RTSI bus capability as the master. To phase lock the DAQArbs to this master, perform the following steps:

1. Set the National Instruments device (master) to send a 20 MHz signal over the RTSI bus on the RTSI Osc line. If this device is a DAQArb, set the source for the RTSI clock line to *board clock* for NI-DAQ software and *internal* for LabVIEW.
2. Set up the slave devices so that the PLL reference source is set to the RTSI clock line.
3. Set the PLL reference frequency parameter to 20 MHz.
4. The boards should now be frequency locked to the master.
5. To further phase lock the boards, set up the master to send the trigger signal on one of the RTSI trigger lines.
6. Set up the slaves to receive their trigger signal on the RTSI bus.
7. Start the waveform generation on all the slaves
8. Start the waveform generation on the master.
9. All the slaves will be triggered by the master and will be phase and frequency locked to each other and the master.

Example 2, shown in Figure 4-21b, shows an external device as the master. To phase lock the DAQArb devices to this master perform the following steps:

1. Set the master device to send any valid reference clock to the PLL reference input connector.
2. Set up the slave devices so that the PLL reference source is set to the I/O connector.
3. Set the PLL reference frequency parameter to the clock frequency sent by the master.
4. The boards should now be frequency locked to the master.
5. To further phase lock the boards, connect the external trigger input to the trigger input of the 50-in digital connectors of all the boards and set up the slaves to receive the triggers on trigger input connector.
6. Start the waveform generation on all the slaves.
7. Activate the external trigger signal. All the slaves are triggered at the same time and get phase and frequency locked.

☞ **Note:** ***If two or more DAQArb devices are running in Arb mode and are locked to each other using the same reference clock, then you will see a maximum phase difference of one sample clock on the locked boards when they are triggered at the same time.***

☞ **Note:** ***If two or more DAQArb devices are running in DDS mode and are locked to each other using the same reference clock, they will be frequency locked, but you will not know the phase relationship.***

Analog Filter Correction

The DAQArb 5411 can correct for slight deviations in the flatness of the frequency characteristic of the analog low-pass filter in its passband, as shown in Figure 4-22. Curve A shows a typical low-pass filter curve. The response of the filter is stored in an onboard EEPROM in 1 MHz increments up to 16 MHz. Curve C is the correction applied to the frequency response. The resulting Curve B is a flat response over the entire passband. If you want to generate a particular frequency with filter correction applied, you have to specify that frequency through software.

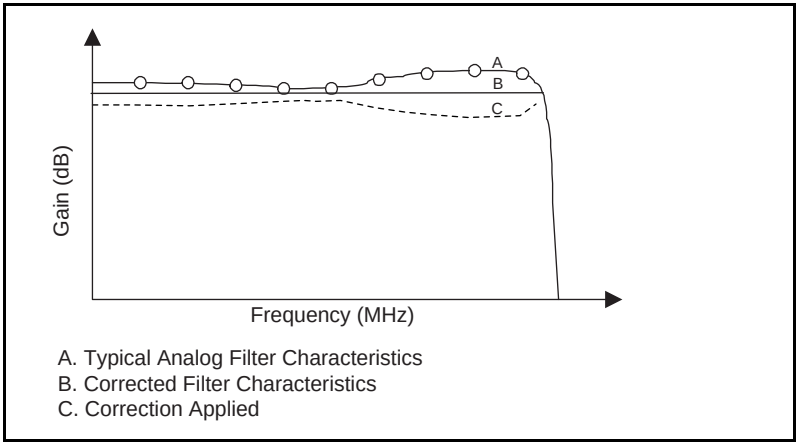


Figure 4-22. Analog Filter Correction

☞ **Note:** ***You can change the filter frequency correction at any time during waveform generation.***

Digital Pattern Generation

The DAQArb 5411 provides 16-bit digital pattern generation outputs at the digital connector. This digital data is first synchronized to the sample clock and then buffered and sent to the connector through a 80 Ω series resistor. The sample clock is also buffered and sent to the digital connector to latch the data externally. Figure 4-23 shows the data path for digital pattern generation. The digital pattern data is available directly from the memory; it does not go through the digital filter.

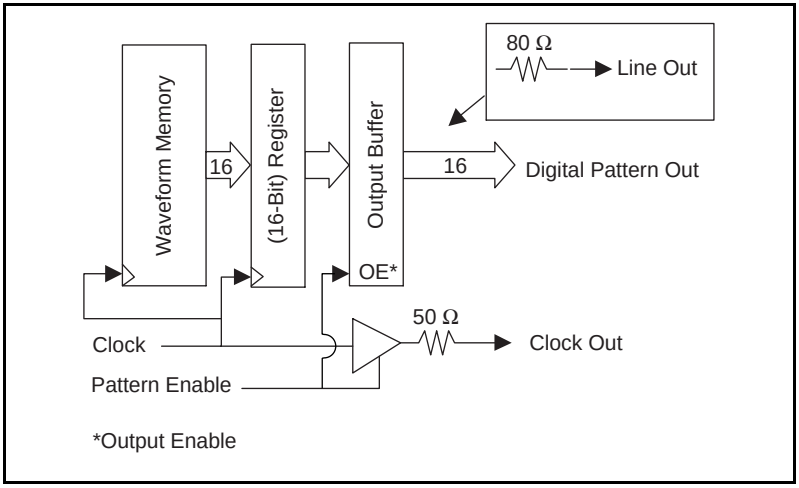


Figure 4-23. Digital Pattern Generator Data Path

You can enable or disable digital pattern generation through software. All linking and looping capabilities are available for digital pattern generation, as well. If you select DDS mode, the DDS data appears at the digital I/O connector.

You can use digital pattern generation to test digital devices such as serial and parallel DACs and to emulate protocols.

☞ **Note:** ***At computer power-up and reset, pattern generation is disabled.***

Figure 4-24 shows the timing waveforms for digital pattern generation; t_{clk} is the clock time period and t_{co} is time delay from clock to output on pattern lines, such as PA <0..15>. Refer to the Appendix A, *Specifications*, for these timing parameters.

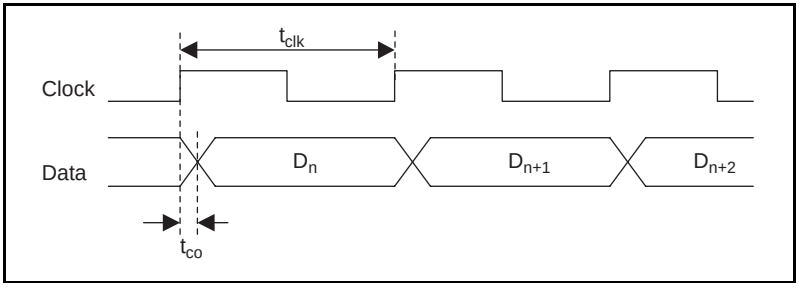


Figure 4-24. Digital Pattern Generation Timing

The sample clock for integral subdivisions of 40 MHz will always have a high pulse width of 25 ns. If the t_{co} time is insufficient for the hold time of your device, then you can use the falling edge of the sample clock output (PCLK) to register the digital pattern data.

RTSI Trigger Lines

The DAQArb 5411 contains seven trigger lines and one RTSI clock line available over the RTSI bus to send and receive DAQArb 5411-specific information to other boards having RTSI connectors. Figure 4-25 shows the RTSI trigger lines and routing of DAQArb 5411 signals to the RTSI switch.

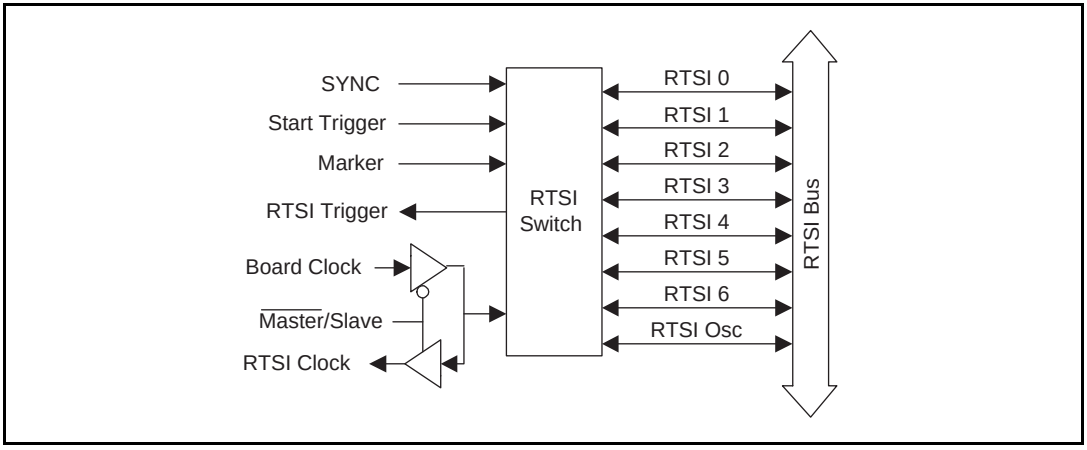


Figure 4-25. DAQArb 5411 RTSI Trigger Lines and Routing

For phase locking to other boards as a master, the 5411 sends an onboard 20 MHz signal to the RTSI Osc line as a Board Clock signal. For locking to other devices as a slave, the DAQArb 5411 receives the RTSI Osc line as a RTSI Clock signal.

The DAQArb 5411 can receive a hardware trigger from another board as a RTSI trigger signal on any of the RTSI trigger lines, RTSI <0.. 6>.

The marker generated during waveform generation in Arb mode can be routed to any of the RTSI bus trigger lines.

The trigger generated on the DAQArb 5411 can be routed to other boards through any of the RTSI bus trigger lines.

The SYNC output generated on the DAQArb 5411 can be routed to other boards through any of the RTSI bus trigger lines.You can use this signal to provide other boards with an accurate and fine frequency resolution clock.

☞ **Note:** ***Refer to your software manual for selecting and routing signals to the RTSI bus.***

Calibration

Calibration is the process of minimizing measurement errors by making small circuit adjustments. On the DAQArb 5411, NI-DAQ automatically makes these adjustments by retrieving predetermined constants from the onboard EEPROM, calculating correction values, and writing those values to the CalDACs.

All DAQArb 5411 devices are factory calibrated to the levels indicated in Appendix A, *Specifications*. Factory calibration involves procedures such as nulling the offset and gain errors, all at room temperature (25^{o} C). The calibration constants are stored in a write-protected area in the EEPROM. Factory calibration may not be sufficient for some applications where different environmental conditions and aging could induce inaccuracy. Contact National Instruments to recalibrate your DAQArb 5411.

Specifications

Appendix A

This appendix lists the specifications of the DAQArb 5411. These specifications are typical at 25° C unless otherwise stated. The operating temperature range is 0° to 50° C.

Analog Output

Number of channels 1

Resolution.....12 bits

Maximum update rate .....40 MHz

DDS accumulator.....32 bits

Frequency range
- Arb.....40 MS/s
- Sine.....16 MHz, max
- SYNC (TTL).....16 MHz, max
- Square .....1 MHz
- Ramp.....1 MHz
- Triangle.....1 MHz

Frequency resolution (DDS Mode) .....9.31 mHz

Voltage Output

Ranges .....±5 V into a 50 Ω load
±10 V into a high impedance load

Accuracy.....±0.1 dB

Output attenuation ..... 0 to 73 dB
Resolution ..... 0.001 dB steps

Pre-attenuation offset
Range ..... ±2.5 V into 50 Ω
(but with less than 10 dB of attenuation, signal maximum plus offset (before attenuation) must not exceed ±5 V (into 50 Ω))
Accuracy ..... ±5 mV

Output coupling ..... DC

Output impedance ..... 50 Ω or 75 Ω software selectable

Load impedance ..... 50 Ω or greater

Output enable ..... Software switchable

Protection ..... Short-circuit protected

Sine Spectral Purity

Harmonic products and spurious
up to 1 MHz ..... –60 dBc
up to 16 MHz ..... –35 dBc

Phase noise ..... –105 dBc/Hz at 10 kHz from carrier

Filter Characteristics

Digital
Type ..... Half-band interpolating
Selection ..... Software switchable
Taps 67
Filter coefficients ..... Fixed 20-bit
Data interpolating frequency ..... 80 MS/s
Pipeline signal delay ..... 26 sampling periods

☞ **Note:** ***The digital filter will be operational only for sample rates of 40 MHz and 20 MHz. For other sample rates, the digital filter will not be of any use.***

Analog

Type.....7th-order L-C low-pass filter
Passband ripple .....±2 dB

Waveform Specifications

Memory

Arb mode .....2,000,000, 16-bit samples
DDS mode.....16,384, 16-bit samples

Segment length

Arb mode .....256 samples min, multiples of eight samples
DDS mode.....16,384 samples, exact

Max segments in waveform memory...5,000
(Arb mode only)

Segment linking (instruction FIFO)

Arb mode .....292 links
DDS mode.....340 links

Segment looping (Arb mode only)

Count .....65,536 loops

Timing I/O

Update clock.....Internal, 40 MHz max
Interval count 2–65,535

Phase locking

External reference sources.....Input connector, RTSI clock line, or internal
Reference clock frequencies.....1 MHz, 5–20 MHz, in 1 MHz steps
Frequency locking range .....±100 ppm

Triggers

Digital Trigger

Compatibility ..... TTL

Response ..... Rising edge

Pulse width (T_{d1}) ..... 20 ns min

Trigger to waveform output (Arb mode)
delay (T_{d2}) ..... 76 sample clocks + 38 ns max

Trigger to waveform output (DDS mode)
delay (T_{d2}) ..... 28 sample clocks + 150 ns max

RTSI

Trigger lines 7

Clock lines 1

Bus Interface

Type ..... Slave

Operational Modes

Type ..... Single, continuous, burst, stepped

Other Outputs

SYNC Out

Level ..... TTL

Duty cycle ..... 20% to 80%, software controllable

Marker Output

Types .....TTL

Location .....User defined, one per stage

Pulse width (T_{d4}) .....8 sample clock periods

Arb output delay from marker (T_{d3})....50 ns max

Digital Pattern Output

Sample rate .....40 MHz max

Resolution .....16 bits

Sample clock logic.....TTL

Clock pulse HIGH time.....25 ns fixed
(for clock interval counts > 1)

PCLK to pattern data
output time (T_{co}).....1 ns max

Digital pattern logic .....TTL

Logic level output ratings for
SYNC, marker, digital pattern, and
sample clock outputs .....

Type	Min	Max
V_{OH}	3.0 V	–
V_{OL}	–	0.7 V
I_{OH}	–	1.0 mA
I_{OL}	–	1.0 mA

V_{OH} = voltage output for logic level 1
V_{OL} = voltage output for logic level 0
I_{OH} = current output for logic level 1
I_{OL} = current output for logic level 0

External Clock Reference Input

Frequency ..... 1 MHz or 5–20 MHz in 1 MHz steps

Amplitude ..... 1 $V_{pk-pk} \leq$ level $\leq$ 5 V_{pk-pk}

Internal clock

Frequency ..... 40 MHz

Initial accuracy..... ±5 ppm

Temperature stability (0° to 5° C)..... ±25 ppm

Aging (1 year)..... ±5 ppm

Mechanical

Connectors

- ARB (output)..... SMB
- SYNC (output) ..... SMB
- PLL Reference (input)..... SMB
- Digital I/O (Digital Pattern Out, Marker Out, External Trigger In)..... 50-pin digital

Size ..... 1 slot

Power Requirements ..... 5 V, 3.5 A max
12V, 125 mA

Waveform Sampling and Interpolation

Appendix
B

This appendix describes the basics of waveform sampling and interpolation.

According to Shannon's sampling theorem, a digital waveform must be updated at least twice as fast as the bandwidth of the signal to be accurately generated. Even though the theoretical requirement for update clock, f_c, is twice that of the bandwidth of the signal of interest, it is very difficult to design an analog filter that will reject the images above the passband and also get maximum output bandwidth, as represented by the curve, Analog Filter 1, shown in Figure B-1.

Analog Filter 2 represents a more practical filter. This filter is not as aggressive and does not filter out the images near f_c, but it does reject all the others.

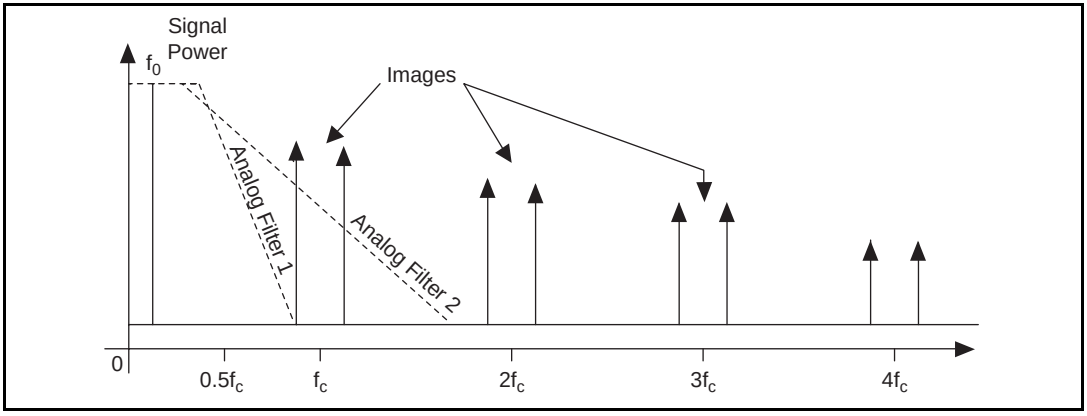


Figure B-1. Analog Filter and Signal Images without Digital Filtering

To ease the requirements of the analog filter and to get more output bandwidth, the DAQArb 5411 uses a half-band digital filter to interpolate a sample between every two samples at twice the update frequency, $2f_c$. Also, the DAC operates at twice the sample frequency. This increase pushes the images from f_c to $2f_c$ and the analog filter roll-off easily rejects any images from the output spectrum. This behavior can be seen in the frequency domain representation from Figure B-2 and in the time domain representation from Figure B-3.

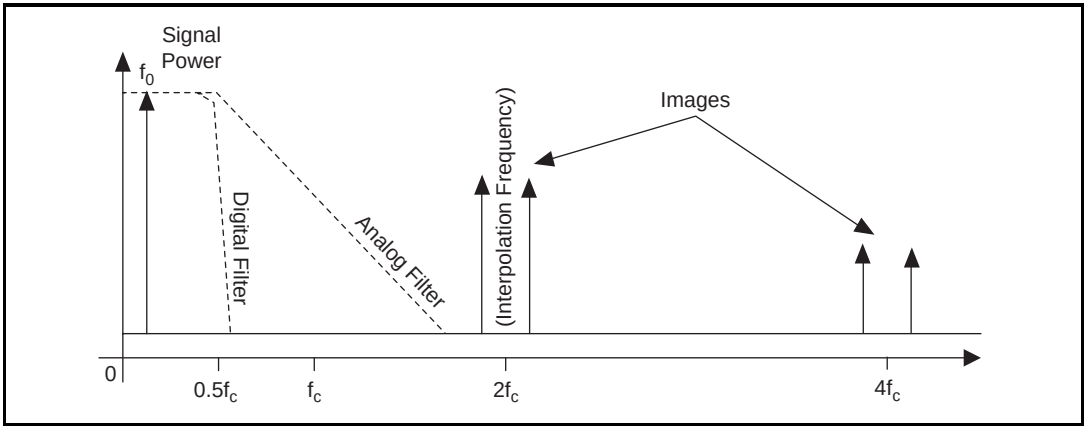


Figure B-2. Digital Filter, Analog Filter, and Signal Images with Digital Filtering

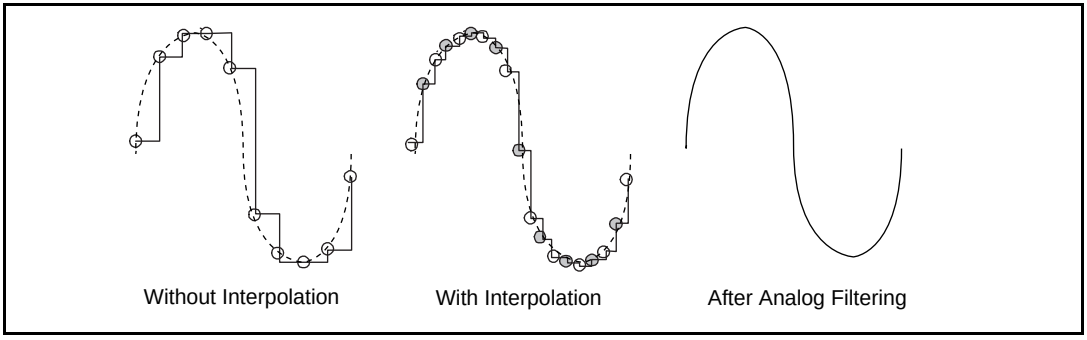


Figure B-3. Waveform Updates

☞ **Note:** ***The digital filter will be operational only for sample rates of 40 MHz and 20 MHz. For other sample rates, the digital filter will not be of any use.***

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Customer Communication

Appendix C

For your convenience, this appendix contains forms to help you gather the information necessary to help us solve your technical problems and a form you can use to comment on the product documentation. When you contact us, we need the information on the Technical Support Form and the configuration form, if your manual contains one, about your system configuration to answer your questions as quickly as possible.

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Up to 9,600 baud, 8 data bits, 1 stop bit, no parity

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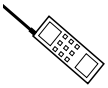
E-Mail Support (currently U.S. only)

You can submit technical support questions to the applications engineering team through e-mail at the Internet address listed below. Remember to include your name, address, and phone number so we can contact you with solutions and suggestions.

`support@natinst.com`

Telephone and Fax Support

National Instruments has branch offices all over the world. Use the list below to find the technical support number for your country. If there is no National Instruments office in your country, contact the source from which you purchased your software to obtain support.





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Belgium	02 757 00 20	02 757 03 11
Canada (Ontario)	905 785 0085	905 785 0086
Canada (Quebec)	514 694 8521	514 694 4399
Denmark	45 76 26 00	45 76 26 02
Finland	09 725 725 11	09 725 725 55
France	01 48 14 24 24	01 48 14 24 14
Germany	089 741 31 30	089 714 60 35
Hong Kong	2645 3186	2686 8505
Israel	03 5734815	03 5734816
Italy	02 413091	06 57284309
Japan	03 5472 2970	03 5472 2977
Korea	02 596 7456	02 596 7455
Mexico	5 520 2635	5 520 3282
Netherlands	0348 433466	0348 430673
Norway	32 84 84 00	32 84 86 00
Singapore	2265886	2265887
Spain	91 640 0085	91 640 0533
Sweden	08 730 49 70	08 730 43 70
Switzerland	056 200 51 51	056 200 51 55
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Technical Support Form

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If you are using any National Instruments hardware or software products related to this problem, include the configuration forms from their user manuals. Include additional pages if necessary.

Name _____

Company _____

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Fax (___)_____ Phone (___) _____

Computer brand _____ Model _____ Processor_____

Operating system (include version number) _____

Clock speed _____MHz RAM _____MB Display adapter _____

Mouse ___yes ___no Other adapters installed _____

Hard disk capacity _____MB Brand _____

Instruments used _____

_____

National Instruments hardware product model _____ Revision _____

Configuration _____

National Instruments software product _____ Version _____

Configuration _____

The problem is: _____

_____

_____

_____

_____

List any error messages: _____

_____

_____

The following steps reproduce the problem:_____

_____

_____

_____

_____

_____

DAQArb 5411 Hardware and Software Configuration Form

Record the settings and revisions of your hardware and software on the line to the right of each item. Complete a new copy of this form each time you revise your software or hardware configuration, and use this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

National Instruments Products

DAQ hardware _____

Serial number _____

Interrupt level of hardware _____

DMA channels of hardware _____

Base I/O address of hardware _____

Programming choice _____

NI-DAQ, LabVIEW, LabWindows/CVI, or VirtualBench version _____

Other boards in system _____

Base I/O address of other boards _____

DMA channels of other boards _____

Interrupt level of other boards _____

Other Products

Computer make and model _____

Microprocessor _____

Clock frequency or speed _____

Type of video board installed _____

Operating system version _____

Operating system mode _____

Programming language _____

Programming language version _____

Other boards in system _____

Base I/O address of other boards _____

DMA channels of other boards _____

Interrupt level of other boards _____

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Prefix	Meaning	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}

Numbers/Symbols

%	percent
+	positive of, or plus
-	negative of, or minus
±	plus or minus
/	per
°	degree
Ω	ohm
+5V	+5 V output signal

A

A	amperes
AC	alternating current
AMM	advanced memory module—used for storing waveform buffers for the Arb mode of waveform generation. The standard AMM size is 2,000,000 16-bit samples.
amplification	method of scaling the signal level to a higher level
ARB	normal waveform output signal
Arb mode	a mode of generating waveforms in which waveforms are defined by multiple buffers that can be linked or looped in any order
arbitrary waveform generator	instrument for generating any desired waveform; this instrument is not restricted to standard waveforms such as sine or square
ASIC	Application-Specific Integrated Circuit—a proprietary semiconductor component designed and manufactured to perform a set of specific functions for a specific customer
AT bus	*See* bus.
attenuation	decreasing the amplitude of a signal

B

b	bit—one binary digit, either 0 or 1
B	byte—eight related bits of data, an eight-bit binary number. Also used to denote the amount of memory required to store one byte of data.
bandwidth	the range of frequencies present in a signal, or the range of frequencies to which a measuring device can respond
BNC	a type of coaxial signal connector
buffer	temporary storage for acquired or generated data
buffer linking	linking different buffers stored in the waveform memory

buffer looping	repeating the same buffer in the waveform memory. This method of waveform generation decreases memory requirements.
burst trigger mode	repeats a stage until a trigger advances the waveform to the next stage
bus	the group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. Examples of PC buses are the AT bus (also known as the ISA bus) and the PCI bus.
bus master	a type of a plug-in board or controller with the ability to read and write devices on the computer bus

C

C	Celsius
CalDAC	calibration DAC
clock	hardware component that controls timing for reading from or writing to groups
continuous trigger mode	repeats a staging list until waveform generation is stopped
conversion device	device that transforms a signal from one form to another. For example, analog-to-digital converters (ADCs) for analog input, digital-to-analog converters (DACs) for analog output, digital input or output ports, and counter/timers are conversion devices.
counter/timer	a circuit that counts external pulses or clock pulses (timing)
coupling	the manner in which a signal is connected from one location to another
CPU	central processing unit

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current

DAQ	data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO boards plugged into a computer, and possibly generating control signals with D/A and/or DIO boards in the same computer
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB=20log10 V1/V2, for signals in volts
DC	direct current
DC coupled	allowing the transmission of both AC and DC signals
DDS	direct digital synthesis—a digital technique of frequency generation using a numerically controlled oscillator (NCO), a dedicated lookup memory, and a DAC
DDS mode	a method of waveform generation that uses built-in DDS functionality to generate very high frequency resolution standard waveforms
default setting	a default parameter value recorded in the driver. In many cases, the default input of a control is a certain value (often 0) that means *use the current default setting*.
device	a plug-in data acquisition board, card, or pad that can contain multiple channels and conversion devices. Plug-in boards, PCMCIA cards, and devices such as the DAQPad-1200, which connects to your computer parallel port, are all examples of DAQ devices.
DGND	digital ground signal
DMA	direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
drivers	software that controls a specific hardware device such as a DAQ board or a GPIB interface board
dynamic range	the ratio of the largest signal level a circuit can handle to the smallest signal level it can handle (usually taken to be the noise level), normally expressed in dB

E

EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
external trigger	a voltage pulse from an external source that triggers an event such as A/D conversion
EXT_TRIG	external trigger input signal

F

FIFO	first-in first-out memory buffer—the first data stored is the first data sent to the acceptor. FIFOs are often used on DAQ devices to temporarily store incoming or outgoing data until that data can be retrieved or output. For example, an analog input FIFO stores the results of A/D conversions until the data can be retrieved into system memory, a process that requires the servicing of interrupts and often the programming of the DMA controller. This process can take several milliseconds in some cases. During this time, data accumulates in the FIFO for future retrieval. With a larger FIFO, longer latencies can be tolerated. In the case of analog output, a FIFO permits faster update rates, because the waveform data can be stored on the FIFO ahead of time. This again reduces the effect of latencies associated with getting the data from system memory to the DAQ device.
filters	digital or analog circuits that change the frequency characteristics of a waveform
frequency resolution	the smallest frequency change that can be generated by a DAQArb 5411
ft	feet

G

gain	the factor by which a signal is amplified, sometimes expressed in decibels

H

h	hour
hardware	the physical components of a computer system, such as the circuit boards, plug-in boards, chassis, enclosures, peripherals, cables, and so on
Hz	hertz—the number of cycles or repetitions per second

I

IC	integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
in.	inches
instruction FIFO	the FIFO that stores the waveform generation staging list
interrupt	a computer signal indicating that the CPU should suspend its current task to service a designated activity
interrupt level	the relative priority at which a device can interrupt
I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
ISA	industry standard architecture

K

k	kilo—the standard metric prefix for 1,000, or 10^3, used with units of measure such as volts, hertz, and meters
K	kilo—the prefix for 1,024, or 2^{10}, used with B in quantifying data or computer memory
kbytes/s	a unit for data transfer that means 1,000 or 10^3 bytes/s
kS	1,000 samples

Kword	1,024 words of memory

L

LabVIEW	laboratory virtual instrument engineering workbench
latch	a digital device that stores digital data based on a control signal
latched digital I/O	a type of digital acquisition/generation where a device or module accepts or transfers data after a digital pulse has been received. Also called handshaked digital I/O.
LED	light-emitting diode
level DAC	the calibration DAC used to change the voltage levels to another device
low-pass filter	a circuit used to smooth the waveform output and removed unwanted high frequency contents form the signal
LSB	least significant bit

M

m	meters
M	(1) Mega, the standard metric prefix for 1 million or 10^6, when used with units of measure such as volts and hertz; (2) mega, the prefix for 1,048,576, or 2^{20}, when used with B to quantify data or computer memory
marker	a digital signal that is generated on a pin on the digital I/O connector at a requested point in the waveform buffer; this happens while the analog waveform is being generated at the DAQArb 5411 Arb output connector
MARKER	marker output signal
marker offset	the position, in number of samples, from the start of the waveform buffer at which the marker is requested
master/slave phase locking	locking the DAQArb 5411 clock in frequency and phase to an external reference clock source
MB	megabytes of memory

Mbytes/s	a unit for data transfer that means 1 million or 10^6 bytes/s
MIPS	million instructions per second—the unit for expressing the speed of processor machine code instructions
MS	million samples
MSB	most significant bit
MTBF	mean time between failure
mux	multiplexer—a switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel

N

NI-DAQ	NI driver software for DAQ hardware
NIST	National Institute of Standards and Technology
noise	an undesirable electrical signal—Noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, soldering irons, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.

O

onboard RAM	optional RAM usually installed into SIMM slots
operating system	base-level software that controls a computer, runs programs, interacts with users, and communicates with installed hardware or peripheral devices
output enable relay	a relay switch at the output of the DAQArb 5411 that can enable the waveform generation at any time or that can connect the output to ground

P

PA<0..15>	digital pattern generator outputs
passband	the range of frequencies which a device can properly propagate or measure
pattern generation	a type of handshaked (latched) digital I/O in which internal counters generate the handshaked signal, which in turn initiates a digital transfer. Because counters output digital pulses at a constant rate, this means you can generate and retrieve patterns at a constant rate because the handshaked signal is produced at a constant rate.
PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and workstations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.
PCLK	digital pattern clock output
peak to peak	a measure of signal amplitude; the difference between the highest and lowest excursions of the signal
pipeline	a high-performance processor structure in which the completion of an instruction is broken into its elements so that several elements can be processed simultaneously from different instructions
PLL	phase-locked loop—a circuit that synthesizes a signal whose frequency is exactly proportional to the frequency of a reference signal
PLL Ref	a PLL input that accepts an external reference clock signal and phase locks to it the DAQArb 5411 internal clock
Plug and Play devices	devices that do not require dip switches or jumpers to configure resources on the devices—also called switchless devices
Plug and Play ISA	a specification prepared by Microsoft, Intel, and other PC-related companies that will result in PCs with plug-in boards that can be fully configured in software, without jumpers or switches on the boards
ppm	parts per million
pre-attenuation offset	an offset provided to the signal before it reaches the attenuators

protocol	the exact sequence of bits, characters, and control codes used to transfer data between computers and peripherals through a communications channel, such as the GPIB bus
pts	points

R

RAM	random-access memory
resolution	the smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has 12-bit resolution, one part in 4,096 resolution, and 0.0244 percent of full scale.
rms	root mean square—the square root of the average value of the square of the instantaneous signal amplitude; a measure of signal amplitude
ROM	read-only memory
RTSI bus	real-time system integration bus—the National Instruments timing bus that connects DAQ boards directly, by means of connectors on top of the boards, for precise synchronization of functions

S

s	seconds
S	samples
sampling rate	the rate, in samples per second (S/s), at which each sample in the waveform buffer is updated
SCXI	Signal Conditioning eXtensions for Instrumentation—the National Instruments product line for conditioning low-level signals within an external chassis near sensors so only high-level signals are sent to DAQ boards in the noisy PC environment
sequence list	*See* staging list.

Shannon's Sampling Theorem	a law of sampling theory stating that if a continuous bandwidth-limited signal contains no frequency components higher than half the frequency at which it is sampled, then the original signal can be recovered without distortion
single trigger mode	when the arbitrary waveform generator goes through the staging list only once
SMB	a type of miniature coaxial signal connector
S/s	samples per second—used to express the rate at which a DAQ board samples an analog signal
stage	in Arb mode, specifies the buffer to be generated, the number of loops on that buffer, the marker position for that buffer, and the sample count for the buffer; for DDS mode, specifies the frequency to be generated of the waveform in the lookup memory and the time for which that frequency has to be generated
staging list	a buffer that contains linking and looping information for multiple waveforms; also known as a sequence list or waveform sequence
stepped trigger mode	a mode of waveform generation used when you want a trigger to advance the waveforms specified by the stages in the staging list
SYNC	TTL version of the sine waveform output signal generated by the DAQArb 5411
system noise	a measure of the amount of noise seen by an analog circuit or an ADC when the analog inputs are grounded

T

transfer rate	the rate, measured in bytes/s, at which data is moved from source to destination after software initialization and set up operations; the maximum rate at which the hardware can operate
trigger	any event that causes or starts some form of data capture
TTL	transistor-transistor logic

U

update rate	the rate at which a DAC is updated

V

V	volts
VCXO	voltage controlled crystal oscillator
VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic standalone instrument (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program

W

waveform	multiple voltage readings taken at a specific sampling rate
waveform buffers	the collection of 16-bit data samples stored in the waveform memory that represent a desired waveform. Also known as a waveform segment.
waveform memory	physical data storage on the DAQArb 5411 for storing the waveform data samples
waveform segment	*See* waveform buffer.
waveform sequence	*See* staging list.

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