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DAQ

Lab-PC-1200/AI
User Manual

Multifunctional I/O Board for the PC AT

June 1996 Edition
Part Number 321230A-01

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About This Manual

This manual describes the electrical and mechanical aspects of the 1200 Series boards and contains information concerning their operation and programming.

The Lab-PC-1200 and Lab-PC-1200AI boards are low-cost analog, digital, and timing boards designed for use in PC AT series computers. Additionally, the Lab-PC-1200 has analog output capabilities. These boards are designed for high-performance data acquisition (DAQ) and control for applications in laboratory testing, production testing, and industrial process monitoring and control.

Organization of This Manual

The *Lab-PC-1200/AI User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the 1200 Series boards, lists what you need to get started, software programming choices, and optional equipment, and explains how to build custom cables and unpack your board.
- Chapter 2, *Installation and Configuration*, describes how to install and configure your 1200 Series board.
- Chapter 3, *Signal Connections*, describes how to make input and output signal connections to the 1200 Series boards via the board I/O connector and details the I/O timing specifications.
- Chapter 4, *Theory of Operation*, explains the operation of each functional unit of the 1200 Series boards.
- Chapter 5, *Calibration*, discusses the calibration procedures for the 1200 Series analog I/O circuitry.
- Appendix A, *Specifications*, lists the specifications for the 1200 Series boards.
- Appendix B, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products.

- The *Glossary* contains an alphabetical list and description of terms used in this manual, including abbreviations, acronyms, metric prefixes, mnemonics, and symbols.
- The *Index* contains an alphabetical list of key terms and topics in this manual, including the page where you can find each one.

Conventions Used in This Manual

The following conventions are used in this manual.

♦	The ♦ symbol indicates that the text following it applies only to a specific 1200 Series board.
< >	Angle brackets containing numbers separated by an ellipses represent a range of values associated with a bit, signal, or port (for example, ACH<0..7> stands for ACH0 through ACH7).
1200 Series	1200 Series refers to both the Lab-PC-1200 and Lab-PC-1200AI boards, unless otherwise noted.
bold	Bold text denotes menus, menu items, or dialog box buttons or options.
bold italic	Bold italic text denotes a note, caution, or warning.
italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept.
`monospace`	Text in this font denotes text or characters that are to be literally input from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, variables, filenames, and extensions, and for statements and comments taken from program code.
NI-DAQ	NI-DAQ refers to the NI-DAQ software for PC compatibles, unless otherwise noted.
SCXI	SCXI stands for Signal Conditioning eXtensions for Instrumentation and is a National Instruments product line designed to perform front-end signal conditioning for National Instruments plug-in DAQ boards.

Abbreviations, acronyms, metric prefixes, mnemonics, symbols, and terms are listed in the *Glossary*.

National Instruments Documentation

The *Lab-PC-1200/AI User Manual* is one piece of the documentation set for your DAQ system. You could have any of several types of manuals, depending on the hardware and software in your system. Use the manuals you have as follows:

- *Getting Started with SCXI*—If you are using SCXI, this is the first manual you should read. It gives an overview of the SCXI system and contains the most commonly needed information for the modules, chassis, and software.
- Your SCXI hardware user manuals—If you are using SCXI, read these manuals next for detailed information about signal connections and module configuration. They also explain in greater detail how the module works and contain application hints.
- Your DAQ hardware user manuals—These manuals have detailed information about the DAQ hardware that plugs into or is connected to your computer. Use these manuals for hardware installation and configuration instructions, specification information about your DAQ hardware, and application hints.
- Software documentation—Examples of software documentation you may have are the LabVIEW and LabWindows®/CVI documentation sets and the NI-DAQ documentation. After you set up your hardware system, use either the application software (LabVIEW or LabWindows/CVI) manuals or the NI-DAQ documentation to help you write your application. If you have a large and complicated system, it is worthwhile to look through the software documentation before you configure your hardware.
- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides and accessory board user manuals. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making your connections.
- SCXI chassis manuals—If you are using SCXI, read these manuals for maintenance information on the chassis and installation instructions.

Related Documentation

The following National Instruments document contains information that you may find helpful as you read this manual:

- Application Note 025, *Field Wiring and Noise Considerations for Analog Signals*

The following documents also contain information that you may find helpful:

- "Dither in Digital Audio," by John Vanderkooy and Stanley P. Lipshitz, *Journal of the Audio Engineering Society, Vol. 35, No. 12, December 1987.*
- Your computer's technical reference manual

The following National Instruments manual contains detailed information for the register-level programmer:

- *Lab-PC-1200/AI Register-Level Programmer Manual*

This manual is available from National Instruments by request. If you are using NI-DAQ or LabVIEW, you should not need the register-level programmer manual. Using NI-DAQ, LabVIEW, or LabWindows/CVI is easier than, and as flexible as, using the low-level programming described in the register-level programmer manual. Refer to the *Software Programming Choices* section in Chapter 1, *Introduction*, of this manual to learn about your programming options.

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix B, *Customer Communication*, at the end of this manual.

Chapter 1

Introduction

This chapter describes the 1200 Series boards, lists what you need to get started, software programming choices, and optional equipment, and explains how to build custom cables and unpack your board.

About the Lab-PC-1200/AI

Thank you for purchasing the Lab-PC-1200 or Lab-PC-1200AI board. These boards are low-cost, high-performance analog, digital, and timing boards for PC AT and compatible computers. Additionally, the Lab-PC-1200 has analog output capabilities. The 1200 Series boards have eight analog input channels that you can configure as eight single-ended or four differential inputs, a 12-bit successive-approximation ADC, 24 lines of TTL-compatible digital I/O, and three 16-bit counter/timers for timing I/O.

The 1200 Series boards are completely switchless and jumperless data acquisition boards. This allows DMA, interrupts, and base I/O addresses to be assigned by your system to avoid resource conflicts with other boards in your system. These boards are designed for high-performance data acquisition and control for applications in laboratory testing, production testing, and industrial process monitoring and control.

Detailed specifications for your 1200 Series board are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use your 1200 Series boards, you will need the following:

- ❑ One of the following boards:
  - Lab-PC-1200
  - Lab-PC-1200AI
- ❑ *Lab-PC-1200/AI User Manual*

- ❑ One of the following software packages and documentation:
  - LabVIEW for Windows
  - LabWindows/CVI for Windows
  - NI-DAQ for PC compatibles
- ❑ Your computer

Software Programming Choices

There are several options to choose from when programming your National Instruments DAQ and SCXI hardware. You can use LabVIEW, LabWindows/CVI, NI-DAQ, or register-level programming.

LabVIEW and LabWindows/CVI Application Software

LabVIEW and LabWindows/CVI are innovative program development software packages for data acquisition and control applications. LabVIEW uses graphical programming, whereas LabWindows/CVI enhances traditional programming languages. Both packages include extensive libraries for data acquisition, instrument control, data analysis, and graphical data presentation.

LabVIEW features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to the NI-DAQ software.

LabWindows/CVI features interactive graphics, a state-of-the-art user interface, and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions for using LabWindows/CVI with National Instruments DAQ hardware, is included with the NI-DAQ software kit. The LabWindows/CVI Data Acquisition library is functionally equivalent to the NI-DAQ software.

Using LabVIEW or LabWindows/CVI software will greatly reduce the development time for your data acquisition and control application.

NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ is not packaged with SCXI or accessory products, except for the SCXI-1200. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation (timed D/A conversion), digital I/O, counter/timer operations, SCXI, RTSI, self-calibration, messaging, and acquiring data to memory.

NI-DAQ has both high-level DAQ I/O functions for maximum ease of use and low-level DAQ I/O functions for maximum flexibility and performance. Examples of high-level functions are streaming data to disk or acquiring a certain number of data points. An example of a low-level function is writing directly to registers on the DAQ device. NI-DAQ does not sacrifice the performance of National Instruments DAQ devices because it lets multiple devices operate at their peak performance.

NI-DAQ also internally addresses many of the complex issues between the computer and the DAQ hardware such as programming interrupts and DMA controllers. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Whether you are using conventional programming languages, LabVIEW, or LabWindows/CVI, your application uses the NI-DAQ driver software, as illustrated in Figure 1-1.

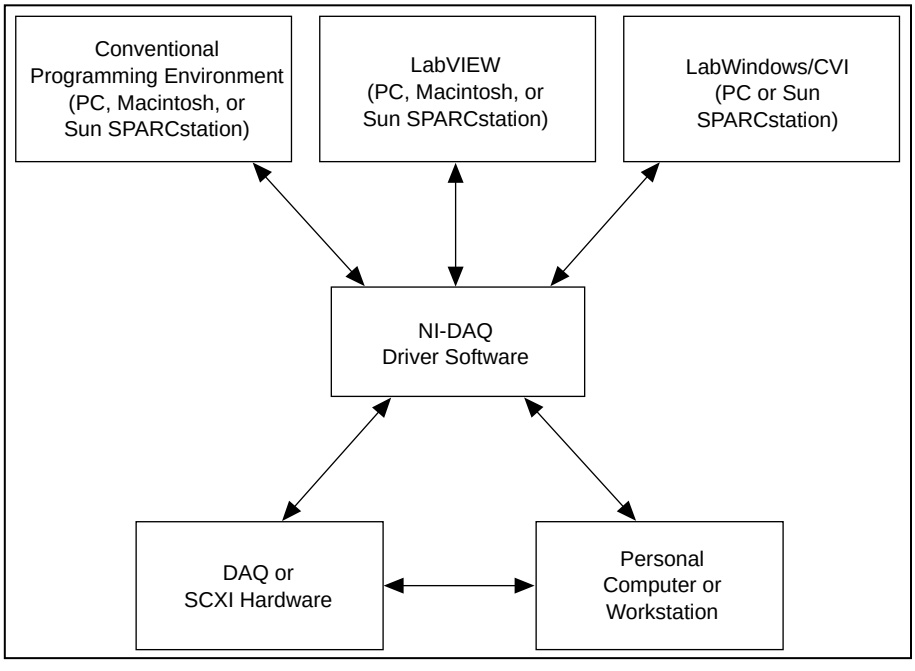


Figure 1-1. The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

Register-Level Programming

The final option for programming any National Instruments DAQ hardware is to write register-level software. Writing register-level programming software can be very time-consuming and inefficient, and is not recommended for most users.

Even if you are an experienced register-level programmer, consider using NI-DAQ, LabVIEW, or LabWindows/CVI to program your National Instruments DAQ hardware. Using the NI-DAQ, LabVIEW, or LabWindows/CVI software is easier than, and as flexible as, register-level programming, and can save weeks of development time.

Optional Equipment

National Instruments offers a variety of products to use with your Lab-PC-1200/AI board, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies
- Connector blocks, 50-pin screw terminals
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI you can condition and acquire up to 3,072 channels.
- Low channel count signal conditioning modules, boards, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold, and relays.

For specific information about these products, refer to your National Instruments catalogue or call the office nearest you.

Custom Cabling

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change board interconnections.

If you want to develop your own cable, however, the following guidelines may be useful:

- For the analog input signals, shielded twisted-pair wires for each analog input pair yield the best results if you use differential inputs. Tie the shield for each signal pair to the ground reference at the source.
- Route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

The mating connector for the Lab-PC-1200/AI is a 50-position, polarized, ribbon socket connector with strain relief. National Instruments uses a polarized (keyed) connector to prevent inadvertent upside-down connection to the Lab-PC-1200/AI. Recommended manufacturer part numbers for this mating connector are as follows:

- Electronic Products Division/3M (part number 3425-7650)
- T&B/Ansley Corporation (part number 609-5041CE)

Unpacking

Your 1200 Series board is shipped in an antistatic package to prevent electrostatic damage to the board. Electrostatic discharge can damage several components on the board. To avoid such damage in handling the board, take the following precautions:

- Ground yourself via a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of your computer chassis before removing the board from the package.
- Remove the board from the package and inspect the board for loose components or any other sign of damage. Notify National Instruments if the board appears damaged in any way. *Do not* install a damaged board into your computer.
- *Never* touch the exposed pins of connectors.

Installation and Configuration

Chapter 2

This chapter describes how to install and configure your 1200 Series board.

Software Installation

If you are using NI-DAQ, refer to your NI-DAQ release notes to install your driver software. Find the installation section for your operating system and follow the instructions given there.

If you are using LabVIEW, refer to your LabVIEW release notes to install your application software. After you have installed LabVIEW, refer to the NI-DAQ release notes and follow the instructions given there for your operating system and LabVIEW.

If you are using LabWindows/CVI, refer to your LabWindows/CVI release notes to install your application software. After you have installed LabWindows/CVI, refer to the NI-DAQ release notes and follow the instructions given there for your operating system and LabWindows/CVI.

Hardware Installation

☞ **Note:** ***You should install your driver software before installing your hardware. Refer to your NI-DAQ release notes for software installation instructions.***

You can install your 1200 Series board in any unused expansion slot in your computer.

The following are general installation instructions. Consult your computer user manual or technical reference manual for specific instructions and warnings.

1. Write down your board's serial number in the hardware and software configuration form in Appendix B, *Customer Communication*. You will need this information when you install and configure your board.

2. Turn off your computer.
3. Remove the top cover or access port to the I/O channel.
4. Remove the expansion slot cover on the back panel of the computer.
5. Insert the board into an unused 8-bit or 16-bit ISA slot. The fit may be tight, but *do not* force the board into place.
6. Screw the board's mounting bracket to the back panel rail of the computer to secure the 1200 Series board in place.
7. Check the installation.
8. Replace the top cover on the computer.

Your 1200 Series board is installed. You are now ready to configure your board.

Hardware Configuration

The 1200 Series boards are completely software-configurable. Two types of configuration are performed on the board—bus-related and data acquisition-related. Bus-related configuration includes setting the base I/O address, DMA channel, and interrupt channel. Data acquisition-related configuration includes such settings as analog I/O polarity selection, range selection, digital I/O configuration, and other settings. For more information about data acquisition-related configuration, refer to your NI-DAQ documentation.

Bus-Related Configuration

Your 1200 Series board works in either a Plug and Play mode or a switchless mode. These modes dictate how the base I/O address, DMA channel, and interrupt channel are determined and assigned to the board.

Plug and Play Mode

The 1200 Series boards are fully compatible with the industry-standard Intel/Microsoft Plug and Play Specification version 1.0. Your Plug and Play system arbitrates and assigns resources through software, freeing you from manually setting switches and jumpers. These resources include the board base I/O address, DMA channel, and interrupt channel. The 1200 Series boards are configured at the factory to request these resources from the Plug and Play Configuration Manager.

The Configuration Manager receives all of the resource requests at startup, compares the available resources to those requested, and assigns the available resources as efficiently as possible to the Plug and Play boards. Application software can query the Configuration Manager to determine the resources assigned to each board without your involvement. The Plug and Play software is installed as a device driver or as an integral component of the computer BIOS.

If you have the Windows 95 operating system on your computer, it will configure your 1200 Series board. Refer to your NI-DAQ documentation for more information.

Switchless Mode

You can use your 1200 Series board in a non-Plug and Play system as a switchless DAQ board. A non-Plug and Play system is a system in which the Configuration Manager has not been installed and which does not contain any non-National Instruments Plug and Play products. You use a configuration utility to enter the base address, DMA channel, and interrupt channel selections, and the application software assigns it to the board.

☞ **Note:** ***To avoid resource conflicts with non-National Instruments boards, do not configure two boards for the same base address.***

Base I/O Address Selection

You can configure your 1200 Series board to use base addresses in the range of 100 to 3E0 hex. The 1200 Series boards occupy 32 bytes of address space and must be located on a 32-byte boundary. Therefore, valid addresses include 100, 120, 140, ..., 3C0, 3E0 hex. This selection is software-configured and does not require you to manually change any board settings.

DMA Channel Selection

The 1200 Series boards can use one DMA channel for data transfers with the analog input section of the board. The 1200 Series boards can use DMA channels 1 or 3. These selections are all software-configured and do not require you to manually change any board settings.

Interrupt Channel Selection

The 1200 Series boards can increase bus efficiency by using an interrupt channel. You can use an interrupt channel for event notification without the use of polling techniques. The 1200 Series boards can use interrupt channels 3, 4, 5, 7, or 9. These selections are all software configured and do not require you to manually change any board settings. Tables 2-1 and 2-2 provide information concerning possible resource conflicts when configuring your 1200 Series board.

Table 2-1. PC AT I/O Address Map

I/O Address Range (Hex)	Device
100 to 1EF	Unreserved
1F0 to 1FF	IBM PC AT Fixed Disk
200 to 20F	PC and PC AT Game Controller, reserved
210 to 213	PC-DIO-24—default
218 to 21F	Unreserved
220 to 23F	Previous generation of AT-MIO boards—default
240 to 25F	AT-DIO-32F—default
260 to 27F	Lab-PC/PC+ —default Lab-PC-1200/AI—recommended in switchless mode
278 to 28F	AT Parallel Printer Port 2 (LPT2)
279	Reserved for Plug and Play operation
280 to 29F	WD EtherCard+ —default
2A0 to 2BF	Unreserved
2E2 to 2F7	Unreserved
2F8 to 2FF	PC, AT Serial Port 2 (COM2)

Table 2-1. PC AT I/O Address Map (Continued)

I/O Address Range (Hex)	Device
300 to 30F	3Com EtherLink—default
310 to 31F	Unreserved
320 to 32F	ICM PC/XT Fixed Disk Controller
330 to 35F	Unreserved
360 to 363	PC Network (low address)
364 to 367	Reserved
368 to 36B	PC Network (high address)
36C to 36F	Reserved
378 to 37F	PC, AT Parallel Printer Port 1 (LPT1)
380 to 38C	SDLC Communications
380 to 389	Bisynchronous (BSC) Communications (alternate)
390 to 393	Cluster Adapter 0
394 to 39F	Unreserved
3A0 to 3A9	BSC Communications (primary)
3AA to 3AF	Unreserved
3B0 to 3BF	Monochrome Display/Parallel Printer Adapter 0
3C0 to 3CF	Enhanced Graphics Adapter, VGA
3D0 to 3DF	Color/Graphics Monitor Adapter, VGA
3E0 to 3EF	Unreserved
3F0 to 3F7	Diskette Controller

Table 2-1. PC AT I/O Address Map (Continued)

I/O Address Range (Hex)	Device
3F8 to 3FF	Serial Port 1 (COM1)
A79	Reserved for Plug and Play operation

Table 2-2. PC AT Interrupt Assignment Map

IRQ	Device
15	Available
14	Fixed Disk Controller
13	Coprocessor
12	AT-DIO-32F—default
11	AT-DIO-32F—default
10	AT-MIO-16—default
9	PC Network—default PC Network Alternate—default
8	Real Time Clock
7	Parallel Port 1 (LPT1)
6	Diskette Drive Controller Fixed Disk and Diskette Drive Controller
5	Parallel Port 2 (LPT2) PC-DIO-24—default Lab-PC/PC+—default Lab-PC-1200/AI—recommended in switchless mode
4	Serial Port 1 (COM1) BSC, BSC Alternate

Table 2-2. PC AT Interrupt Assignment Map (Continued)

IRQ	Device
3	Serial Port 2 (COM2) BSC, BSC Alternate Cluster (primary) PC Network, PC Network Alternate WD EtherCard+ — default 3Com EtherLink — default
2	IRQ 8-15 Chain (from interrupt controller 2)
1	Keyboard Controller Output Buffer Full
0	Timer Channel 0 Output

Data Acquisition-Related Configuration

Analog I/O Configuration

- Lab-PC-1200

  Upon power up or after a software reset, the Lab-PC-1200 is set to the following configuration:

  - Referenced single-ended input mode
  - ±5 V analog input range (bipolar)
  - ±5 V analog output range (bipolar)

  Table 2-3 lists all of the available analog I/O configurations for the Lab-PC-1200 and shows the configuration in reset condition.

Table 2-3. Analog I/O Settings, Lab-PC-1200

Parameter	Configuration
Analog Output CH0 Polarity	Bipolar—±5 V (reset condition) Unipolar—0 to 10 V
Analog Output CH1 Polarity	Bipolar—±5 V (reset condition) Unipolar—0 to 10 V

Table 2-3. Analog I/O Settings, Lab-PC-1200 (Continued)

Parameter	Configuration
Analog Input Polarity	Bipolar—±5 V (reset condition) Unipolar—0 to 10 V
Analog Input Mode	Referenced single-ended (RSE) (reset condition) Nonreferenced single-ended (NRSE) Differential (DIFF)

Both the analog input and analog output circuitry is software-configurable.

- Lab-PC-1200AI

  Upon power up or after a software reset, the Lab-PC-1200AI is set to the following configuration:

  - Referenced single-ended input mode
  - ±5 V analog input range (bipolar)

  Table 2-4 lists the available analog input configurations for the Lab-PC-1200AI and shows the configuration in reset condition.

Table 2-4. Analog Input Settings, Lab-PC-1200AI

Parameter	Configuration
Analog Input Polarity	Bipolar—±5 V (reset condition) Unipolar—0 to 10 V
Analog Input Mode	Referenced single-ended (RSE) (reset condition) Nonreferenced single-ended (NRSE) Differential (DIFF)

The analog input circuitry is completely software-configurable.

Analog Output Polarity

- Lab-PC-1200

  The Lab-PC-1200 has two analog output channels at the I/O connector. You can configure each analog output channel for either unipolar or bipolar output. A unipolar configuration has a range of 0 to 10 V at the analog output. A bipolar configuration has a range

of -5 to +5 V at the analog output. If you select a bipolar range, data values written to the analog output channel range from -2,048 to 2,047 (F800 hex to 7FF hex). If you select a unipolar range for a DAC, the data values written to the analog output channel range from 0 to 4,095 (0 to FFF hex).

Analog Input Polarity

You can select the analog input on the 1200 Series board for either a unipolar range (0 to 10 V) or a bipolar range (-5 to +5 V). If you select a bipolar range, -5 V input corresponds to F800 hex (-2,048 decimal) and +5 V corresponds to 7FF hex (2,047 decimal). If you select a unipolar mode, 0 V input corresponds to 0 hex, and +10 V corresponds to FFF hex (4,095 decimal).

Analog Input Mode

The 1200 Series boards have three different input modes—RSE input, NRSE input, and DIFF input. The single-ended input configurations use eight channels. The DIFF input configuration uses four channels. Table 2-5 describes these configurations.

Table 2-5. Analog Input Modes for the 1200 Series Boards

Analog Input Modes	Description
RSE	RSE mode provides eight single-ended inputs with the negative input of the instrumentation amplifier referenced to analog ground (reset condition).
NRSE	NRSE mode provides eight single-ended inputs with the negative input of the instrumentation amplifier tied to AISENSE/AIGND and not connected to ground.
DIFF	DIFF mode provides four differential inputs with the positive (+) input of the instrumentation amplifier tied to channels 0, 2, 4, or 6 and the negative (-) input tied to channels 1, 3, 5, or 7, respectively, thus choosing channel pairs (0, 1), (2, 3), (4, 5), or (6, 7).

While reading the following paragraphs, you may find it helpful to refer to the *Analog Input Signal Connections* section of Chapter 3, *Signal Connections*, which contains diagrams showing the signal paths for the three configurations.

RSE Input (Eight Channels, Reset Condition)

RSE input means that all input signals are referenced to a common ground point that is also tied to the 1200 Series board analog input ground. The differential amplifier negative input is tied to analog ground. The RSE configuration is useful for measuring floating signal sources. With this input configuration, your 1200 Series board can monitor eight different analog input channels.

Considerations for using the RSE configuration are discussed in Chapter 3, *Signal Connections*. Notice that in this mode, the signal return path is analog ground at the connector through the AISENSE/AIGND pin.

NRSE Input (Eight Channels)

NRSE input means that all input signals are referenced to the same common-mode voltage, which floats with respect to the board analog ground. This common-mode voltage is subsequently subtracted by the input instrumentation amplifier. The NRSE configuration is useful for measuring ground-referenced signal sources.

Considerations for using the NRSE configuration are discussed in Chapter 3, *Signal Connections*. Notice that in this mode, the signal return path is through the negative terminal of the amplifier at the connector through the AISENSE/AIGND pin.

DIFF Input (Four Channels)

DIFF input means that each input signal has its own reference, and the difference between each signal and its reference is measured. The signal and its reference are each assigned an input channel. With this input configuration, the 1200 Series board can monitor four differential analog input signals.

Considerations for using the DIFF configuration are discussed in Chapter 3, *Signal Connections*. Notice that the signal return path is through the amplifier's negative terminal and through channel 1, 3, 5, or 7, depending on which channel pair you select.

Chapter 3

Signal Connections

This chapter describes how to make input and output signal connections to the 1200 Series boards via the board I/O connector and details the I/O timing specifications.

The I/O connector for the 1200 Series boards has 50 pins that you can connect to 50-pin accessories.

I/O Connector

Figures 3-1 and 3-2 show the pin assignments for the 1200 Series board I/O connectors.



Warning: ***Connections that exceed any of the maximum ratings of input or output signals on the 1200 Series boards can damage your board and the computer. This includes connecting any power signals to ground and vice versa. National Instruments is NOT liable for any damages resulting from signal connections that exceed these maximum ratings.***

ACH0	1	2	ACH1
ACH2	3	4	ACH3
ACH4	5	6	ACH5
ACH6	7	8	ACH7
AISENSE/AIGND	9	10	DAC0OUT
AGND	11	12	DAC1OUT
DGND	13	14	PA0
PA1	15	16	PA2
PA3	17	18	PA4
PA5	19	20	PA6
PA7	21	22	PB0
PB1	23	24	PB2
PB3	25	26	PB4
PB5	27	28	PB6
PB7	29	30	PC0
PC1	31	32	PC2
PC3	33	34	PC4
PC5	35	36	PC6
PC7	37	38	EXTTRIG
EXTUPDATE*	39	40	EXTCONV*
OUTB0	41	42	GATB0
OUTB1	43	44	GATB1
CLKB1	45	46	OUTB2
GATB2	47	48	CLKB2
+5 V	49	50	DGND

Figure 3-1. Lab-PC-1200 I/O Connector Pin Assignments

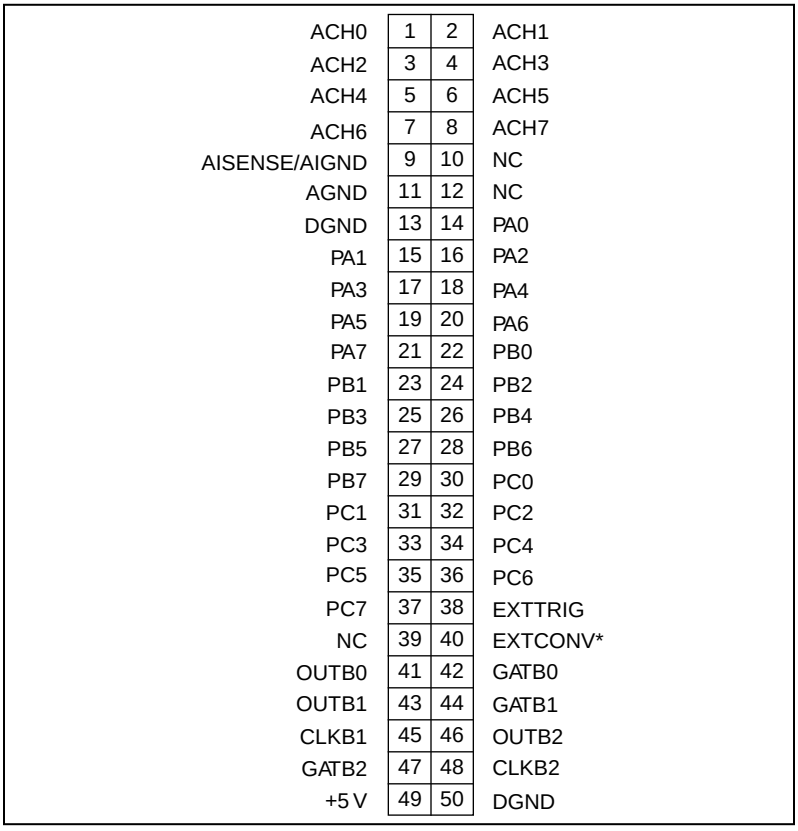


Figure 3-2. Lab-PC-1200AI I/O Connector Pin Assignments

I/O Connector Signal Descriptions

Table 3-1 lists the connector pins on the 1200 Series boards' I/O connectors by pin number and gives each signal name and signal connector pin description.

Table 3-1. Signal Descriptions for 1200 Series I/O Connector Pins

Pin	Signal Name	Direction	Reference	Description
1–8	ACH<0..7>	AI	AGND	Analog Channel 0 through 7—Analog input channels 0 through 7. Each channel pair, ACH (i, i + 1) <i = 0..6>, can be configured as either one differential input or two single-ended inputs.
9	AISENSE/AIGND	I/O	AGND	Analog Input Sense/Analog Input Ground—Connected to AGND in RSE mode, analog input sense in NRSE mode.
10	DAC0OUT NC	AO	AGND	Digital-to-Analog Converter 0 Output—(Lab-PC-1200 only). Voltage output signal for analog output channel 0. No Connect—(Lab-PC-1200AI only). This pin is a low impedance to ground.
11	AGND	N/A	N/A	Analog Ground—Analog output ground reference for analog output voltages. Bias current return point for differential measurements.
12	DAC1OUT NC	AO	AGND	Digital-to-Analog Converter 1 Output—(Lab-PC-1200 only). Voltage output signal for analog output channel 1. No Connect—(Lab-PC-1200AI only). This pin is a low impedance to ground.

Table 3-1. Signal Descriptions for 1200 Series I/O Connector Pins (Continued)

Pin	Signal Name	Direction	Reference	Description
13, 50	DGND	N/A	N/A	Digital Ground—Voltage ground reference for the digital signals and the +5 V supply.
14–21	PA<0..7>	DIO	DGND	Port A 0 through 7—Bidirectional data lines for port A. PA7 is the MSB, and PA0 is the LSB.
22–29	PB<0..7>	DIO	DGND	Port B 0 through 7—Bidirectional data lines for port B. PB7 is the MSB, and PB0 is the LSB.
30–37	PC<0..7>	DIO	DGND	Port C 0 through 7—Bidirectional data lines for port C. PC7 is the MSB, and PC0 is the LSB.
38	EXTTRIG	DI	DGND	External Trigger—External control signal to trigger a data acquisition operation.
39	EXTUPDATE* NC	DI	DGND	External Update—(Lab-PC-1200 only). External control signal to update DAC outputs. No Connect—(Lab-PC-1200AI only). This pin is not connected.
40	EXTCONV*	DIO	DGND	External Convert—External control signal to time A/D conversions (DI) and drive SCANCLK when you use SCXI (DO).
41	OUTB0	DO	DGND	Output B0—Digital output signal of counter B0.
42	GATB0	DI	DGND	Gate B0—External control signal for gating counter B0.
43	OUTB1	DIO	DGND	Output B1—Digital output signal of counter B1 (DO). External control signal for timing a scan interval (DI).

Table 3-1. Signal Descriptions for 1200 Series I/O Connector Pins (Continued)

Pin	Signal Name	Direction	Reference	Description
44	GATB1	DI	DGND	Gate B1—External control signal for gating counter B1.
45	CLKB1	DI	DGND	Clock B1—External control clock signal for counter B1.
46	OUTB2	DO	DGND	Counter B2—Digital output signal of counter B2.
47	GATB2	DI	DGND	Gate B2—External control signal for gating counter B2.
48	CLKB2	DI	DGND	Clock B2—External control clock signal for counter B2.
49	+5 V	DO	DGND	+5 Volts—This pin is fused for up to 1 A of +4.65 to +5.25 V.

*Indicates that the signal is active low.

AI = Analog Input DI = Digital Input DIO = Digital Input/Output NC = Not Connected
AO = Analog Output DO = Digital Output N/A = Not Applicable

The connector pins are grouped into analog input signal pins, analog output signal pins, digital I/O signal pins, timing I/O signal pins, and power connections. The following sections describe the signal connection guidelines for each of these groups.

Analog Input Signal Connections

Pins 1 through 8 are analog input signal pins for your 1200 Series board 12-bit ADC. Pin 9, AISENSE/AIGND, is an analog common signal. You can use this pin for a general analog power ground tie to the 1200 Series board in RSE mode or as a return path in NRSE mode. Pin 11, AGND, is the bias current return point for differential measurements. Pins 1 through 8 are tied to the eight single-ended analog input channels of the input multiplexer through 4.7 kΩ series resistors. Pins 2, 4, 6, and 8 are also tied to an input multiplexer for DIFF mode.

The signal ranges for inputs ACH<0..7> at all possible gains are shown in Tables 3-2 and 3-3. Exceeding the input signal range will not damage the input circuitry as long as you don't exceed the maximum powered-on input voltage rating of ±35 V or the powered-off voltage rating of ±25 V. The 1200 Series board is guaranteed to withstand inputs up to the maximum input voltage rating.



Warning: ***Exceeding the input signal range, even on unused analog input channels, distorts input signals. Exceeding the maximum input voltage rating can damage the 1200 Series board and the computer. National Instruments is NOT liable for any damages resulting from such signal connections.***

Table 3-2. Bipolar Analog Input Signal Range Versus Gain

Gain Setting	Input Signal Range
1	-5.0 to 4.99756 V
2	-2.5 to 2.49878 V
5	-1.0 to 0.99951 V
10	-500 to 499.756 mV
20	-250 to 249.877 mV
50	-100 to 99.951 mV
100	-50 to 49.975 mV

Table 3-3. Unipolar Analog Input Signal Range Versus Gain

Gain Setting	Input Signal Range
1	0 to 9.99756 V
2	0 to 4.99878 V
5	0 to 1.99951 V
10	0 to 999.756 mV
20	0 to 499.877 mV

Table 3-3. Unipolar Analog Input Signal Range Versus Gain (Continued)

Gain Setting	Input Signal Range
50	0 to 199.951 mV
100	0 to 99.975 mV

How you connect analog input signals to your 1200 Series board depends on how you configure the board's analog input circuitry and the type of input signal source. With different board configurations, you can use the 1200 Series instrumentation amplifier in different ways. Figure 3-3 shows a diagram of the 1200 Series instrumentation amplifier.

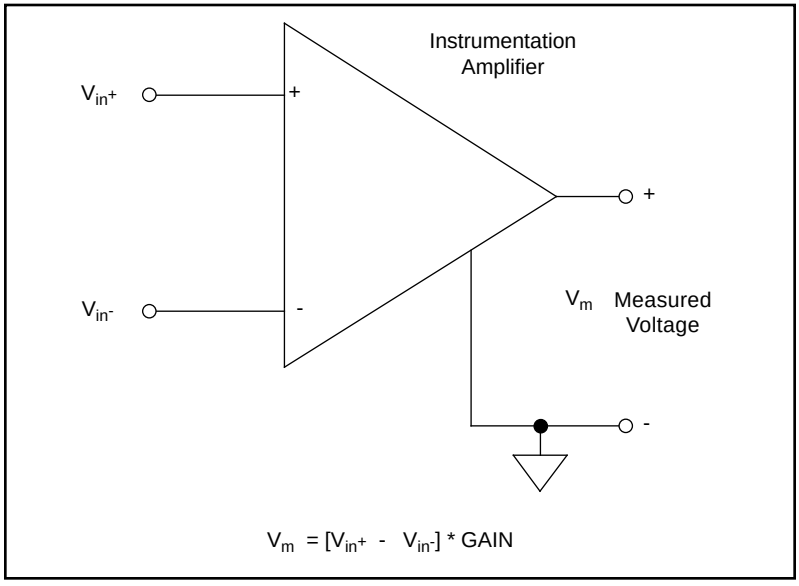


Figure 3-3. 1200 Series Instrumentation Amplifier

The instrumentation amplifier applies gain, common-mode voltage rejection, and high-input impedance to the analog input signals connected to the 1200 Series board. Signals are routed to the positive and negative inputs of the instrumentation amplifier through input multiplexers on the board. The instrumentation amplifier converts two input signals to a signal that is the difference between the two input signals multiplied by the gain setting of the amplifier. The amplifier

output voltage is referenced to the board ground. The 1200 Series ADC measures this output voltage when it performs A/D conversions.

All signals must be referenced to ground, either at the source device or at the 1200 Series board. If you have a floating source, you must use a ground-referenced input connection at the board. If you have a grounded source, you must use a nonreferenced input connection at the board.

Types of Signal Sources

When configuring the input mode of the 1200 Series and making signal connections, first determine whether the signal source is floating or ground referenced. These two types of signals are described in the following sections.

Floating Signal Sources

A floating signal source does not connect in any way to earth ground but has an isolated ground-reference point. Some examples of floating signal sources are transformer outputs, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. Tie the ground reference of a floating signal to the 1200 Series board analog input ground to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies or appears to float. An instrument or device that supplies an isolated output falls into the floating signal source category.

Ground-Referenced Signal Sources

A ground-referenced signal source connects in some way to earth ground and is, therefore, already connected to a common ground point with respect to the 1200 Series board, if the computer is plugged into the same power supply. Nonisolated outputs of instruments and devices that plug into the power supply fall into this category.

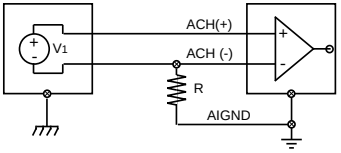
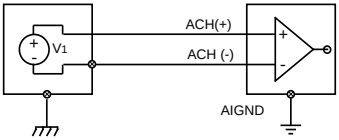
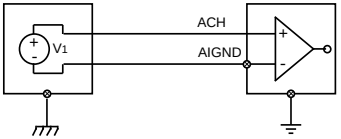
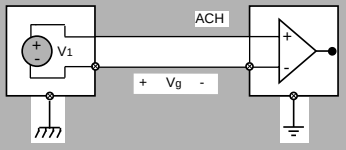
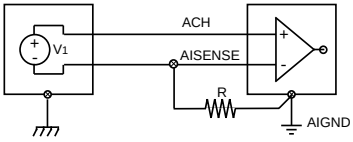
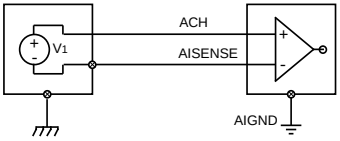
The difference in ground potential between two instruments connected to the same power supply is typically between 1 and 100 mV but can be much higher if power distribution circuits are not properly connected. The connection instructions that follow for grounded signal sources eliminate this ground potential difference from the measured signal.

☞ **Note:** ***If you power both the 1200 Series board and your computer with a floating power source (such as a battery), your system may be floating with respect to earth ground. In this case, treat all of your signal sources as floating sources.***

Input Configurations

You can configure the 1200 Series for one of three input modes—RSE, NRSE, or DIFF. The following sections discuss the use of single-ended and differential measurements, and considerations for measuring both floating and ground-referenced signal sources. Table 3-4 summarizes the recommended input configurations for both types of signal sources.

Table 3-4. Summary of Analog Input Connections

Input	Signal Source Type	
	Floating Signal Source (Not Connected to Earth Ground)	**Grounded Signal Source**
	Examples • Ungrounded thermocouples • Signal conditioning with isolated outputs • Battery devices	Examples • Plug-in instruments with nonisolated outputs
Differential (DIFF)	 See text for information on bias resistors.	
Referenced Single-Ended Ground (RSE)		NOT RECOMMENDED  Ground-loop losses, V_g, are added to measured signal
Nonreferenced Single-Ended (NRSE)	 See text for information on bias resistors.	

Differential Connection Considerations (DIFF Configuration)

Differential connections are those in which each 1200 Series analog input signal has its own reference signal or signal return path. These connections are available when you configure the 1200 Series board in the DIFF mode. Each input signal is tied to the positive input of the instrumentation amplifier, and its reference signal, or return, is tied to the negative input of the instrumentation amplifier.

When configuring the 1200 Series for DIFF input, each signal uses two of the multiplexer inputs—one for the signal and one for its reference signal. Therefore, only four analog input channels are available when using the DIFF configuration. Use the DIFF input configuration when your DAQ system has any of the following conditions:

- Input signals are low level (less than 1 V).
- Leads connecting the signals to the 1200 Series board are greater than 10 ft.
- Any of the input signals require a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce picked-up noise and increase common-mode signal and noise rejection. With these connections, input signals can float within the common-mode limits of the input instrumentation amplifier.

Differential Connections for Ground-Referenced Signal Sources

Figure 3-4 shows how to connect a ground-referenced signal source to a 1200 Series board configured for DIFF input. Configuration instructions are in the *Analog I/O Configuration* section in Chapter 2, *Installation and Configuration*.

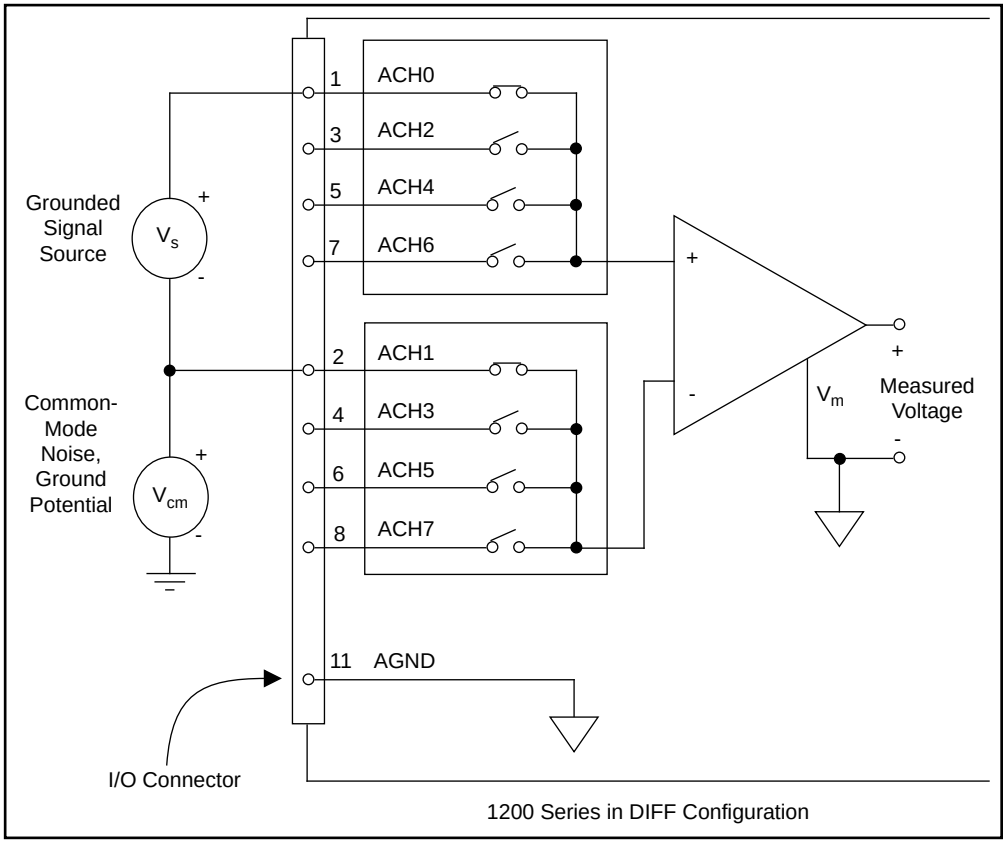


Figure 3-4. Differential Input Connections for Grounded Signal Sources

With this type of connection, the instrumentation amplifier rejects both the common-mode noise in the signal and the ground-potential difference between the signal source and the 1200 Series ground (shown as V_{cm} in Figure 3-4).

Differential Connections for Nonreferenced or Floating Signal Sources

Figure 3-5 shows how to connect a floating signal source to a 1200 Series board configured for DIFF input. Configuration instructions are in the *Analog I/O Configuration* section in Chapter 2, *Installation and Configuration*.

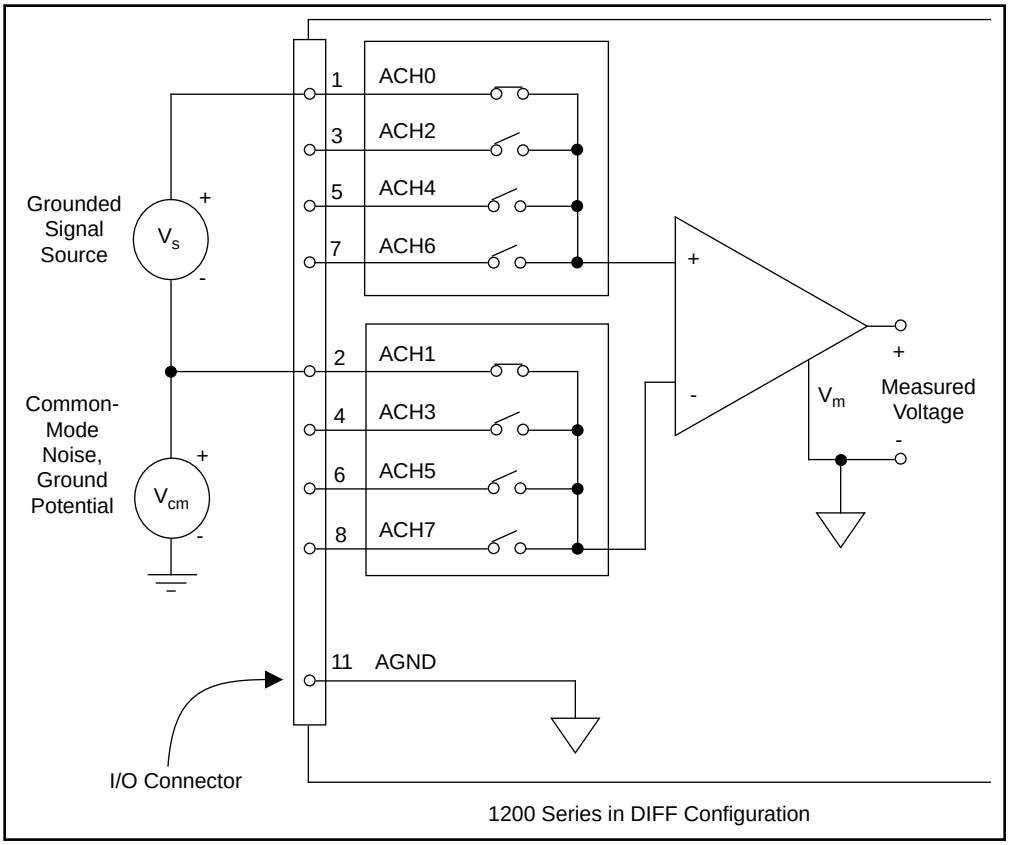


Figure 3-5. Differential Input Connections for Floating Sources

The 100 kΩ resistors shown in Figure 3-5 create a return path to ground for the bias currents of the instrumentation amplifier. If there is no return path, the instrumentation amplifier bias currents charge stray capacitances, resulting in uncontrollable drift and possible saturation in the amplifier. Typically, values from 10 to 100 kΩ are used.

A resistor from each input to ground, as shown in Figure 3-5, provides bias current return paths for an AC-coupled input signal.

If the input signal is DC-coupled, you need only the resistor that connects the negative signal input to ground. This connection does not lower the input impedance of the analog input channel.

Single-Ended Connection Considerations

Single-ended connections are those in which all 1200 Series analog input signals are referenced to one common ground. The input signals are tied to the positive input of the instrumentation amplifier, and their common ground point is tied to the negative input of the instrumentation amplifier.

When you configure the 1200 Series board for single-ended input (NRSE or RSE), eight analog input channels are available. Use single-ended input connections when all of the input signals meet the following conditions:

- Input signals are high level (greater than 1 V).
- Leads connecting the signals to the 1200 Series board are less than 10 ft.
- All input signals share a common reference signal (at the source).

If any of the preceding criteria is not met, use the DIFF input configuration.

You can software-configure the 1200 Series boards for two different types of single-ended connections, RSE configuration and NRSE configuration. Use the RSE configuration for floating signal sources; in this case, the 1200 Series boards provide the reference ground point for the external signal. Use the NRSE configuration for ground-referenced signal sources; in this case, the external signal supplies its own reference ground point and the 1200 Series boards should not supply one.

Single-Ended Connections for Floating Signal Sources (RSE Configuration)

Figure 3-6 shows how to connect a floating signal source to a 1200 Series board configured for RSE mode. Configure the 1200 Series analog input circuitry for RSE input to make these types of connections. Configuration instructions are in the *Analog I/O Configuration* section of Chapter 2, *Installation and Configuration*.

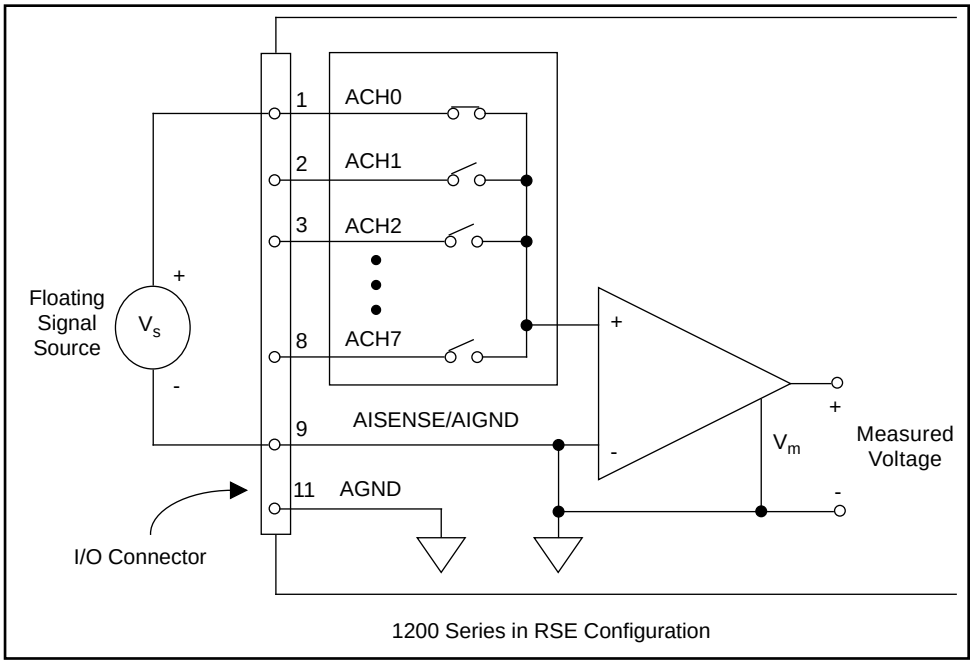


Figure 3-6. Single-Ended Input Connections for Floating Signal Sources

Single-Ended Connections for Grounded Signal Sources (NRSE Configuration)

If you measure a grounded signal source with a single-ended configuration, configure the 1200 Series in the NRSE input configuration. The signal connects to the positive input of the 1200 Series instrumentation amplifier, and the signal local ground reference connects to the negative input of the 1200 Series instrumentation amplifier. Therefore, connect the ground point of the signal to the AISENSE pin. Any potential difference between the 1200 Series ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the instrumentation amplifier and is, therefore, rejected by the amplifier. On the other hand, if the input circuitry of the 1200 Series is referenced to ground, such as in the RSE configuration, this difference in ground potentials appears as an error in the measured voltage.

Figure 3-7 shows how to connect a grounded signal source to a 1200 Series board configured in the NRSE configuration.

Configuration instructions are in the *Analog I/O Configuration* section of Chapter 2, *Installation and Configuration*.

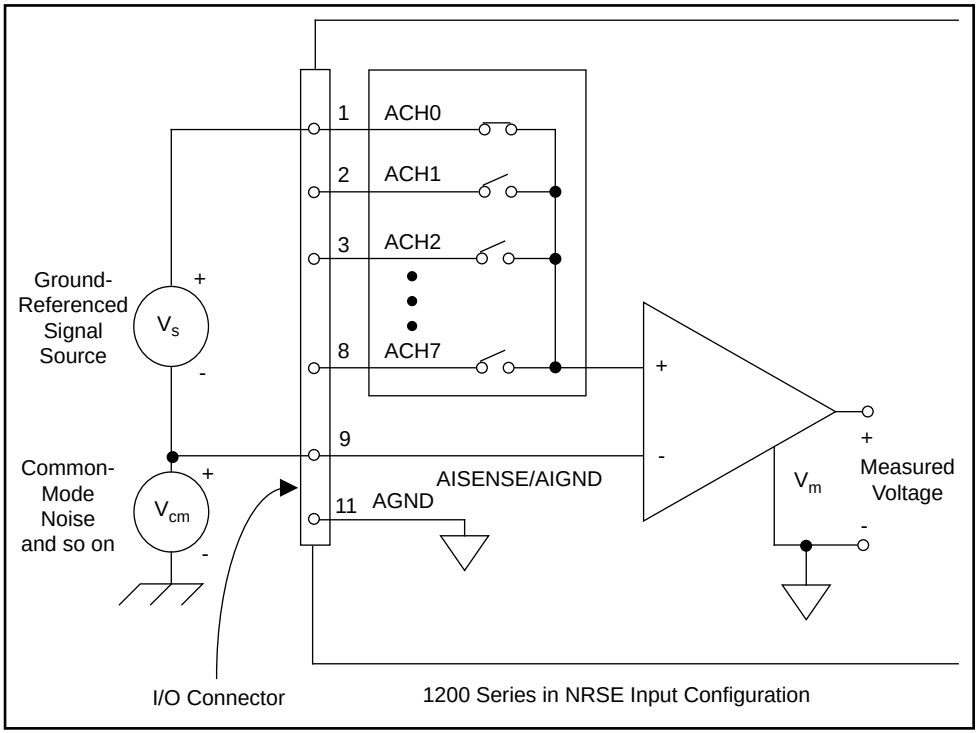


Figure 3-7. Single-Ended Input Connections for Grounded Signal Sources

Common-Mode Signal Rejection Considerations

Figures 3-5 and 3-7 show connections for signal sources that are already referenced to some ground point with respect to the 1200 Series. In these cases, the instrumentation amplifier can reject any voltage caused by ground-potential differences between the signal source and the 1200 Series board. In addition, with differential input connections, the instrumentation amplifier can reject common-mode noise pickup in the leads connecting the signal sources to the 1200 Series board.

The common-mode input range of the instrumentation amplifier is the magnitude of the greatest common-mode signal that it can reject.

The common-mode input range for the 1200 Series depends on the size of the differential input signal ($V_{diff} = V+_{in} - V-_{in}$) and the gain setting

of the instrumentation amplifier. In unipolar mode, the differential input range is 0 to 10 V. In bipolar mode, the differential input range is -5 to +5 V. In differential or NRSE mode, the negative input /AISENSE should remain within ±5 V (bipolar input range) or -5 to +2 V (unipolar input range) of AGND. The positive input should remain within -5 V to +10 V of AGND.

Analog Output Signal Connections

- Lab-PC-1200

  Pins 10 through 12 on the I/O connector are analog output signal pins.

  Pins 10 and 12 are the DAC0OUT and DAC1OUT signal pins. DAC0OUT is the voltage output signal for analog output channel 0. DAC1OUT is the voltage output signal for analog output channel 1.

  Pin 11, AGND, is the ground-reference point for both analog output channels as well as analog input.

  The following output ranges are available:

  - Output signal range
    - Bipolar output ±5 V*
    - Unipolar output 0 to 10 V*

  *Maximum load current ±2 mA for 12-bit linearity

  Figure 3-8 shows how to make analog output signal connections.

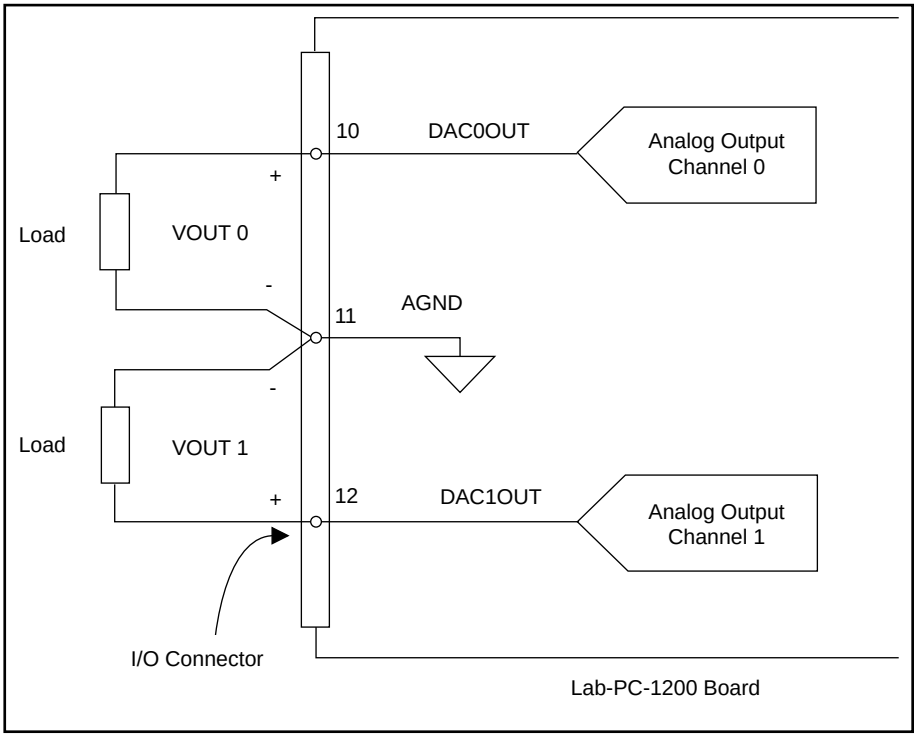


Figure 3-8. Analog Output Signal Connections

Digital I/O Signal Connections

Pins 13 through 37 of the I/O connector are digital I/O signal pins. Digital I/O on the 1200 Series boards uses the 82C55A integrated circuit. The 82C55A is a general-purpose peripheral interface containing 24 programmable I/O pins. These pins represent the three 8-bit ports (PA, PB, and PC) of the 82C55A.

Pins 14 through 21 are connected to the digital lines PA<0..7> for digital I/O port A. Pins 22 through 29 are connected to the digital lines PB<0..7> for digital I/O port B. Pins 30 through 37 are connected to the digital lines PC<0..7> for digital I/O port C. Pin 13, DGND, is the digital ground pin for all three digital I/O ports. Refer to Appendix A, *Specifications*, for signal voltage and current specifications.

The logical input and output specifications and ratings apply to the digital I/O lines. All voltages are with respect to DGND.

Logical Input and Output

- Absolute maximum voltage rating: -0.5 to +5.5 V with respect to DGND
- Digital I/O lines:
  - Input logic low voltage: -0.3 V min, 0.8 V max
  - Input logic high voltage: 2.2 V min, 5.3 V max
  - Output logic low voltage (at output sink current = 2.5 mA): — , 0.4 V max
  - Output logic high voltage (at output source current = -2.5 mA): 3.7 V min, —
  - Input leakage current ($0 < V_{in} < 5$ V): -1 μA min, 1 μA max

Figure 3-9 illustrates signal connections for three typical digital I/O applications.

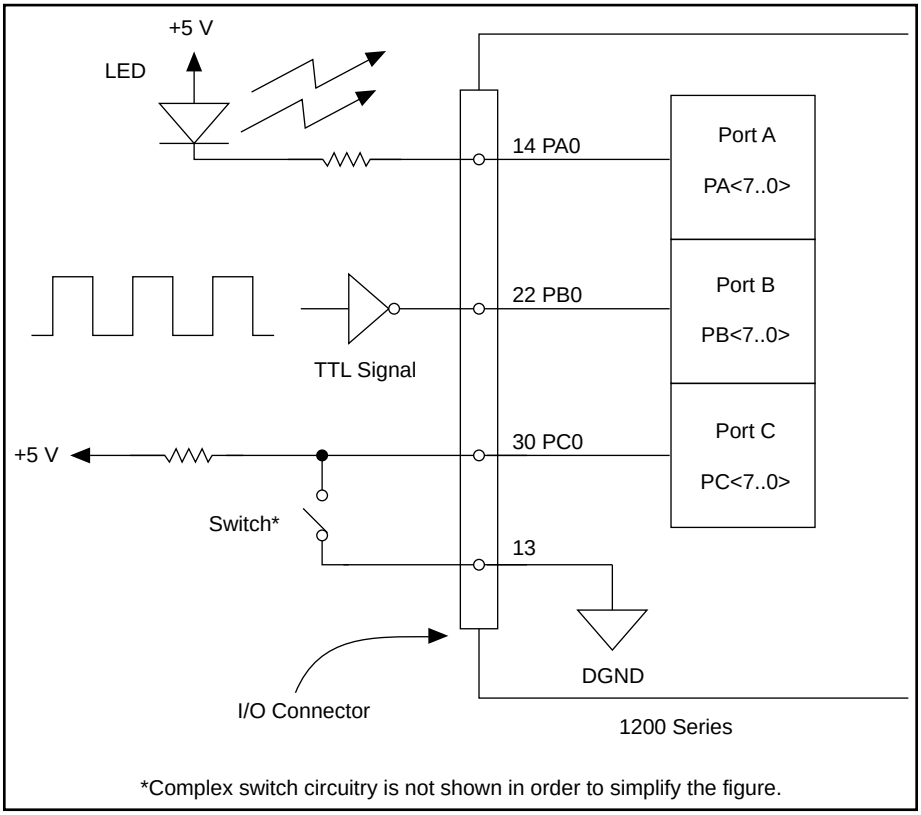


Figure 3-9. Digital I/O Connections

In Figure 3-9, port A is configured for digital output, and ports B and C are configured for digital input. Digital input applications include receiving TTL signals and sensing external device states such as the switch in Figure 3-9. Digital output applications include sending TTL signals and driving external devices such as the LED shown in Figure 3-9.

Port C Pin Connections

The signals assigned to port C depend on the mode in which the 82C55A is programmed. In mode 0, port C is considered to be two 4-bit I/O ports. In modes 1 and 2, port C is used for status and handshaking signals with two or three I/O bits mixed in. Table 3-5 summarizes the signal assignments of port C for each programmable mode.

Table 3-5. Port C Signal Assignments

Programmable Mode	Group A					Group B		
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Mode 0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Mode 1 Input	I/O	I/O	IBF_A	STB_A*	$INTR_A$	STB_B*	$IBFB_B$	$INTR_B$
Mode 1 Output	OBF_A*	ACK_A*	I/O	I/O	$INTR_A$	ACK_B*	OBF_B*	$INTR_B$
Mode 2	OBF_A*	ACK_A*	IBF_A	STB_A*	$INTR_A$	I/O	I/O	I/O
*Indicates that the signal is active low.								

Timing Specifications

Use the handshaking lines STB* and IBF to synchronize input transfers. Use the handshaking lines OBF* and ACK* to synchronize output transfers.

Table 3-6 lists the signals used in the timing diagrams shown later in this chapter.

Table 3-6. Port C Signal Descriptions

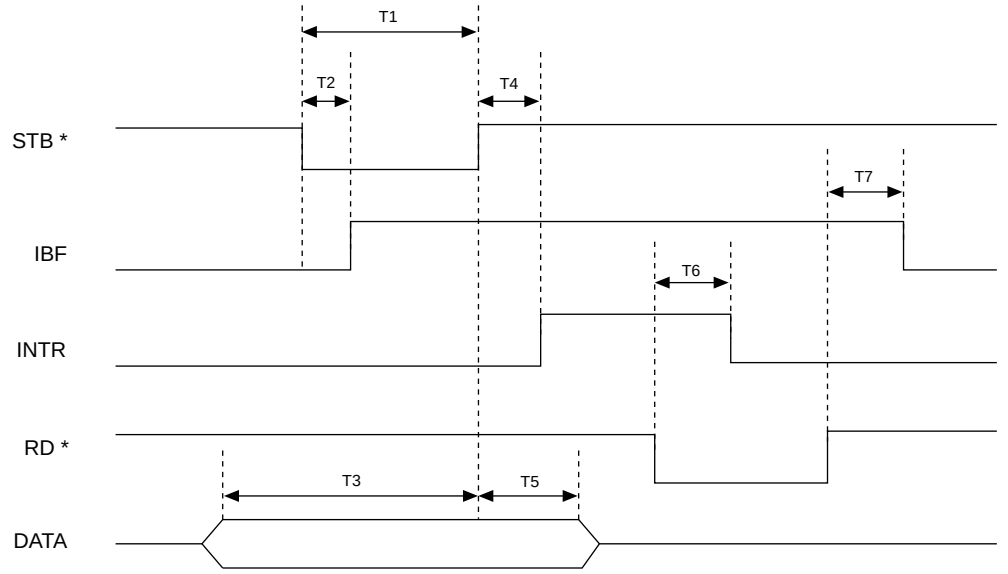
Name	Type	Description
STB*	Input	Strobe Input—A low signal on this handshaking line loads data into the input latch.
IBF	Output	Input Buffer Full—A high signal on this handshaking line indicates that data has been loaded into the input latch. This is primarily an input acknowledge signal.
ACK*	Input	Acknowledge Input—A low signal on this handshaking line indicates that the data written from the specified port has been accepted. This signal is primarily a response from the external device that it has received the data from the 1200 Series.
OBF*	Output	Output Buffer Full—A low signal on this handshaking line indicates that data has been written from the specified port.

Table 3-6. Port C Signal Descriptions (Continued)

Name	Type	Description
INTR	Output	Interrupt Request—This signal becomes high when the 82C55A is requesting service during a data transfer. Set the appropriate interrupt enable signals to generate this signal.
RD*	Internal	Read Signal—This signal is the read signal generated from the interface circuitry.
WRT*	Internal	Write Signal—This signal is the write signal generated from the interface circuitry.
DATA	Bidirectional	Data Lines at the Specified Port—This signal indicates when the data on the data lines at a specified port is or should be available.

Mode 1 Input Timing

The timing specifications for an input transfer in mode 1 are as follows:



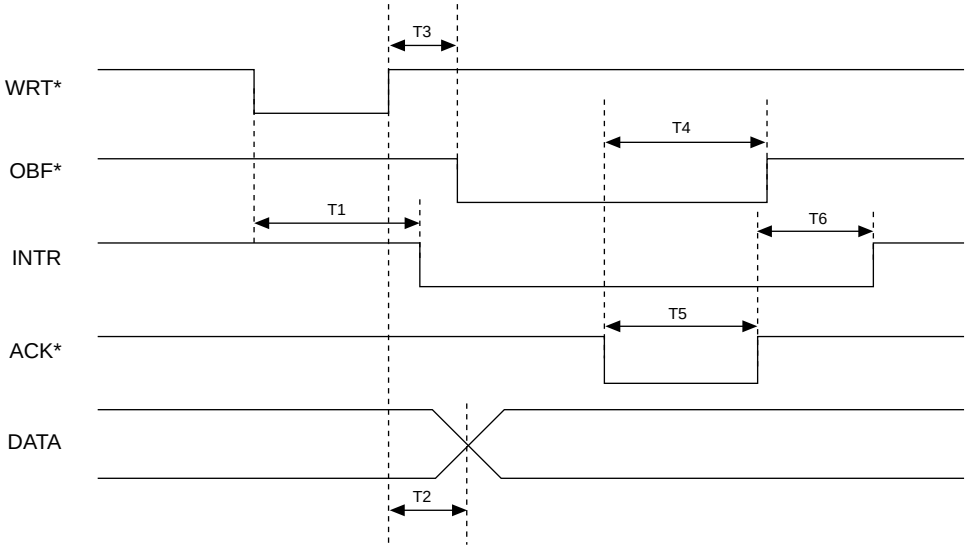
Name	Description	Minimum	Maximum
T1	STB* pulse width	500	—
T2	STB* = 0 to IBF = 1	—	300
T3	Data before STB* = 1	0	—
T4	STB* = 1 to INTR = 1	—	300
T5	Data after STB* = 1	180	—
T6	RD* = 0 to INTR = 0	—	400
T7	RD* = 1 to IBF = 0	—	300

All timing values are in nanoseconds.

Figure 3-10. Mode 1 Timing Specifications for Input Transfers

Mode 1 Output Timing

The timing specifications for an output transfer in mode 1 are as follows:



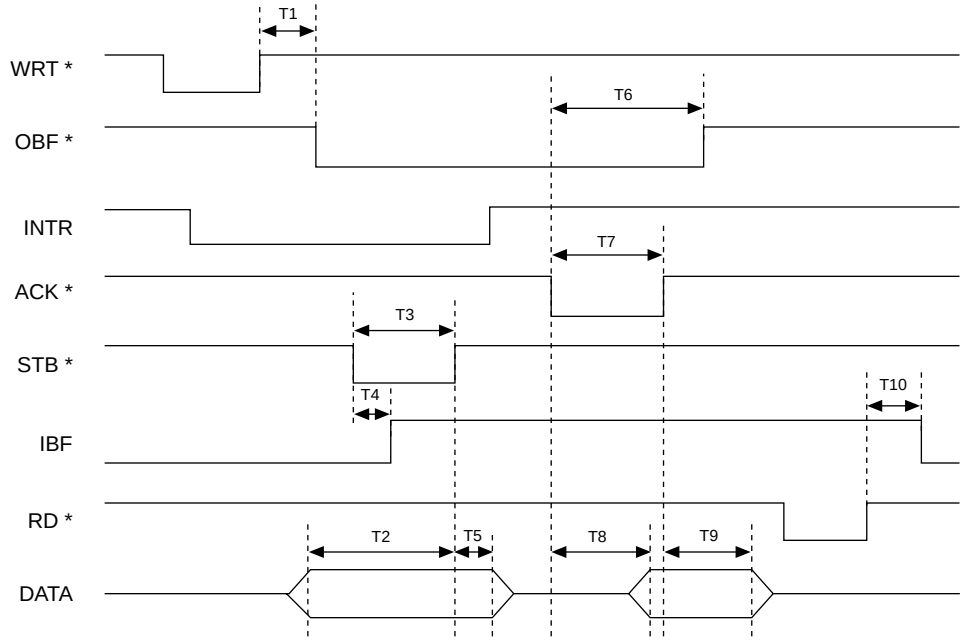
Name	Description	Minimum	Maximum
T1	WRT* = 0 to INTR = 0	—	450
T2	WRT* = 1 to output	—	350
T3	WRT* = 1 to OBF* = 0	—	650
T4	ACK* = 0 to OBF* = 1	—	350
T5	ACK* pulse width	300	—
T6	ACK* = 1 to INTR = 1	—	350

All timing values are in nanoseconds.

Figure 3-11. Mode 1 Timing Specifications for Output Transfers

Mode 2 Bidirectional Timing

The timing specifications for bidirectional transfers in mode 2 are as follows:



Name	Description	Minimum	Maximum
T1	WRT* = 1 to OBF* = 0	—	650
T2	Data before STB* = 1	0	—
T3	STB* pulse width	500	—
T4	STB* = 0 to IBF = 1	—	300
T5	Data after STB* = 1	180	—
T6	ACK* = 0 to OBF = 1	—	350
T7	ACK* pulse width	300	—
T8	ACK* = 0 to output	—	300
T9	ACK* = 1 to output float	20	250
T10	RD* = 1 to IBF = 0	—	300

All timing values are in nanoseconds.

Figure 3-12. Mode 2 Timing Specification for Bidirectional Transfers

Data Acquisition and General-Purpose Timing Signal Connections

Pins 38 through 48 of the I/O connector are connections for timing I/O signals. The 1200 Series timing input/output circuitry uses two 82C53 counter/timer integrated circuits. One counter, the 82C53(A), is used exclusively for data acquisition timing, and the other, 82C53(B), is available for general use. Use pins 38 through 40 and pin 43 to carry external signals for data acquisition timing. These signals are explained in the *Data Acquisition Timing Connections* section. Pins 41 through 48 carry general-purpose timing signals from 82C53(B). These signals are explained in the *General-Purpose Timing Signal Connections* section later in this chapter.

Data Acquisition Timing Connections

Each 82C53 counter/timer circuit contains three counters. Counter 0 on the 82C53(A) counter/timer, referred to as A0, is a sample-interval counter in timed A/D conversions. Counter 1 on the 82C53(A) counter/timer, referred to as A1, is a sample counter in controlled A/D conversions. Therefore, counter A1 stops data acquisition after a predefined number of samples. These counters are not available for general use.

Instead of counter A0, you can use EXTCONV* to externally time conversions. Figure 3-13 shows the timing requirements for the EXTCONV* input. An A/D conversion is initiated by a falling edge on EXTCONV*. EXTCONV* can also be configured as an output and used as a strobe signal for SCXI through NI-DAQ or LabVIEW.

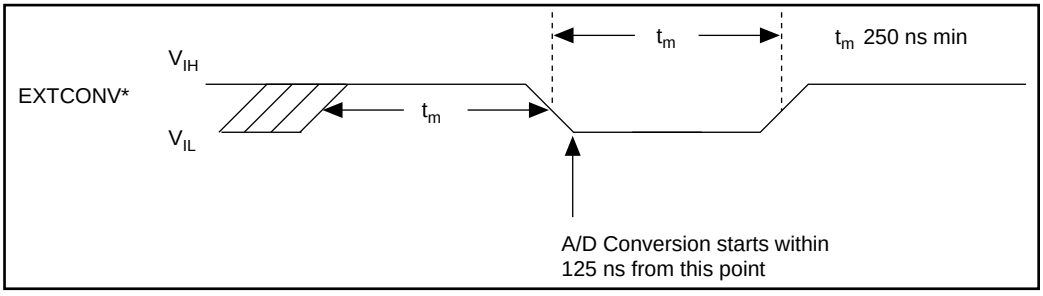


Figure 3-13. EXTCONV* Signal Timing

The external control signal EXTTRIG can either start a data acquisition sequence or terminate an ongoing data acquisition sequence depending on the mode—posttrigger (POSTTRIG) or pretrigger (PRETRIG). These modes are software-selectable.

In the POSTTRIG mode, EXTTRIG serves as an external trigger that initiates a data acquisition sequence. When you use counter A0 to time sample intervals, a rising edge on EXTTRIG starts counter A0 and the data acquisition sequence. When you use EXTCONV* to time sample intervals, the data acquisition starts on a rising edge of EXTTRIG followed by a rising edge on EXTCONV*. The first conversion occurs on the next falling edge of EXTCONV*. Further transitions on the EXTTRIG line have no effect until a new data acquisition sequence is established.

Figure 3-14 shows a possible controlled data acquisition sequence using EXTCONV* and EXTTRIG. The rising edge of EXTCONV* that enables external conversions must occur a minimum of 50 ns after the rising edge of EXTTRIG. The first conversion occurs on the next falling edge of EXTCONV*.

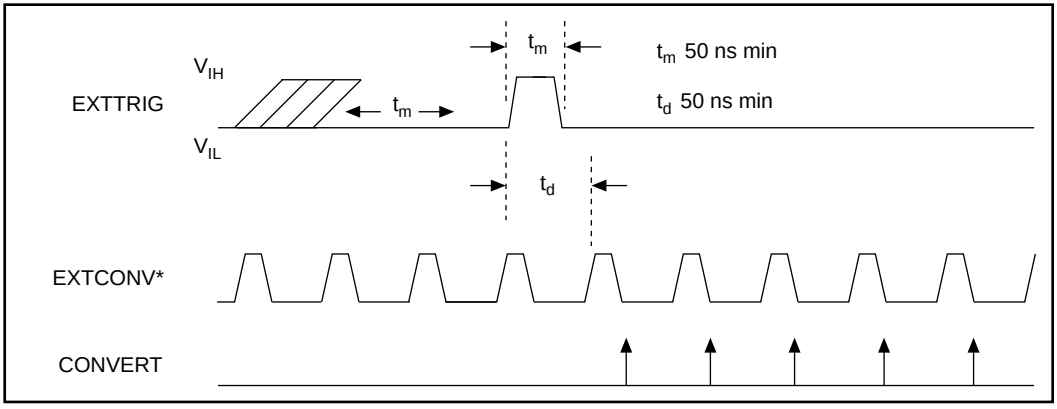


Figure 3-14. Posttrigger Data Acquisition Timing

In the PRETRIG mode, EXTTRIG serves as a pretrigger signal. Data is acquired both before and after the EXTTRIG signal occurs. A/D conversions are software enabled, which initiates the data acquisition operation. However, the sample counter is not started until a rising edge is sensed on the EXTTRIG input. Conversions remain enabled until the sample counter counts to zero. The maximum number of samples acquired after the stop trigger is limited to 65,535. The number of samples acquired before the trigger is limited only by the size of the memory buffer available for data acquisition.

Figure 3-15 shows a pretrigger data acquisition timing sequence using EXTTRIG and EXTCONV*. The data acquisition operation has been initiated through software. Notice that the sample counter has been

programmed to allow five conversions after the rising edge on the EXTTRIG signal. Additional transitions on the EXTTRIG line have no effect until you initiate a new data acquisition sequence.

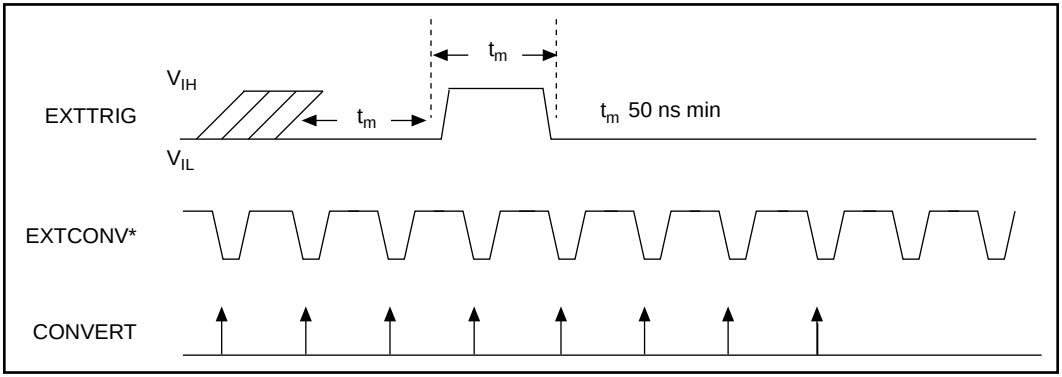


Figure 3-15. Pretrigger Data Acquisition Timing

Because both pretrigger and posttrigger modes use EXTTRIG input, you can only use one mode at a time.

For interval scanning data acquisition, counter B1 determines the scan interval. Instead of using counter B1, you can externally time the scan interval through OUTB1. If you externally time the sample interval, you should also externally time the scan interval.

Figure 3-16 shows an example of an interval scanning data acquisition operation. The scan interval and the sample interval are being timed externally through OUTB1 and EXTCONV*. Channels 1 and 0 of the input multiplexers are being scanned once during each scan interval. The first rising edge of EXTCONV* must occur a minimum of 50 ns after the rising edge on OUTB1. The first rising edge of EXTCONV* after the rising edge of OUTB1 enables an internal GATE signal that allows conversions to occur. The first conversion then occurs on the following falling edge of EXTCONV*. The GATE signal disables conversions for the rest of the scan interval after the desired channels have been scanned. Refer to the *Interval-Scanning Acquisition Mode* section in Chapter 4, *Theory of Operation*, for more information on interval scanning.

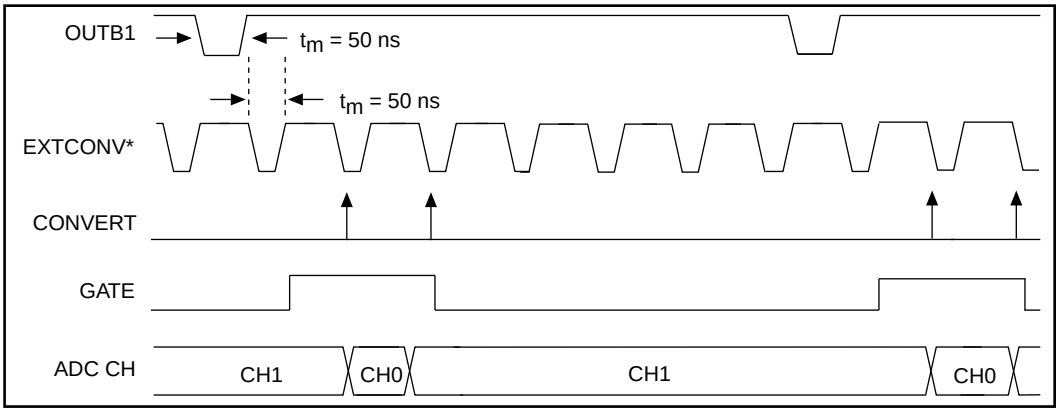


Figure 3-16. Interval-Scanning Signal Timing

- Lab-PC-1200

  Only the Lab-PC-1200 uses the EXTUPDATE* signal. It externally controls updating the output voltage of the 12-bit DACs and/or generates an externally timed interrupt. There are two update modes, immediate update and delayed update. In immediate update mode the analog output is updated as soon as a value is written to the DAC. If you select the delayed update mode, a value is written to the DAC; however, the corresponding DAC voltage is not updated until a low level on the EXTUPDATE* signal is sensed. Furthermore, if you enable interrupt generation, an interrupt is generated whenever a rising edge is detected on the EXTUPDATE* bit. Therefore, you can perform externally timed, interrupt-driven waveform generation on the Lab-PC-1200. The EXTUPDATE* line is susceptible to noise caused by switching lines and could generate false interrupts. The width of the EXTUPDATE* pulse should, therefore, be as short as possible, but greater than 50 ns.

Figure 3-17 illustrates a waveform generation timing sequence using the EXTUPDATE* signal and the delayed update mode. The DACs are updated by a high level on the DAC OUTPUT UPDATE signal, which in this case is triggered by a low level on the EXTUPDATE* line. The CNTINT signal interrupts the computer. The rising edge of EXTUPDATE* generates this interrupt. DACWRT is the signal that writes a new value to the DAC.

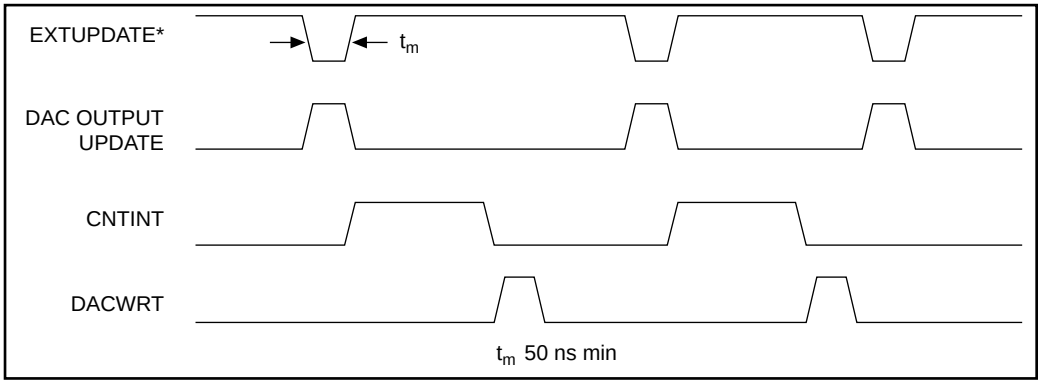


Figure 3-17. EXTUPDATE* Signal Timing for Updating DAC Output

The following rating applies to the EXTCONV*, EXTTRIG, OUTB1, and EXTUPDATE* signals.

- Absolute maximum voltage input rating — -0.5 to 5.5 V with respect to DGND

For more information concerning the various modes of data acquisition and analog output, refer to your NI-DAQ documentation or to Chapter 4, *Theory of Operation*, in this manual.

General-Purpose Timing Signal Connections

The general-purpose timing signals include the GATE, CLK, and OUT signals for the three 82C53(B) counters. The 82C53 counter/timers can be used for the 1200 Series board general-purpose applications such as pulse and square wave generation, event counting, and pulse-width, time-lapse, and frequency measurement. For these applications, the CLK and GATE signals at the I/O connector control the counters. The single exception is counter B0, which has an internal 2 MHz clock.

To perform pulse and square wave generation, program a counter to generate a timing signal at its OUT output pin. To perform event counting, program a counter to count rising or falling edges applied to any of the 82C53 CLK inputs, then read the counter value to determine the number of edges that have occurred. You can enable or disable the counting operation by controlling the gate input. Figure 3-18 shows connections for a typical event-counting operation in which a switch gates the counter on and off.

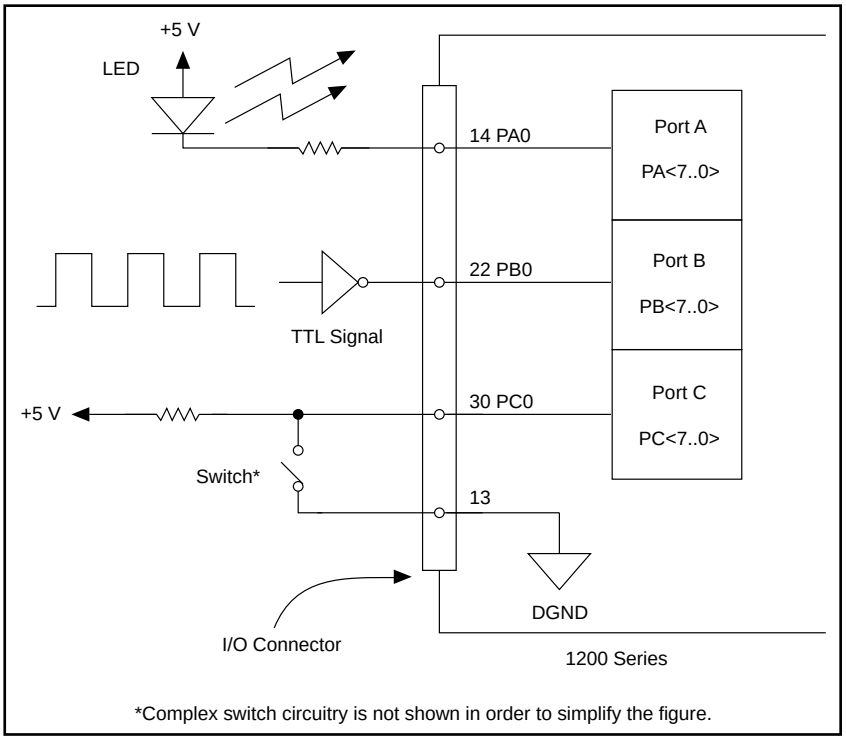


Figure 3-18. Event-Counting Application with External Switch Gating

Level gating performs pulse-width measurement. The pulse you want to measure is applied to the counter GATE input. Load the counter with the known count and program it to count down while the signal at the GATE input is high. The pulse width equals the counter difference (loaded value minus read value) multiplied by the CLK period.

Perform time-lapse measurement by programming a counter to be edge gated. Apply an edge to the counter GATE input to start the counter. Program the counter to start counting after receiving a low-to-high edge. The time lapse since receiving the edge equals the counter value difference (loaded value minus read value) multiplied by the CLK period.

To perform frequency measurement, program a counter to be level gated and count the number of falling edges in a signal applied to a CLK input. The gate signal applied to the counter GATE input is of known duration. In this case, program the counter to count falling edges at the CLK input while the gate is applied. The frequency of the input signal

then equals the count value divided by the gate period. Figure 3-19 shows the connections for a frequency measurement application. You can also use a second counter to generate the gate signal in this application. If you use a second counter, however, you must externally invert the signal.

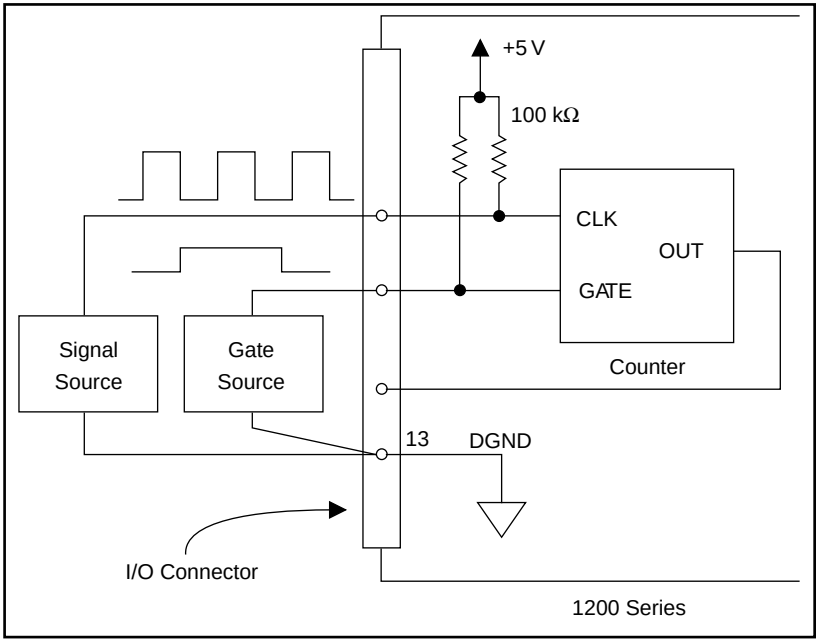


Figure 3-19. Frequency Measurement Application

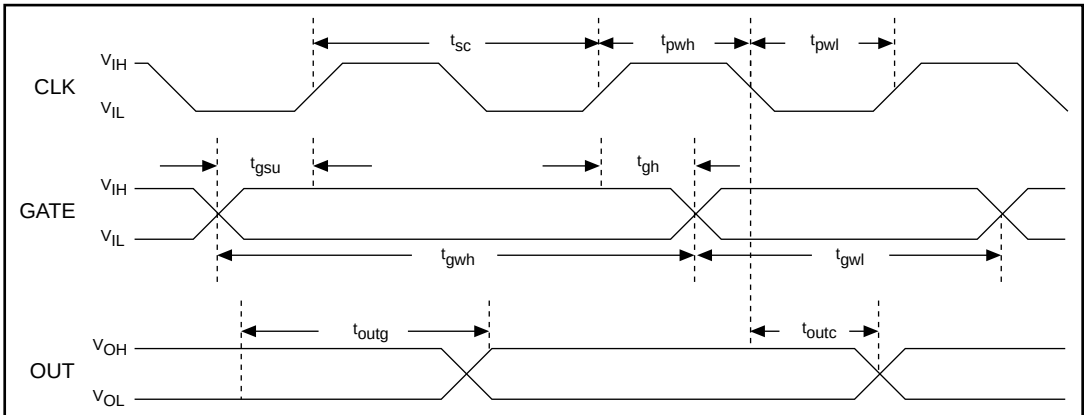
The GATE, CLK, and OUT signals for counters B1 and B2 are available at the I/O connector. The GATE and CLK pins are internally pulled up to +5 V through a 100 kΩ resistor. Refer to Appendix A, *Specifications*, for signal voltage and current specifications.

The following specifications and ratings apply to the 82C53 I/O signals:

- Absolute maximum voltage input rating -0.5 to +5.5 V with respect to DGND
- 82C53 digital input specifications (referenced to DGND):
  - V_{IH} input logic high voltage 2.2 V min 5.3 V max
  - V_{IL} input logic low voltage -0.3 V min 0.8 V max
  - Input load current -10 µA min +10 µA max

- 82C53 digital output specifications (referenced to DGND):
  - V_{OH} output logic high voltage — 3.7 V min — —
  - V_{OL} output logic low voltage — — — 0.45 V max
  - I_{OH} output source current, at V_{OH} — — — -0.92 mA max
  - I_{OL} output sink current, at V_{OL} — — — 2.1 mA max

Figure 3-20 shows the timing requirements for the GATE and CLK input signals and the timing specifications for the 82C53 OUT output signals.



t_{sc}	clock period	380 ns minimum
t_{pwh}	clock high level	230 ns minimum
t_{pwl}	clock low level	150 ns minimum
t_{gsu}	gate setup time	100 ns minimum
t_{gh}	gate hold time	50 ns minimum
t_{gwh}	gate high level	150 ns minimum
t_{gwl}	gate low level	100 ns minimum
t_{outg}	output delay from clock ↓	300 ns maximum
t_{outc}	output delay from gate ↓	400 ns maximum

Figure 3-20. General-Purpose Timing Signals

The GATE and OUT signals in Figure 3-20 are referenced to the rising edge of the CLK signal.

Power Connections

Pin 49 of the I/O connector supplies +5 V from the computer's power supply via a self-resetting fuse. The fuse will reset automatically within a few seconds after you remove the overcurrent condition. Pin 49 is referenced to DGND and you can use the +5 V to power external digital circuitry.

- Power rating 1 A at +4.65 to +5.25 V

Warning: ***Do not directly connect this +5 V power pin to analog or digital ground or to any other voltage source on the 1200 Series or any other device. Doing so can damage the 1200 Series board or your computer. National Instruments is NOT liable for any damage due to incorrect power connections.***

Chapter 4

Theory of Operation

This chapter explains the operation of each functional unit of the 1200 Series boards.

Functional Overview

The block diagrams in Figures 4-1 and 4-2 show the functional overviews of the 1200 Series boards.

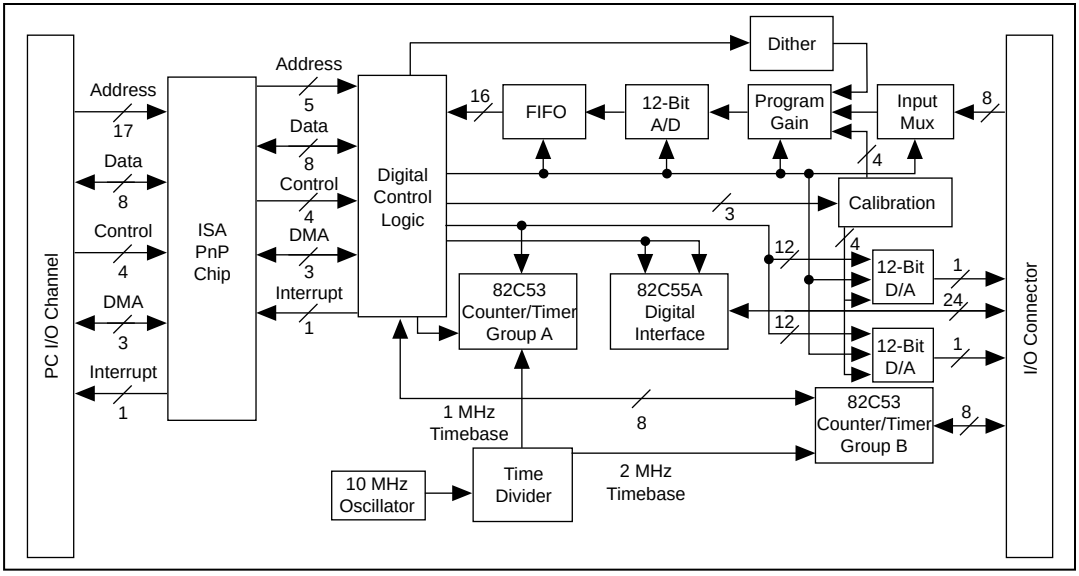


Figure 4-1. Lab-PC-1200 Block Diagram

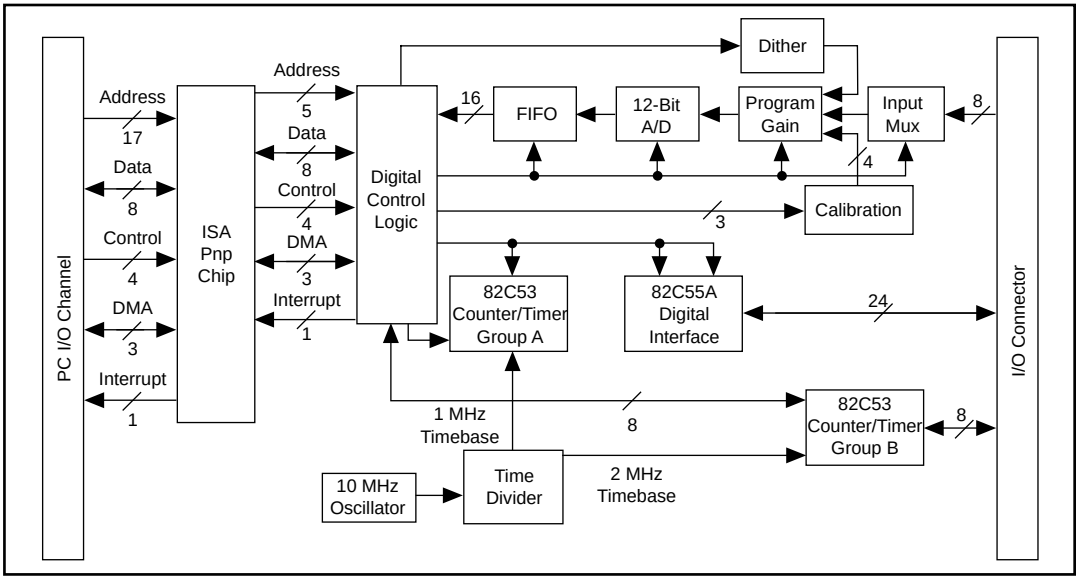


Figure 4-2. Lab-PC-1200AI Block Diagram

The major components of the 1200 Series boards are as follows:

- PC I/O interface circuitry
- Timing circuitry
- Analog input circuitry
- Digital I/O circuitry
- Calibration circuitry

The Lab-PC-1200 also contains an analog output circuitry component. The internal data and control buses interconnect the components.

The rest of the chapter explains the theory of operation of each of the 1200 Series components. Calibration circuitry is discussed in Chapter 5, *Calibration*.

PC I/O Channel Interface Circuitry

The PC I/O channel consists of an address bus, a data bus, a DMA arbitration bus, interrupt lines, and several control and support signals. The components making up the 1200 Series boards' interface circuitry are shown in Figure 4-3.

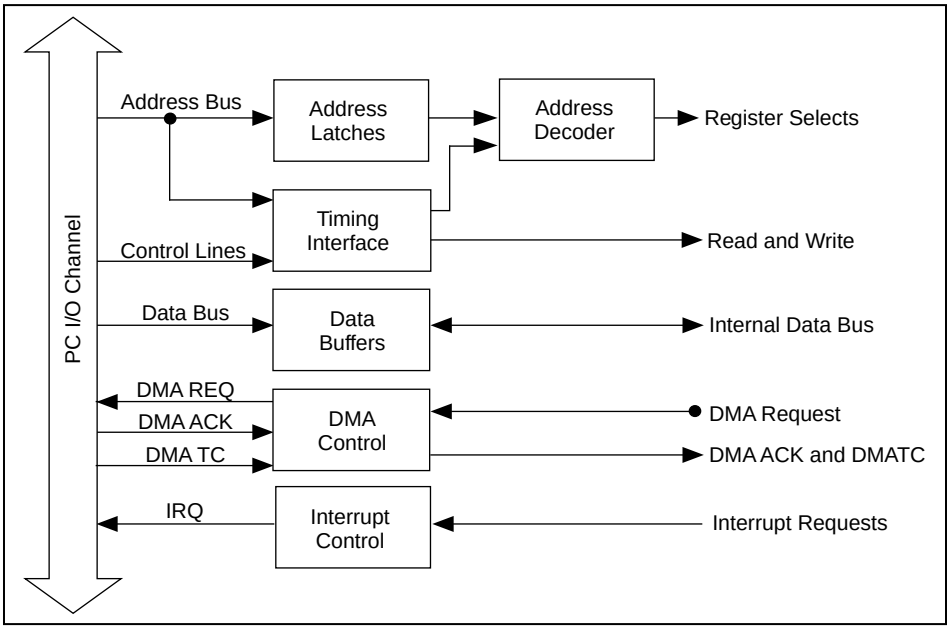


Figure 4-3. PC Interface Circuitry

The 1200 Series boards generate an interrupt in the following cases (each of these interrupts is individually enabled and cleared):

- When a single A/D conversion can be read from the A/D FIFO memory.
- When the A/D FIFO is half-full.
- When a data acquisition operation completes, including when either an OVERFLOW or an OVERRUN error occurs.
- When the digital I/O circuitry generates an interrupt.
- When a DMA terminal count pulse is received.
- The Lab-PC-1200 can also generate an interrupt when a rising edge signal is detected on the DAC update signal.

Timing

The 1200 Series boards use two 82C53 counter/timer integrated circuits for internal data acquisition timing and for general-purpose I/O timing functions. They are also used for analog output timing if you have a

Lab-PC-1200. Figure 4-4 shows a block diagram of both groups of timing circuitry (counter groups A and B).

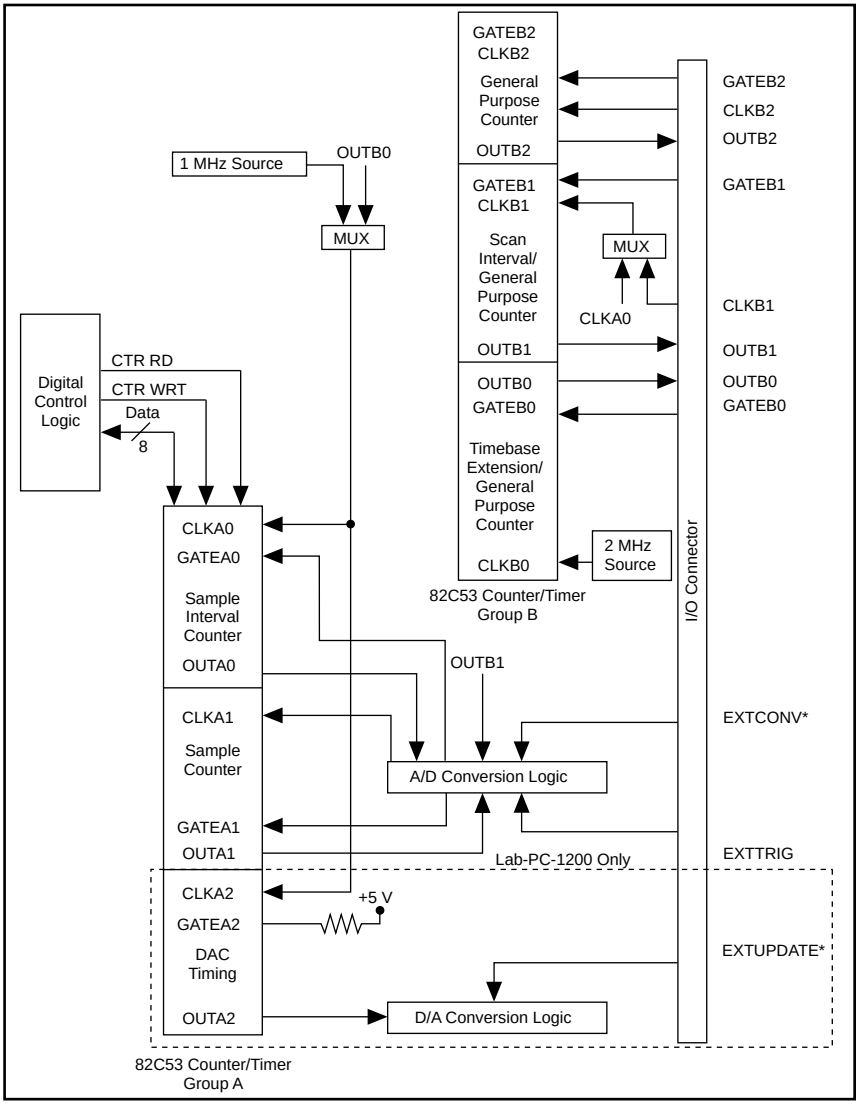


Figure 4-4. 1200 Series Timing Circuitry

Each 82C53 contains three independent 16-bit counter/timers and one 8-bit mode register. Each counter has a CLK input pin, a GATE input pin, and an OUT output pin. You can program all six counter/timers to operate in several useful timing modes.

The first group of counter/timers is group A and includes A0, A1, and A2. For internal data acquisition timing on both boards, you can use counters A0 and A1. If you have a Lab-PC-1200, you can also use counter A2 for analog output timing. Or, instead of using these three counters, you can use the three external timing signals, EXTCONV*, EXTTRIG, and EXTUPDATE*, for data acquisition and DAC timing. For external data acquisition timing on both boards, you can use the EXTCONV* and EXTRIG signals. If you have a Lab-PC-1200, you can also use the EXTUPDATE* signal for analog output timing.

The second group of counter/timers is group B and includes B0, B1, and B2. You can use counters B0 and B1 for internal data acquisition timing, or you can use the external timing signal CLKB1 for analog input timing. If you have a Lab-PC-1200, you can also use counter B0 for analog output timing. If you are not using counters B0 and B1 for internal timing, you can use these counters as general-purpose counter/timers. Counter B2 is reserved for external use as a general-purpose counter/timer.

For a more detailed description of counter group A and counters B0 and B1, refer to the *Analog Input* section and *Analog Output* section.

Analog Input

The 1200 Series boards have eight channels of analog input with software-programmable gain and 12-bit A/D conversion. The 1200 Series boards also contain data acquisition timing circuitry for automatic timing of multiple A/D conversions and include advanced options such as external triggering, gating, and clocking. Figure 4-5 shows an analog input circuitry block diagram.

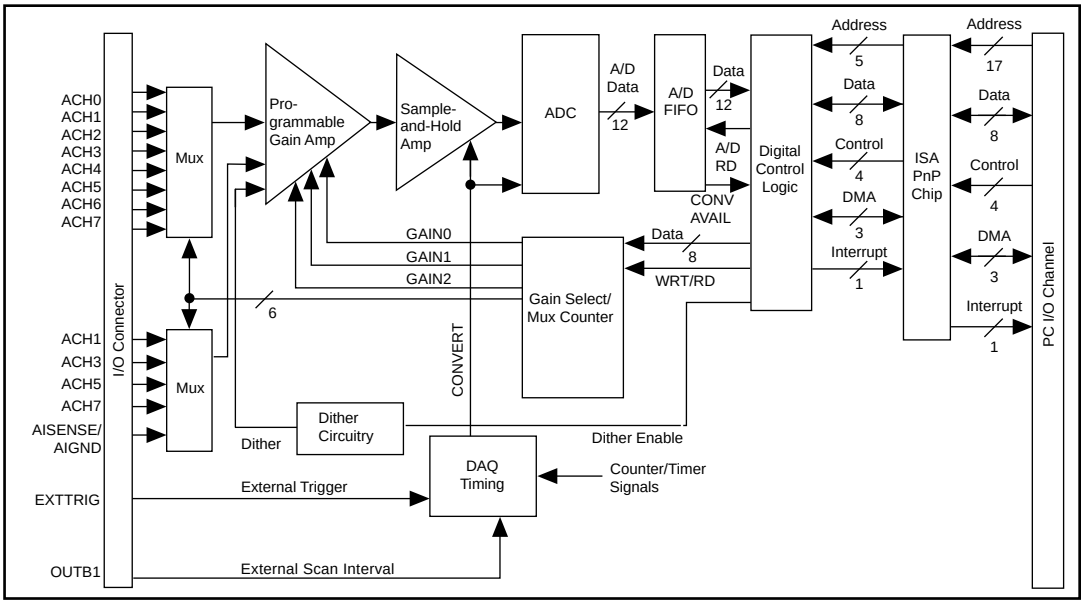


Figure 4-5. 1200 Series Analog Input Circuitry

Analog Input Circuitry

The analog input circuitry consists of two analog input multiplexers (muxes), mux counter/gain select circuitry, a software-programmable gain amplifier, a 12-bit ADC, and a 16-bit, sign-extended FIFO memory.

One of the input muxes has eight analog input channels (channels 0 through 7). The other mux is connected to channels 1, 3, 5, and 7 for differential mode. The input muxes provide input overvoltage protection of ±35 V powered on and ±25 V powered off.

The mux counters control the input muxes. The 1200 Series can perform either single-channel data acquisition or multichannel scanned data acquisition. These two modes are software-selectable. For single-channel data acquisition, you select the channel and gain before data acquisition starts. These gain and mux settings remain constant during the entire data acquisition process. For multichannel scanned data acquisition, you select the highest numbered channel and gain before data acquisition starts. Then the mux counter decrements from the highest numbered channel to channel 0 and repeats the process. Thus, you can scan any number of channels from two to eight. Notice that you use the same gain setting for all channels in the scan sequence.

The programmable-gain amplifier applies gain to the input signal, allowing an analog input signal to be amplified before being sampled and converted, thus increasing measurement resolution and accuracy. The instrumentation amplifier gain is software-selectable. The 1200 Series boards provide gains of 1, 2, 5, 10, 20, 50, and 100.

The dither circuitry, when enabled, adds approximately 0.5 LSB rms of white Gaussian noise to the signal to be converted to the ADC. This addition is useful for applications involving averaging to increase the resolution of the 1200 Series to more than 12 bits, as in calibration. In such applications, which are often lower frequency, noise modulation decreases and differential linearity improves by adding dither. For high-speed, 12-bit applications not involving averaging, you should disable dither because it only adds noise.

When taking DC measurements, such as when calibrating the board, enable dither and average about 1,000 points to take a single reading. This process removes the effects of 12-bit quantization and reduces measurement noise, resulting in improved resolution. Dither, or additive white noise, has the effect of forcing quantization noise to become a zero-mean random variable rather than a deterministic function of input. For more information on the effects of dither, see "Dither in Digital Audio" by John Vanderkooy and Stanley P. Lipshitz, *Journal of the Audio Engineering Society*, Vol. 35, No. 12, Dec. 1987.

The 1200 Series use a 12-bit successive-approximation ADC. The converter 12-bit resolution allows it to resolve its input range into 4,095 different steps. The ADC has an input range of ±5 V and 0 to 10 V.

When an A/D conversion is complete, the ADC clocks the result into the A/D FIFO. The A/D FIFO is 16 bits wide and 512 words deep. This FIFO serves as a buffer to the ADC. The A/D FIFO can collect up to 512 A/D conversion values before losing any information, thus allowing the software some extra time to catch up with the hardware. If you store more than 512 values in the A/D FIFO before reading from it, an error condition called *A/D FIFO overflow* occurs and you lose A/D conversion information.

The output from the ADC can be interpreted as either straight binary or two's complement, depending on which coding scheme you select. Straight binary is the recommended coding scheme for unipolar input mode. With this scheme, the data from the ADC is interpreted as a 12-bit straight binary number with a range of 0 to +4,095. Two's complement is the recommended coding scheme for bipolar input

mode. With this scheme, the data from the ADC is interpreted as a 12-bit two's complement number with a range of -2,048 to +2,047. The output from the ADC is then sign-extended to 16 bits, causing either a leading 0 or a leading F (hex) to be added, depending on the coding and the sign. Thus, data values read from the FIFO are 16 bits wide.

Data Acquisition Operations

This manual uses the phrase *data acquisition operation* to refer to a sequence of timed A/D conversions. The 1200 Series boards perform data acquisition operations in one of three modes: controlled acquisition mode, freerun acquisition mode, and interval scanning acquisition mode. The 1200 Series boards perform both single-channel and multichannel scanned data acquisition.

The data acquisition timing circuitry consists of various clocks and timing signals that control the data acquisition operation. data acquisition timing consists of signals that initiate a data acquisition operation, time the individual A/D conversions, gate the data acquisition operation, and generate scanning clocks. The data acquisition operation can be timed either by the timing circuitry or by externally generated signals. These two timing modes are software-configurable.

Data acquisition operations are initiated either externally through EXTTRIG or through software. The data acquisition operation is terminated either internally by counter A1 of the 82C53 (A) counter/timer circuitry, which counts the total number of samples taken during a controlled operation, or through software in a freerun operation.

Controlled Acquisition Mode

The 1200 Series boards use two counters, counter A0 and counter A1, to execute data acquisition operations in controlled acquisition mode. Counter A0 is used as a sample interval counter, while counter A1 is used as a sample counter. In controlled acquisition mode, the board performs a specified number of conversions, and then the hardware shuts off the conversions. Counter A0 generates the conversion pulses, and counter A1 gates off counter A0 after the programmed count has expired. The number of conversions in a single controlled acquisition mode data acquisition operation is limited to a 16-bit count (65,535 conversions).

Freerun Acquisition Mode

The 1200 Series boards use one counter, counter A0, to execute data acquisition operations in freerun acquisition mode. Counter A0 continuously generates the conversion pulses as long as GATEA0 is held at a high logic level. The software keeps track of the number of conversions that have occurred and turns off counter A0 either after the required number of conversions has been obtained or after some other user-defined criteria have been met. The number of conversions in a single freerun acquisition mode data acquisition operation is unlimited.

Interval-Scanning Acquisition Mode

The 1200 Series boards use two counters for interval-scanning data acquisition. Counter B1 times the scan interval. Counter A0 times the sample interval. In interval-scanning analog input operations, scan sequences are executed at regular, specified intervals. The amount of time that elapses between consecutive scans within the sequence is the *sample interval*. The amount of time that elapses between consecutive scan sequences is the *scan interval*. LabVIEW, LabWindows/CVI, and NI-DAQ support only multichannel interval scanning. Single-channel interval scanning is available only through register-level programming.

Because interval scanning allows you to specify how frequently scan sequences are executed, it is useful for applications in which you need to sample data at regular but relatively infrequent intervals. For example, to sample channel 1, wait 12 µs, sample channel 0, then repeat this process every 65 ms. Then define the operation as follows:

- Start channel: ch1 (which gives a scan sequence of “ch1, ch0”)
- Sample interval: 12 µs
- Scan interval: 65 ms

The first channel will not be sampled until one sample interval from the scan interval pulse. Since the A/D conversion time is 10 µs, your sample interval must be at least this value to ensure proper operation.

Single-Channel Data Acquisition

The 1200 Series boards execute a single-channel analog input operation by performing an A/D conversion on a specified analog input channel every sample interval. The *sample interval* is the amount of time that elapses between successive A/D conversions. The sample interval is controlled either externally by EXTCONV* or internally by counter A0.

To specify a single-channel analog input operation, select an analog input channel and a gain setting for that channel.

Multichannel Scanned Data Acquisition

The 1200 Series boards execute a multichannel data acquisition operation by repeatedly scanning a sequence of analog input channels (the same gain is applied to each channel in the sequence). The channels are scanned in decreasing consecutive order; the highest-numbered channel is the start channel, and channel 0 is the last channel in the sequence.

During each scan sequence, the 1200 Series board scans the start channel (the highest-numbered channel) first, then the next highest-numbered channel, and so on until it scans channel 0. It repeats these scan sequences until the data acquisition operation stops.

For example, if channel 3 is specified as the start channel, the scan sequence is as follows:

ch3, ch2, ch1, ch0, ch3, ch2, ch1, ch0, ch3, ch2, …

To specify the scan sequence for a multichannel scanned analog input operation, you select the start channel for the scan sequence and a gain setting.

Data Acquisition Rates

Maximum data acquisition rates (number of samples per second) are determined by the ADC conversion period plus the sample-and-hold acquisition time. During multichannel scanning, the data acquisition rates are further limited by the input multiplexer and programmable gain amplifier settling times. After switching the input multiplexers, you must allow the amplifier to settle to the new input signal value to within 12-bit accuracy before you perform an A/D conversion, or you will not get 12-bit accuracy. The settling time is a function of the gain selected.

Table 4-1 shows the recommended settling time for each gain setting during multichannel scanning. Table 4-2 shows the maximum recommended data acquisition rates for both single-channel and multichannel data acquisition. For single-channel scanning, this rate is limited only by the ADC conversion period plus the sample-and-hold acquisition time, specified at 10 µs. For multichannel data acquisition, observing the data acquisition rates in Table 4-2 ensures 12-bit

resolution. The hardware is capable of multiscanning at higher rates than those listed in Table 4-2, but 12-bit resolution is not guaranteed.

Table 4-1. Analog Input Recommended Settling Time Versus Gain

Gain	Settling Time (Accuracy ±0.024% (±1 LSB))
1	10 µs typ, 14 µs max
2–10	13 µs typ, 16 µs max
20	15 µs typ, 19 µs max
50	27 µs typ, 34 µs max
100	60 µs typ, 80 µs max

Table 4-2. 1200 Series Maximum Recommended Data Acquisition Rates

Acquisition Mode	Gain	Rate
Single-channel	1, 2, 5, 10, 20, 50, 100	100 kS/s
Multichannel	1	90 kS/s
	2, 5, 10	77 kS/s
	20	66.6 kS/s
	50	37 kS/s
	100	16.6 kS/s

The recommended data acquisition rates in Table 4-2 assume that voltage levels on all the channels included in the scan sequence are within range for the given gain and are driven by low-impedance sources.

Analog Output

- Lab-PC-1200

  The Lab-PC-1200 has two channels of 12-bit D/A output. Each analog output channel can provide unipolar or bipolar output. The Lab-PC-1200 also contains timing circuitry for waveform generation timed either externally or internally. Figure 4-6 shows the analog output circuitry.

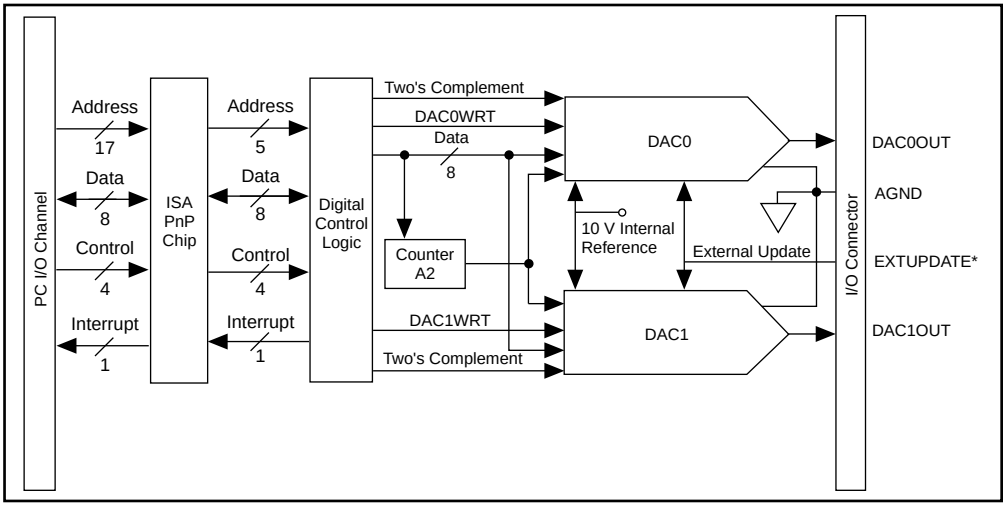


Figure 4-6. Lab-PC-1200 Analog Output Circuitry

Analog Output Circuitry

Each analog output channel contains a 12-bit DAC. The DAC in each analog output channel generates a voltage proportional to the 10 V internal reference multiplied by the 12-bit digital code loaded into the DAC. The voltage output from the two DACs is available at the DAC0OUT and DAC1OUT pins.

You can program each DAC channel for a unipolar voltage output or a bipolar voltage output range. A unipolar output gives an output voltage range of 0.0000 to +9.9976 V. A bipolar output gives an output voltage range of -5.0000 to +4.9976 V. For unipolar output, 0.0000 V output corresponds to a digital code word of 0. For bipolar output, -5.0000 V output corresponds to a digital code word of F800 hex. One LSB is the

voltage increment corresponding to an LSB change in the digital code word. For both outputs:

$$1\ \text{LSB} = \frac{10\ \text{V}}{4{,}095}$$

DAC Timing

You can update the DAC voltages in two modes. In *immediate update mode*, the DAC output voltage is updated as soon as you write to the corresponding DAC. In *delayed update mode*, the DAC output voltage does not change until a low level is detected either from counter A2 of the timing circuitry or EXTUPDATE*. This mode is useful for waveform generation. These two modes are software-selectable.

Digital I/O

The digital I/O circuitry for the 1200 Series has an 82C55A integrated circuit. The 82C55A is a general-purpose programmable peripheral interface containing 24 programmable I/O pins. These pins represent the three 8-bit I/O ports (A, B, and C) of the 82C55A, as well as PA<0..7>, PB<0..7>, and PC<0..7> on the 1200 Series I/O connector. Figure 4-7 shows the digital I/O circuitry.

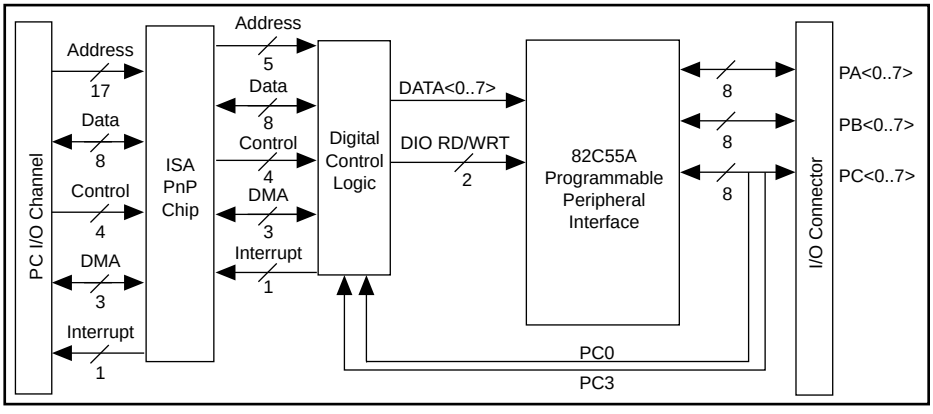


Figure 4-7. Digital I/O Circuitry

All three ports on the 82C55A are TTL-compatible. When enabled, the digital output ports can sink 2.5 mA of current and can source 2.5 mA of current on each digital I/O line. When the ports are not enabled, the digital I/O lines act as high-impedance inputs.

Chapter 5

Calibration

This chapter discusses the calibration procedures for the 1200 Series analog I/O circuitry. However, the 1200 Series boards are factory calibrated, and National Instruments can recalibrate your board if needed. To maintain the 12-bit accuracy of the board analog input circuitry, recalibrate at 6-month intervals. If you have a Lab-PC-1200, you should also recalibrate the analog output circuitry at 6-month intervals.

There are four ways to calibrate your board:

- If you have LabVIEW, use the 1200 Calibrate VI. This VI is located in the **Calibration and Configuration** palette.
- If you have LabWindows/CVI, use the `Calibrate_1200` function.
- Use the NI-DAQ `Calibrate_1200` function. (This function is also used for the SCXI-1200 module, which is functionally equivalent to the 1200 Series boards.) This is the simplest method.
- Use your own register-level writes to the calibration DACs and the EEPROM.

To calibrate using the last method, you need to know the details of the calibration process. This information is in the *Lab-PC-1200/AI Register-Level Programmer Manual.* Use the last calibration method only if NI-DAQ does not support your operating system.

The 1200 Series boards are software-calibrated. The calibration process involves reading offset and gain errors from the analog input section, also the analog output section if you have a Lab-PC-1200, and writing values to the appropriate calibration DACs to null the errors. There are four calibration DACs associated with the analog input section.

♦ Lab-PC-1200

  The Lab-PC-1200 has an additional four calibration DACs associated with the analog output section, two for each output channel.

After the calibration process is complete, each calibration DAC is at a known value. Because these values are lost when the board is powered

down, they are also stored in the onboard EEPROM for future reference.

The factory information occupies one half of the EEPROM and is write protected. The lower half of the EEPROM contains user areas for calibration data. There are four different user areas, outlined in the *Lab-PC-1200/AI Register-Level Programmer Manual*.

When the board is powered on, or the conditions under which it is operating change, you must load the calibration DACs with the appropriate calibration constants.

If you use your 1200 Series board with NI-DAQ, LabVIEW, or LabWindows/CVI, the factory calibration constants are automatically loaded into the calibration DAC the first time a function pertaining to the board is called, and again each time you change your configuration (which includes gain). You can instead choose to load the calibration DACs with calibration constants from the user areas in the EEPROM or you can recalibrate the board and load these constants directly into the calibration DACs. Calibration software is included with the 1200 Series as part of the NI-DAQ software.

Calibration at Higher Gains

The 1200 Series boards have a maximum gain error of 0.8%. This means that if the board is calibrated at a gain of 1 and if the gain is switched to 100, a maximum of 32 LSB error may result in the reading. Therefore, when you are recalibrating your 1200 Series board, you should perform gain calibration at all other gains (2, 5, 10, 20, 50, and 100), and store the corresponding values in the user gain calibration data area of the EEPROM, thus ensuring a maximum error of 0.02% at all gains. The 1200 Series boards are factory calibrated at all gains, and NI-DAQ automatically loads the correct values into the calibration DACs whenever you switch gains.

Calibration Equipment Requirements

The equipment you use to calibrate your 1200 Series board should have a ±0.001% rated accuracy, which is 10 times as accurate as the board. However, calibration equipment with only four times the accuracy as the board and a ±0.003% rated accuracy is acceptable. The inaccuracy

of the calibration equipment results only in gain error; offset error is unaffected.

Calibrate your 1200 Series board to a measurement accuracy of ±0.5 LSBs, which is within ±0.012% of its input range.

For analog input calibration, use a precision DC voltage source, such as a calibrator, with the following specifications.

- Voltage 0 to 10 V
- Accuracy ±0.001% standard
  ±0.003% acceptable

Using the Calibration Function

NI-DAQ contains the `Calibrate_1200` function, with which you can either load the calibration DACs with the factory constants or the user-defined constants stored in the EEPROM, or you can perform your own calibration and directly load these constants into the calibration DACs. To use the `Calibrate_1200` function for analog input calibration, ground an analog input channel at the I/O connector for offset calibration and apply an accurate voltage reference to another input channel for gain calibration.

♦ Lab-PC-1200

  To calibrate the analog output section, the DAC0 and DAC1 outputs must be wrapped back and applied to two other analog input channels.

To calibrate the analog input on your 1200 Series boards, first configure the ADC for RSE mode and for the correct polarity at which you want to perform data acquisition.

♦ Lab-PC-1200

  To calibrate the analog output, first configure the analog input circuitry for RSE and for bipolar polarity, then configure the analog output circuitry for the polarity at which you want to perform output waveform generation.

Refer to the *NI-DAQ Function Reference Manual for PC Compatibles* for more details on the `Calibrate_1200` function.

Specifications

Appendix A

This appendix lists the specifications for the 1200 Series boards. These specifications are typical at 25° C unless otherwise stated.

Analog Input

Input Characteristics

Number of channels ..... Eight single-ended, eight pseudodifferential or four differential, software selectable

Type of ADC..... Successive approximation

Resolution ..... 12 bits, 1 in 4,096

Max sampling rate..... 100 kS/s single channel

Input signal ranges .....

Board Gain (Software-Selectable)	Board Range (Software-Selectable)	
	±5 V	0 to 10 V
1	±5 V	0 to 10 V
2	±2.5 V	0 to 5 V
5	±1 V	0 to 2 V
10	±500 mV	0 to 1 V
20	±250 mV	0 to 500 mV
50	±100 mV	0 to 200 mV
100	±50 mV	0 to 100 mV

Input coupling ..... DC

Max working voltage
(signal + common mode)..... In differential or NRSE mode, the negative input /AISENSE should remain within ±5 V (bipolar input range) or

-5 to +2 V (unipolar input range) of AGND. The positive input should remain within -5 V to +10 V of AGND.

Overvoltage protection ..... ±35 V powered on, ±25 V powered off

Inputs protected ..... ACH<0..7>

FIFO buffer size ..... 512 S

Data transfers ..... DMA, interrupts, programmed I/O

Dither ..... Available

Transfer Characteristics

Relative accuracy ..... ±0.5 LSB typ dithered, ±1.5 LSB max undithered

DNL ..... ±1 LSB max

No missing codes ..... 12 bits, guaranteed

Offset error

Pregain error after calibration ..... 10 μV max

Pregain error before calibration... ±20 mV max

Postgain error after calibration.... 1 mV max

Postgain error before calibration . ±200 mV max

Gain error (relative to calibration reference)

After calibration..... 0.02% of reading max

Before calibration ..... ±2% of reading max

Gain ≠ 1 with gain error adjusted to 0 at gain = 1 ..... ±0.8% of reading max

Amplifier Characteristics

Input impedance

Normal powered on..... 100 GΩ in parallel with 50 pF

Powered off ..... 4.7 kΩ min

Overload ..... 4.7 kΩ min

Input bias current ..... ±100 pA

Input offset current..... ±100 pA

CMRR..... 70 dB, DC to 60 Hz

Dynamic Characteristics

Bandwidth

Small signal (-3 dB) .....

Gain	Bandwidth
1–10	250 kHz
20	150 kHz
50	60 kHz
100	30 kHz

Settling time for full-scale step .....

Gain	Settling Time (Accuracy ±0.024% (±1 LSB))
1	10 µs typ, 14 µs max
2–10	13 µs typ, 16 µs max
20	15 µs typ, 19 µs max
50	27 µs typ, 34 µs max
100	60 µs typ, 80 µs max

System noise *(including quantization error)*.....

Gain	Dither off	Dither on
1–50	0.3 LSB rms	0.5 LSB rms
100	0.5 LSB rms	0.7 LSB rms

Stability

Recommended warm-up time ..... 15 min

Offset temperature coefficient

Pregain.....±15 µV/°C

Postgain .....±100 µV/°C

Gain temperature coefficient ..... ±40 ppm/°C

Explanation of Analog Input Specifications

Relative accuracy is a measure of the linearity of an ADC. However, relative accuracy is a tighter specification than a *nonlinearity* specification. Relative accuracy indicates the maximum deviation from a straight line for the analog-input-to-digital-output transfer curve. If an ADC has been calibrated perfectly, this straight line is the ideal transfer function, and the relative accuracy specification indicates the worst deviation from the ideal that the ADC permits.

A relative accuracy specification of ±1 LSB is roughly equivalent to, but not the same as, a ±0.5 LSB nonlinearity or integral nonlinearity specification because relative accuracy encompasses both nonlinearity and variable quantization uncertainty, a quantity often mistakenly assumed to be exactly ±0.5 LSB. Although quantization uncertainty is ideally ±0.5 LSB, it can be different for each possible digital code and is actually the analog width of each code. Thus, it is more specific to use relative accuracy as a measure of linearity than it is to use what is normally called nonlinearity, because relative accuracy ensures that the *sum* of quantization uncertainty and A/D conversion error does not exceed a given amount.

Integral nonlinearity (INL) in an ADC is an often ill-defined specification that is supposed to indicate a converter's overall A/D transfer linearity. The manufacturer of the ADC chip National Instruments uses on the PCI-1200 specifies its integral nonlinearity by stating that the analog center of any code will not deviate from a straight line by more than ±1 LSB. This specification is misleading because, although a particularly wide code's center may be found within ±1 LSB of the ideal, one of its edges may be well beyond ±1.5 LSB; thus, the ADC would have a relative accuracy of that amount. National Instruments tests its boards to ensure that they meet all three linearity specifications defined in this appendix.

Differential nonlinearity (DNL) is a measure of deviation of code widths from their theoretical value of 1 LSB. The width of a given code is the size of the range of analog values that can be input to produce that code, ideally 1 LSB. A specification of ±1 LSB differential nonlinearity ensures that no code has a width of 0 LSBs (that is, no missing codes) and that no code width exceeds 2 LSBs.

System noise is the amount of noise seen by the ADC when there is no signal present at the input of the board. The amount of noise that is reported directly (without any analysis) by the ADC is not necessarily

the amount of real noise present in the system, unless the noise is considerably greater than 0.5 LSB rms. Noise that is less than this magnitude produces varying amounts of flicker, and the amount of flicker seen is a function of how near the real mean of the noise is to a code transition. If the mean is near or at a transition between codes, the ADC flickers evenly between the two codes, and the noise is very near 0.5 LSB. If the mean is near the center of a code and the noise is relatively small, very little or no flicker is seen, and the noise is reported by the ADC as nearly 0 LSB. From the relationship between the mean of the noise and the measured rms magnitude of the noise, the character of the noise can be determined. National Instruments has determined that the character of the noise in the 1200 Series boards is fairly Gaussian, so the noise specifications given are the amounts of pure Gaussian noise required to produce our readings.

Explanation of Dither

The *dither circuitry*, when enabled, adds approximately 0.5 LSB rms of white Gaussian noise to the signal to be converted to the ADC. This addition is useful for applications involving averaging to increase the resolution of the 1200 Series to more than 12 bits, as in calibration. In such applications, which are often lower frequency in nature, noise modulation is decreased and differential linearity is improved by the addition of dither. For high-speed 12-bit applications not involving averaging, dither should be disabled because it only adds noise.

When taking DC measurements, such as when calibrating the board, enable dither and average about 1,000 points to take a single reading. This process removes the effects of 12-bit quantization and reduces measurement noise, resulting in improved resolution. Dither, or additive white noise, has the effect of forcing quantization noise to become a zero-mean random variable rather than a deterministic function of input. For more information on the effects of dither, see "Dither in Digital Audio" by John Vanderkooy and Stanley P. Lipshitz, *Journal of the Audio Engineering Society*, Vol. 35, No. 12, Dec. 1987.

Explanation of Data Acquisition Rates

Maximum data acquisition rates (number of samples per second) are determined by the conversion period of the ADC plus the sample-and-hold acquisition time, which is specified at 10 µs. During multichannel scanning, the data acquisition rates are further limited by the settling time of the input multiplexers and programmable gain amplifier. After the input multiplexers are switched, the amplifier must

be allowed to settle to the new input signal value to within 12-bit accuracy. The settling time is a function of the gain selected.

Analog Output, Lab-PC-1200 Only

Output Characteristics

Number of channels ..... Two voltage

Resolution ..... 12 bits, 1 in 4,096

Typical update rate ..... 1 kS/s, system dependent

Type of DAC ..... Double buffered

Data transfers ..... Interrupts, programmed I/O

Transfer Characteristics

Relative accuracy (INL) ..... ±0.25 LSB typ, ±0.50 LSB max

DNL ..... ±0.25 LSB typ, ±0.75 LSB max

Monotonicity ..... 12 bits, guaranteed

Offset error

- After calibration ..... ±0.2 mV max
- Before calibration ..... ±50 mV max

Gain error (relative to internal reference)

- After calibration ..... 0.004% of reading max
- Before calibration ..... ±1% of reading max

Voltage Output

Ranges ..... 0 to 10 V, ±5 V, software selectable

Output coupling ..... DC

Output impedance ..... 0.2 Ω typ

Current drive ..... ±2 mA

Protection ..... Short circuit to ground

Power-on state ..... 0 V

Dynamic Characteristics

Settling time to full-scale range (FSR) ..... 5 µs

Stability

Offset temperature coefficient ..... ±50 µV/°C

Gain temperature coefficient ..... ±30 ppm/°C

Explanation of Analog Output Specifications

- Lab-PC-1200

  Relative accuracy in a D/A system is the same as nonlinearity because no uncertainty is added due to code width. Unlike an ADC, every digital code in a D/A system represents a specific analog value rather than a range of values. The relative accuracy of the system is therefore limited to the worst-case deviation from the ideal correspondence (a straight line), except noise. If a D/A system has been calibrated perfectly, the relative accuracy specification reflects its worst-case absolute error.

  DNL in a D/A system is a measure of deviation of code width from 1 LSB. In this case, code width is the difference between the analog values produced by consecutive digital codes. A specification of ±1 LSB differential nonlinearity ensures that the code width is always greater than 0 LSBs (guaranteeing monotonicity) and is always less than 2 LSBs.

Digital I/O

Number of channels ..... 24 I/O (three 8-bit ports; uses the 82C55A PPI

Compatibility ..... TTL

Digital logic levels .....

Level	Min	Max
Input low voltage	-0.3 V	0.8 V
Input high voltage	2.2 V	5.3 V
Output low voltage	—	—
(I_{OUT} = 2.5 mA)	—	0.4 V
Output high voltage	—	—
(I_{OUT} = -40 µA)	4.2 V	—
(I_{OUT} = -2.5 mA)	3.7 V	—

Power-on state..... All ports mode 0 input

Protection ..... -0.5 V to 5.5 V powered on, ±0.5 V powered off

Data transfers ..... Interrupts, programmed I/O

Timing I/O

Number of channels ..... 3 counter/timers

Protection ..... -0.5 V to 5.5 V powered on, ±0.5 V powered off

Resolution

Counter/timers ..... 16 bits

Compatibility ..... TTL

Base clock available ..... 2 MHz

Base clock accuracy ..... ±50 ppm max

Max source frequency ..... 8 MHz

Min source pulse duration ..... 125 ns

Min gate pulse duration ..... 100 µs

Digital logic levels .....

Level	Min	Max
Input low voltage	-0.3 V	0.8 V
Input high voltage	2.2 V	5.3 V
Output low voltage	—	—
(I_{OUT} = 2.1 mA)	—	0.45 V
Output high voltage	—	—
(I_{OUT} = 0.92 mA)	3.7 V	—

Protection ..... -0.5 to 5.5 V powered on, ±0.5 V powered off

Data transfer ..... Interrupts, programmed I/O

Digital Trigger

Compatibility ..... TTL

Response ..... Rising edge

Pulse width ..... 50 ns min

Bus Interface

Type ..... Slave

Power Requirement

Power consumption

Lab-PC-1200..... 185 mA at ±5 VDC (±5%)

Lab-PC-1200AI ..... 150 mA at ±5 VDC (±5%)

Power available at I/O connector..... +4.65 to +5.25 V fused at 1 A

Physical

Dimensions ..... 17.45 by 10.56 cm (6.87 by 4.16 in.)

I/O connector ..... 50-pin male

Environment

Operating temperature..... 0° to 50° C

Storage temperature..... -55° to 150° C

Relative humidity..... 5% to 90% noncondensing

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http://www.natinst.com/documentation/daq/

Customer Communication

Appendix B

For your convenience, this appendix contains forms to help you gather the information necessary to help us solve your technical problems and a form you can use to comment on the product documentation. When you contact us, we need the information on the Technical Support Form and the configuration form, if your manual contains one, about your system configuration to answer your questions as quickly as possible.

National Instruments has technical assistance through electronic, fax, and telephone systems to quickly provide the information you need. Our electronic services include a bulletin board service, an FTP site, a FaxBack system, and e-mail support. If you have a hardware or software problem, first try the electronic support systems. If the information available on these systems does not answer your questions, we offer fax and telephone support through our technical support centers, which are staffed by applications engineers.

Electronic Services

Bulletin Board Support

National Instruments has BBS and FTP sites dedicated for 24-hour support with a collection of files and documents to answer most common customer questions. From these sites, you can also download the latest instrument drivers, updates, and example programs. For recorded instructions on how to use the bulletin board and FTP services and for BBS automated information, call (512) 795-6990. You can access these services at:

United States: (512) 794-5422 or (800) 327-3077
Up to 14,400 baud, 8 data bits, 1 stop bit, no parity

United Kingdom: 01635 551422
Up to 9,600 baud, 8 data bits, 1 stop bit, no parity

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Hard disk capacity _____MB _____Brand _____

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_____

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Configuration _____

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Configuration _____

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_____

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List any error messages: _____

_____

_____

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Other Products

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Type of video board installed _____

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Prefix	Meaning	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
μ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

Numbers/Symbols

°	degrees
>	greater than
≥	greater than or equal to
<	less than
-	negative of, or minus
Ω	ohms
%	percent
±	plus or minus
+	positive of, or plus

A

A	amperes
ACH <0..7>	analog channel 0 through 7 signals
ACK*	acknowledge input signal
A/D	analog-to-digital
ADC	analog-to-digital converter
AGND	analog ground signal
AI	analog input
AISENSE/AIGND	analog input sense/analog input ground signal
ANSI	American National Standards Institute
AO	analog output
AVAIL	available

B

BBS	bulletin board system
BSC	bisynchronous

C

C	Celsius
CH	channel
CLKB1, CLKB2	counter B1, B2 clock signals
cm	centimeters
CNTINT	counter interrupt signal
CONV	conversion

CTR	counter

D

D/A	digital-to-analog
DAC	digital-to-analog converter
DAC OUTPUT UPDATE	DAC output update signal
DAC0OUT, DAC1OUT	digital-to-analog converter 0, 1 output signals
DACWRT	DAC write signal
DAQ	data acquisition
DAQD*/A	data acquisition board data/address line signal
DATA	data lines at the specified port signal
dB	decibels
DC	direct current
DGND	digital ground signal
DI	digital input
DIFF	differential
DIO	digital input/output
DMA	direct memory access
DMATC	direct memory access terminal count
DNL	differential nonlinearity
DO	digital output

E

EEPROM	electrically erased programmable read-only memory

EXTCONV*	external convert signal
EXTTRIG	external trigger signal
EXTUPDATE*	external update signal

F

F	farad
ft.	feet
FIFO	first in first out memory buffer
FSR	full-scale range
FTP	file transfer protocol

G

GATB <0..2>	counter B0, B1, B2 gate signals
GATE	gate signal

H

hex	hexadecimal
Hz	hertz

I

IBF	input buffer full signal
in.	inches
INTR	interrupt request signal
I/O	input/output
I_{OUT}	output current

IRQ	interrupt request
ISA	industry standard architecture

L

LED	light-emitting diode
LSB	least significant bit

M

max	maximum
MB	megabytes of memory
min	minimum
min.	minutes
MIO	multifunction I/O
mux	multiplexer

N

N/A	not applicable
NC	not connected
NRSE	nonreferenced single-ended

O

OBF*	output buffer full signal
OUTB0, OUTB1	counter B0, B1 output signals
OVERFLOW	overflow error
OVERRUN	overrun error

P

PA, PB, PC <0..7>	port A, B, or C 0 through 7 signals
PC	personal computer
Pgm	program
POSTTRIG	posttrigger mode
PnP	Plug and Play
PPI	programmable peripheral interface
ppm	parts per million
PRETRIG	pretrigger mode

R

RD*	read signal
REQ	request
RMA	return material authorization
rms	root mean square
RSE	referenced single-ended
RTD	resistance temperature detector

S

s	seconds
S	samples
SCXI	signal conditioning eXtensions for instrumentation (bus)
STB	strobe input signal

T

t_d	minimum period
t_{gh}	gate hold time
t_{gsu}	gate setup time
t_{gwh}	gate high level
t_{gwl}	gate low level
t_m	minimum pulse width
t_{outc}	output delay from gate
t_{outg}	output delay from clock
t_{pwh}	clock high level
t_{pwl}	clock low level
t_{sc}	clock period
TTL	transistor-transistor logic
typ	typical

U

UP/BP*	unipolar/bipolar bit

V

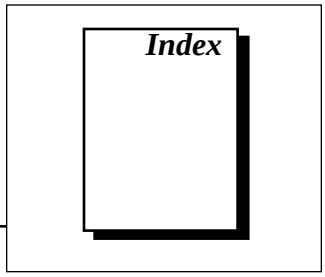
V	volts
$V\pm_{in}$	positive/negative input voltage
V_{cm}	common-mode noise
VDC	volts direct current
V_{diff}	differential input voltage

V_g	ground loop losses
VGA	video graphics array
VI	virtual instrument
V_{IH}	volts, input high
V_{IL}	volts, input low
V_m	measured voltage
VOUT0, VOUT1	DAC output voltages
V_s	signal source

W

WRT*	write signal

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