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# PC-LPM-16/PnP User Manual

*Multifunction I/O Board for the PC*

November 1996 Edition
Part Number 320287C-01

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This manual describes the mechanical and electrical aspects of the PC-LPM-16PnP and contains information concerning its installation, operation, and programming. The PC-LPM-16PnP is a low-cost, low-power analog input, digital, and timing I/O board for the IBM PC/XT, PC AT, Personal System/2 Models 25 and 30, and laptop compatible computers.

This manual also applies to the PC-LPM-16, a non-Plug and Play board. The boards are identical in functionality, programming, and performance, except for the differences listed in Appendix C, *Using Your PC-LPM-16 (Non-PnP) Board*.

# Organization of This Manual

The *PC-LPM-16/PnP User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the PC-LPM-16/PnP, lists what you need to get started, software programming choices, and optional equipment, and explains how to unpack the PC-LPM-16/PnP.
- Chapter 2, *Installation and Configuration*, describes the installation and configuration of the PC-LPM-16PnP.
- Chapter 3, *Theory of Operation*, includes an overview of the PC-LPM-16PnP board and explains the operation of each functional unit making up the board. This chapter also explains the basic operation of the PC-LPM-16PnP circuitry.
- Chapter 4, *Signal Connections*, describes how to make input and output signal connections to your PC-LPM-16PnP board via the I/O connector.
- Appendix A, *Specifications*, lists the specifications of the PC-LPM-16PnP.
- Appendix B, *MSM82C53 Data Sheet*, contains a manufacturer data sheet for the MSM82C53 CMOS programmable interval timer (OKI Semiconductor).

- Appendix C, *Using Your PC-LPM-16 (Non-PnP) Board*, describes the differences between the PC-LPM-16PnP and the PC-LPM-16 non-PnP boards, the PC-LPM-16 board configuration, and installing the PC-LPM-16 into your computer.
- Appendix D, *Register-Level Programming*, describes in detail information related to register-level programming the PC-LPM-16/PnP.
- Appendix E, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products.
- The *Glossary* contains an alphabetical list and description of terms used in this manual, including abbreviations, acronyms, metric prefixes, mnemonics, and symbols.
- The *Index* lists topics covered in this manual, including the page number where the topic can be found.

# Conventions Used in This Manual

The following conventions are used in this manual:

| | |
|---|---|
| < > | Angle brackets containing numbers separated by an ellipsis represent a range, signal, or port (for example, ACH<0..7> stands for ACH0 through ACH7). |
| **bold** | Bold text denotes menus, menu items, or dialog box buttons or options, and error messages. |
| ***bold italic*** | Bold italic text denotes a note, caution, or warning. |
| *italic* | Italic text denotes emphasis, a cross reference, or an introduction to a key concept. |
| `monospace` | Text in this font denotes text or characters that are to be literally input from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions, and for statements and comments taken from program code. |
| NI-DAQ | NI-DAQ refers to the NI-DAQ software for PC compatibles, unless otherwise noted. |

| | |
|---|---|
| Non-PnP | Non-PnP (non-Plug and Play) means that the board requires you to manually configure the product's base address and interrupt level with switches and jumpers. You must perform this configuration before installing the board into your computer. |
| PC | PC refers to the IBM PC/XT, PC AT, Personal System/2 Models 25 and 30, and laptop compatible computers. |
| PC-LPM-16/PnP | PC-LPM-16/PnP refers to both the Plug and Play and the non-Plug and Play versions of the board. |
| PC-LPM-16PnP | PC-LPM-16PnP refers to the Plug and Play version of the board. |
| PC-LPM-16 | PC-LPM-16 refers to the non-Plug and Play version of the board. |
| PnP | PnP (Plug and Play) means that the board is fully compatible with the industry-standard Plug and Play ISA Specification. All bus-related configuration is performed through software, freeing you from manually configuring jumpers or switches to set the product's base address and interrupt level. Plug and Play systems automatically arbitrate and assign system resources to a PnP product. |

Abbreviations, acronyms, metric prefixes, mnemonics, symbols, and terms are listed in the *Glossary*.

# National Instruments Documentation

The *PC-LPM-16/PnP User Manual* is one piece of the documentation set for your DAQ or SCXI system. You could have any of several types of manuals depending on the hardware and software in your system. Use the manuals you have as follows:

- *Getting Started with SCXI*—If you are using SCXI, this is the first manual you should read. It gives an overview of the SCXI system and contains the most commonly needed information for the modules, chassis, and software.
- Your SCXI hardware user manuals—If you are using SCXI, read these manuals next for detailed information about signal connections and module configuration. They also explain in greater detail how the module works and contain application hints.
- Your DAQ hardware documentation—This documentation has detailed information about the DAQ hardware that plugs into or is connected to your computer. Use this documentation for hardware

installation and configuration instructions, specification information about your DAQ hardware, and application hints.

- Software documentation—Examples of software documentation you may have are the LabVIEW, LabWindows®/CVI documentation sets, and the NI-DAQ documentation. After you set up your hardware system, use either the application software (LabVIEW or LabWindows/CVI) or the NI-DAQ documentation to help you write your application. If you have a large, complicated system, it is worthwhile to look through the software documentation before you configure your hardware.
- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making your connections.
- *SCXI Chassis User Manual*—If you are using SCXI, read this manual for maintenance information on the chassis and for installation instructions.

# Related Documentation

The following document contains information that you may find helpful as you read this manual:

- Your computer user or technical reference manual

# Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix E, *Customer Communication*, at the end of this manual.

Chapter 1

# Introduction

This chapter describes the PC-LPM-16/PnP, lists what you need to get started, software programming choices, and optional equipment, and explains how to unpack the PC-LPM-16/PnP.

## About the PC-LPM-16/PnP

The PC-LPM-16/PnP is a low-cost, low-power analog input, digital, and timing I/O board for the PC. The board contains a 12-bit, successive-approximation, self-calibrating ADC with 16 analog inputs, 8 lines of TTL-compatible digital input, and 8 lines of digital output. The PC-LPM-16/PnP also contains two 16-bit counter/timer channels for timing I/O.

The low cost of a PC-LPM-16/PnP-based system makes it ideal for laboratory work in industrial and academic environments. The board's low power consumption and small size make the PC-LPM-16/PnP especially suitable for laptop computers. The multichannel analog input is useful in signal analysis and data logging. The 12-bit ADC is useful in high-resolution applications such as chromatography, temperature measurement, and DC voltage measurement. You can use the 16 TTL-compatible digital I/O lines for switching external devices such as transistors and solid-state relays, for reading the status of external digital logic, and for generating interrupts. You can use the counter/timers to synchronize events, generate pulses, and measure frequency and time. The PC-LPM-16/PnP, used in conjunction with your computer, is a versatile, cost-effective platform for laboratory test, measurement, and control.

# What You Need to Get Started

To set up and use your PC-LPM-16/PnP board, you will need the following:

- ❏ PC-LPM-16/PnP board
- ❏ *PC-LPM-16/PnP User Manual*
- ❏ One of the following software packages and documentation:
  NI-DAQ for PC Compatibles
  LabVIEW for Windows
  LabWindows/CVI for Windows
- ❏ Your computer

# Software Programming Choices

There are several options to choose from when programming your National Instruments DAQ and SCXI hardware. You can use LabVIEW, LabWindows/CVI, NI-DAQ, or register-level programming.

## LabVIEW and LabWindows/CVI Application Software

LabVIEW and LabWindows/CVI are innovative program development software packages for data acquisition and control applications. LabVIEW uses graphical programming, whereas LabWindows/CVI enhances traditional programming languages. Both packages include extensive libraries for data acquisition, instrument control, data analysis, and graphical data presentation.

LabVIEW features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to the NI-DAQ software.

LabWindows/CVI features interactive graphics, a state-of-the-art user interface, and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions for using LabWindows/CVI with National Instruments DAQ hardware, is

included with the NI-DAQ software kit. The LabWindows/CVI Data Acquisition Library is functionally equivalent to the NI-DAQ software.

Using LabVIEW or LabWindows/CVI software will greatly reduce the development time for your data acquisition and control application.

## NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ is not packaged with signal conditioning or accessory products. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation (timed D/A conversion), digital I/O, counter/timer operations, SCXI, RTSI, calibration, messaging, and acquiring data to extended memory.

NI-DAQ has both high-level DAQ I/O functions for maximum ease of use and low-level DAQ I/O functions for maximum flexibility and performance. Examples of high-level functions are streaming data to disk or acquiring a certain number of data points. An example of a low-level function is writing directly to registers on the DAQ device. NI-DAQ does not sacrifice the performance of National Instruments DAQ devices because it lets multiple devices operate at their peak performance.

NI-DAQ also internally addresses many of the complex issues between the computer and the DAQ hardware such as programming interrupts and DMA controllers. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Whether you are using conventional programming languages, LabVIEW, or LabWindows/CVI, your application uses the NI-DAQ driver software, as illustrated in Figure 1-1.

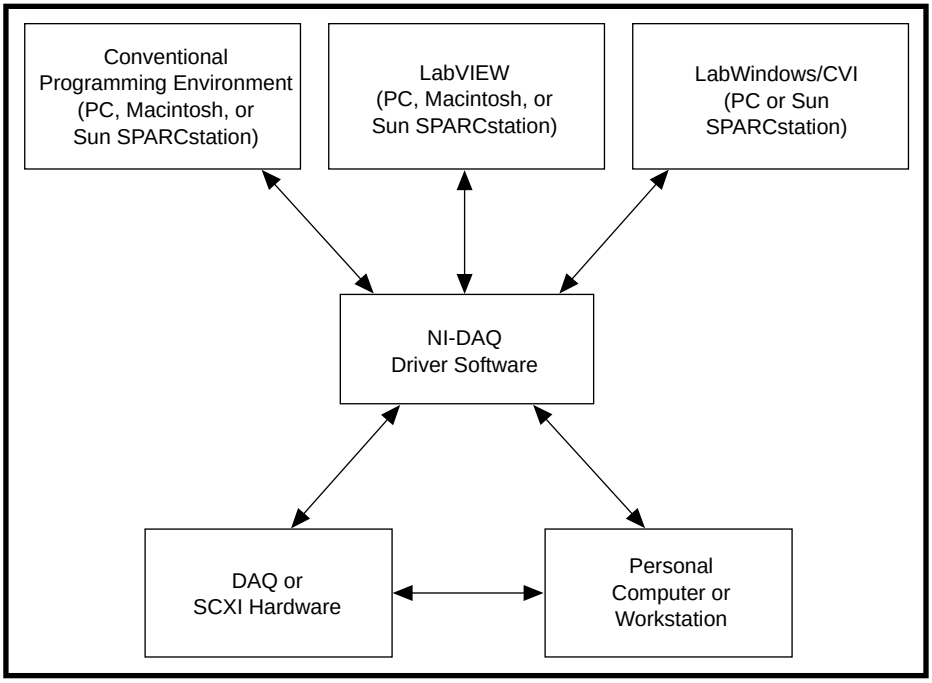



**Figure 1-1.** The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

## Register-Level Programming

The final option for programming any National Instruments DAQ hardware is to write register-level software. Writing register-level programming software can be very time-consuming and inefficient and is not recommended for most users.

Even if you are an experienced register-level programmer, consider using NI-DAQ, LabVIEW, or LabWindows/CVI to program your National Instruments DAQ hardware. Using the NI-DAQ, LabVIEW, or LabWindows/CVI software is as easy and as flexible as register-level programming and can save weeks of development time.

# Optional Equipment

National Instruments offers a variety of products to use with your PC-LPM-16/PnP board, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded with 50-pin screw terminals
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI you can condition and acquire up to 3,072 channels.
- Low channel-count signal conditioning modules, boards, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample-and-hold circuitry, and relays

For more specific information about these products, refer to your National Instruments catalogue or call the office nearest you.

# Custom Cables

National Instruments currently offers a cable termination accessory, the CB-50, for use with the PC-LPM-16/PnP. This kit includes a terminated, 50-conductor, flat ribbon cable and a connector block. Signal input and output wires can be attached to screw terminals on the connector block and connected to the PC-LPM-16/PnP I/O connector.

The CB-50 is useful for the initial prototyping of an application or in situations where PC-LPM-16/PnP interconnections are frequently changed. Once you develop a final field wiring scheme, however, you may want to develop your own cable. This section contains information and guidelines for the design of custom cables.

The PC-LPM-16/PnP I/O connector is a 50-pin, male, ribbon cable header connector. The following list gives recommended part numbers for use with your PC-LPM-16/PnP board:

- Electronic Products Division/3M (part number 3596-5002)
- T&B/Ansley Corporation (part number 609-5007)

The mating connector for the PC-LPM-16/PnP is a 50-position, polarized, ribbon socket connector with strain relief. National Instruments uses a polarized (keyed) connector to prevent inadvertent upside-down connection to the PC-LPM-16/PnP. Recommended manufacturer part numbers for this mating connector are as follows:

- Electronic Products Division/3M (part number 3425-7650)
- T&B/Ansley Corporation (part number 609-5041CE)

The following are the standard ribbon cables (50-conductor, 28 AWG, stranded) that can be used with these connectors:

- Electronic Products Division/3M (part number 3365/50)
- T&B/Ansley Corporation (part number 171-50)

# Unpacking

Your PC-LPM-16/PnP board is shipped in an antistatic package to prevent electrostatic damage to the board. Electrostatic discharge can damage several components on the board. To avoid such damage in handling the board, take the following precautions:

- Ground yourself via a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of your computer chassis before removing the board from the package.
- Remove the board from the package and inspect the board for loose components or any other sign of damage. Notify National Instruments if the board appears damaged in any way. *Do not* install a damaged board into your computer.
- *Never* touch the exposed pins of connectors.

# Installation and Configuration

Chapter 2

This chapter describes the installation and configuration of the PC-LPM-16PnP. For information on installing and configuring the PC-LPM-16, a non-PnP board, refer to Appendix C, *Using Your PC-LPM-16 (Non-PnP) Board*.

## Hardware Installation

You can install the PC-LPM-16PnP in any available expansion slot in your computer. The following are general installation instructions, but consult your computer user manual or technical reference manual for specific instructions and warnings.

1. Turn off and unplug your computer.
2. Remove the top cover or access port to the I/O channel.
3. Remove the expansion slot cover on the back panel of the computer.
4. Insert the PC-LPM-16PnP board into any 8-bit or 16-bit slot. It may be a tight fit, but *do not force* the board into place.
5. Screw the mounting bracket of the PC-LPM-16PnP board to the back panel rail of the computer.
6. Replace the cover.
7. Plug in and turn on your computer.

The PC-LPM-16PnP is installed.

# Software Installation

If you are using NI-DAQ, refer to your NI-DAQ release notes to install your driver software. Find the installation section for your operating system and follow the instructions given there.

If you are using LabVIEW, refer to your LabVIEW release notes to install your application software. After you have installed LabVIEW, refer to the NI-DAQ release notes and follow the instructions given there for your operating system and LabVIEW.

If you are using LabWindows/CVI, refer to your LabWindows/CVI release notes to install your application software. After you have installed LabWindows/CVI, refer to the NI-DAQ release notes and follow the instructions given there for your operating system and LabWindows/CVI.

If you are a register-level programmer, refer to Appendix D, *Register-Level Programming*, for software configuration information.

# Board Configuration

## Plug and Play

The PC-LPM-16PnP is fully compatible with the industry-standard Intel/Microsoft Plug and Play Specification version 1.0a. A Plug and Play system arbitrates and assigns resources through software, freeing you from manually setting switches and jumpers. These resources include the board base I/O address and interrupt channels. Each PC-LPM-16PnP is configured at the factory to request these resources from the Plug and Play Configuration Manager.

The Configuration Manager receives all of the resource requests at startup, compares the available resources to those requested, and assigns the available resources as efficiently as possible to the Plug and Play boards. Application software can query the Configuration Manager to determine the resources assigned to each board without your involvement. The Plug and Play software is installed as a device driver or as an integral component of the computer BIOS.

## Base I/O Address and Interrupt Selection

You can configure your PC-LPM-16PnP to use base addresses in the range of 100 to FFF0 hex. The PC-LPM-16PnP occupies 16 bytes of address space and must be located on a 16-byte boundary. Therefore, valid addresses include 100, 110, 120…, FFE0, FFF0 hex. This selection is software-configured and does not require you to manually change any settings on the board.

The PC-LPM-16PnP can use interrupt channels 3, 4, 5, 6, 7, and 9.

There are different ways to assign the base address to your board:

- For Windows 95, the base address and interrupt should be set automatically. However, if you want to view or change these settings, you can set the board resources using the **Device Manager**. Windows 95 will automatically allocate resources, but these can be changed in the **Device Manager**:
  a. Click the right mouse button on **My Computer** to bring up system properties.
  b. Select **Device Manager**.
  c. Select **Data Acquisition Devices**.
  d. Select the **PC-LPM-16**.

  You can change address and interrupt settings on the **Resources** page.
- For Windows 3.10 or 3.11, you can use the NI-DAQ Configuration Utility (formerly `WDAQCONF`) to assign the board resources. If a standard configuration utility is present in the system, you will not be able to modify the board resources.
- You can use a standard configuration utility like Intel ISA Configuration Utility (ICU). ICU dynamically assigns the base address to your board when you boot up the computer. You can also lock the board resources when you use ICU. For additional information on ICU, contact Intel Corporation for a copy of Plug and Play Specification version 1.0a.

# Non-Plug and Play

To configure the non-Plug and Play PC-LPM-16 board, refer to Appendix C, *Using Your PC-LPM-16 (Non-PnP) Board*.

Chapter 3

# Theory of Operation

This chapter includes an overview of the PC-LPM-16PnP board and explains the operation of each functional unit making up the board. This chapter also explains the basic operation of the PC-LPM-16PnP circuitry.

## Functional Overview

The following are the major components making up the PC-LPM-16PnP:

- PC I/O channel interface circuitry
- Analog input and data acquisition circuitry
- Digital I/O circuitry
- Timing I/O circuitry

You can execute data acquisition functions by using the analog input circuitry and some of the timing I/O circuitry. The internal data and control buses interconnect the components. The theory of operation for each of these components is explained in the remainder of this chapter.

The block diagram in Figure 3-1 shows a functional overview of the PC-LPM-16PnP.

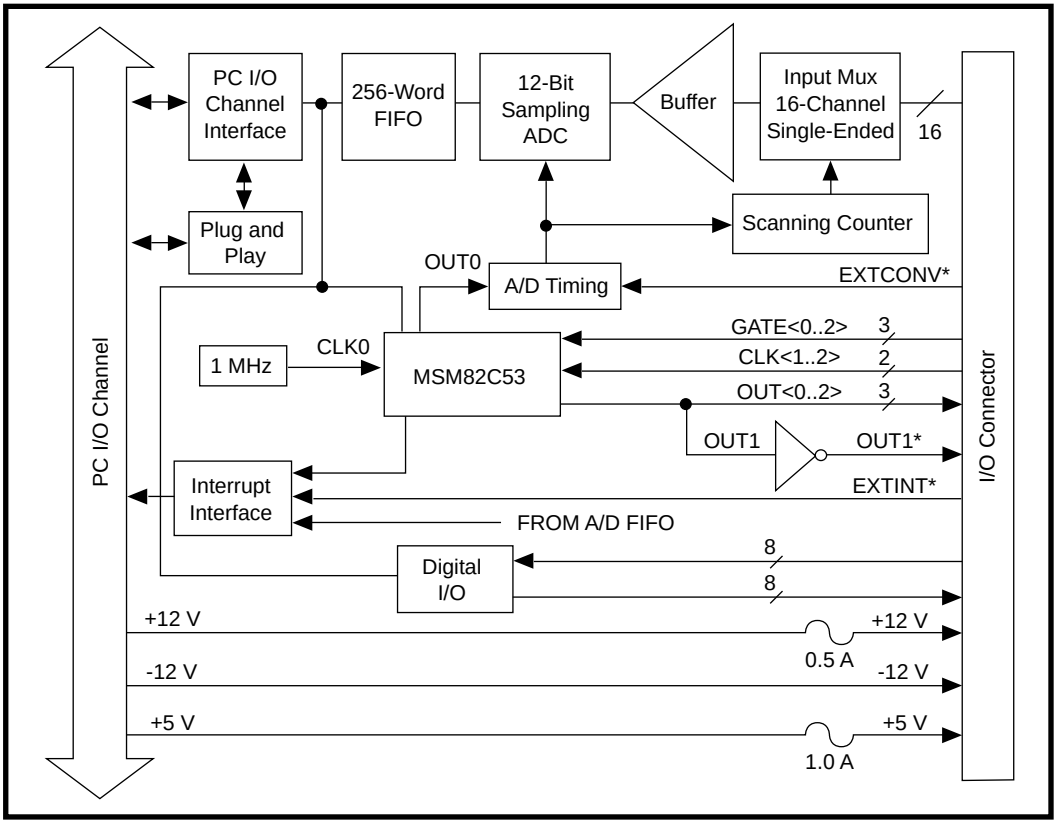



**Figure 3-1.** PC-LPM-16PnP Block Diagram

# PC I/O Channel Interface Circuitry

The PC I/O channel interface circuitry consists of an address bus, a data bus, interrupt lines, and several control and support signals. The components making up the PC-LPM-16PnP PC I/O channel interface circuitry are shown in Figure 3-2.

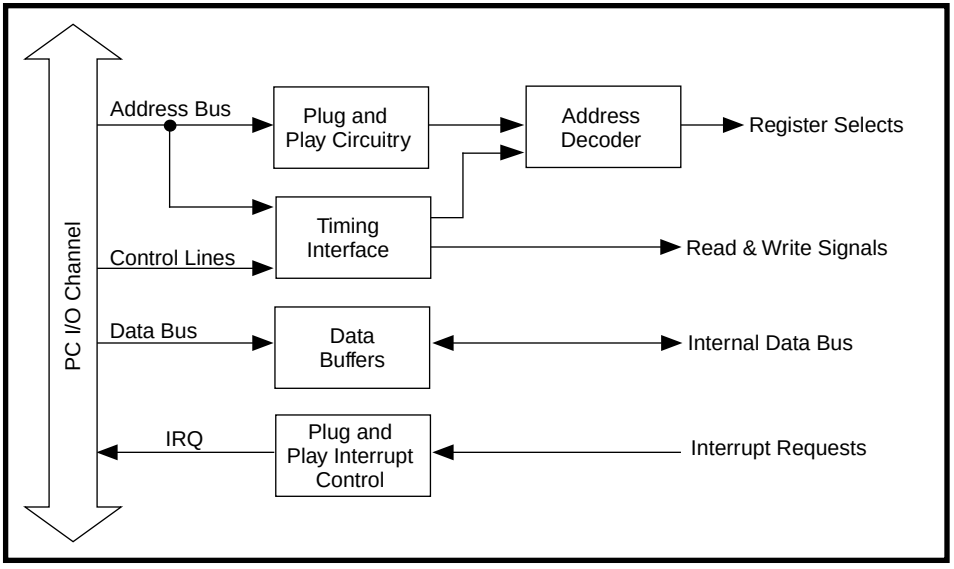



**Figure 3-2.** PC I/O Interface Circuitry Block Diagram

The circuitry consists of Plug and Play address decoders, data buffers, I/O channel interface timing control circuitry, and interrupt control circuitry. The circuitry monitors address lines SA4 through SA15 to generate the board enable signal, and uses lines SA0 through SA3 plus timing signals to generate the onboard register select signals and read/write signals. The data buffers control the direction of data transfer on the bidirectional data lines based on whether the transfer is a read or write operation.

The interrupt control circuitry routes any enabled interrupts to the selected interrupt request line. The PC-LPM-16PnP has six interrupt

request lines available: IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, and IRQ9. The PC-LPM-16PnP generates interrupts in three different situations:

- When an A/D conversion generates data that can be read from FIFO
- When an active low-level signal is detected on the EXTINT* line
- When a rising-edge signal is detected on counter 2 output

The PC-LPM-16PnP individually enables and clears each one of these interrupts. For more detailed information on generating interrupts externally, see the EXTINTEN bit of the Command Register 1 description in Appendix D, *Register-Level Programming*.

# Analog Input and Data Acquisition Circuitry

The PC-LPM-16PnP has 16 channels of analog input with 12-bit A/D conversion. Using the timing circuitry, the PC-LPM-16PnP can also automatically time multiple A/D conversions. Figure 3-3 shows a block diagram of the analog input and data acquisition circuitry.

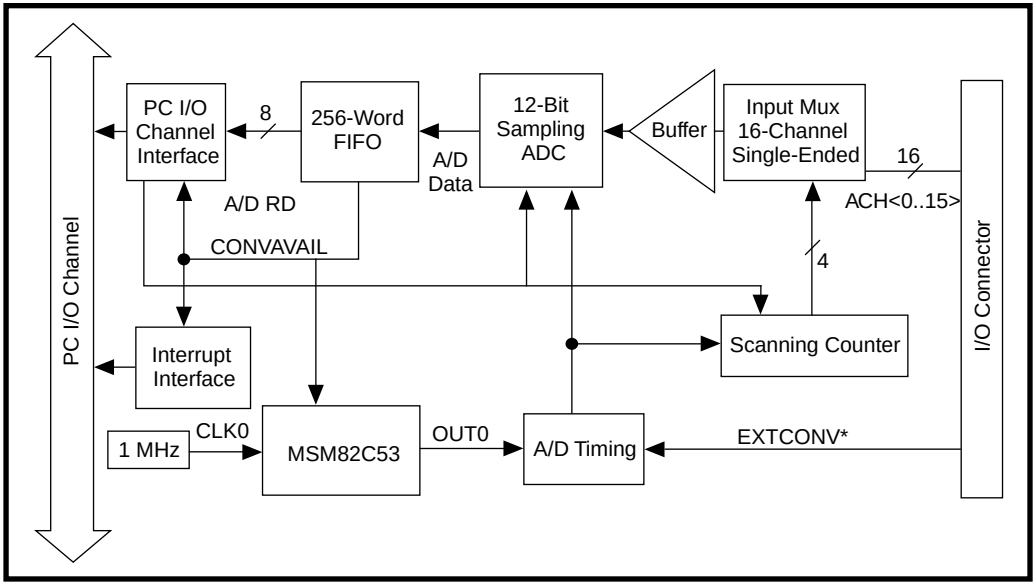



**Figure 3-3.** Analog Input and Data Acquisition Circuitry Block Diagram

## Analog Input Circuitry

The analog input circuitry consists of an input multiplexer, a jumper-selectable gain stage, and a 12-bit sampling ADC. The 12-bit output is sign-extended to 16 bits before it is stored in a 256-word deep FIFO memory.

The input multiplexer stage is made up of a CMOS analog input multiplexer and has 16 analog input channels (channels 0 through 15). With the input multiplexer stage, input overvoltage protection of ±45 V is available powered on, or ±35 V powered off.

The PC-LPM-16PnP uses a successive-approximation analog-to-digital converter (ADC). Software-selectable gains of 0.5, 1, and 2 for the input signal combined with the ADC's fixed input range of ±5 V yield four useful analog input signal ranges, 0 to 10 V, ±5 V, 0 to 5 V, and ±2.5 V.

When an A/D conversion is complete, the ADC clocks the result into the A/D FIFO. The A/D FIFO is 16 bits wide and 256 words deep. This FIFO serves as a buffer to the ADC and has two benefits. First, any time an A/D conversion is complete, the A/D FIFO saves the value for later reading, and the ADC can start a new conversion. Secondly, the A/D FIFO can collect up to 256 A/D conversion values before losing any information, thus giving the software some extra time (256 times the sample interval) to catch up with the hardware. If the A/D FIFO stores more than 256 values without the A/D FIFO being read, an error condition called A/D FIFO Overflow occurs and A/D conversion information is lost.

The A/D FIFO generates a signal that indicates when it contains conversion data. You can read the signal state from the PC-LPM-16PnP Status Register 1.

The output from the ADC is in two's complement format. In unipolar input mode (0 to 10 V or 0 to 5 V input range configuration), the data from the ADC is interpreted as a 12-bit positive number ranging from 0 to 4,095. In bipolar input mode (±5 or ±2.5 V input range configuration), the data from the ADC is interpreted as a two's complement number ranging from -2,048 to +2047. The ADC's output is always sign-extended to 16 bits by board circuitry so that data values read from the FIFO are 16 bits wide.

The ADC on the PC-LPM-16PnP includes calibration circuitry that makes it possible to minimize zero, full-scale, and linearity errors. The

ADC goes through a self-calibration cycle under software control. To properly use this ADC auto-calibration feature, you need an accurate input stage that does not introduce significant offset and gain errors. The analog input stage on the PC-LPM-16PnP maintains the required accuracy without trimpot adjustments.

## Data Acquisition Timing Circuitry

A data acquisition operation refers to the process of carefully timing the interval between successive A/D conversions. This interval is called the *sample interval*. The data acquisition timing circuitry consists of various clocks and timing signals that perform this timing. The PC-LPM-16PnP can perform two types of data acquisition: single-channel data acquisition and multichannel scanning data acquisition. Multichannel scanning data acquisition uses a counter to automatically switch between analog input channels during a data acquisition operation.

Data acquisition timing consists of signals that initiate a data acquisition operation and generate scanning clocks. Sources for these signals are supplied mainly by timers on the PC-LPM-16PnP board. One of the three counters of the onboard MSM82C53 is reserved for this purpose.

You can initiate an A/D conversion by a falling edge on the counter 0 output (OUT0) of the MSM82C53 onboard counter/timer chip, or by a rising edge on EXTCONV* input.

The sample-interval timer is a 16-bit down-counter that uses the onboard 1 MHz clock to generate sample intervals from 20 to 65,535 µs (see *Timing I/O Circuitry* later in this chapter for more timing information). Each time the sample-interval timer reaches zero, it generates a pulse and reloads with the programmed sample-interval count. This operation continues until you reprogram the counter.

As stated in Appendix D, *Register-Level Programming*, only counter 0 is required for data acquisition operations. The software must keep track of the number of conversions that have occurred and turn off counter 0 after it receives the required number of conversions.

## Single-Channel Data Acquisition

During single-channel data acquisition, the channel-select bits in Command Register 1 select the analog input channel before data acquisition begins. This multiplexer setting remains constant during the entire data acquisition process; therefore, all A/D conversion data is read from a single channel.

## Multichannel Scanning Data Acquisition

Multichannel data acquisition is performed when you enable scanned data acquisition. A scan counter on the board controls multichannel scanning.

For multichannel scanning operations, the scan counter decrements from the highest channel which you select through channel 0. Thus, the board can scan any number of channels from 2 to 16. Notice that the same analog input range is used for all channels in the scan sequence.

## Data Acquisition Rates

The maximum data acquisition rate (number of samples per second) is determined by the conversion period of the ADC plus the acquisition time of its track-and-hold stage. During multichannel scanning, the settling time of the input multiplexers and operational amplifier further limits the data acquisition rate. After the input multiplexers switch channels, the amplifier must be able to settle to the new input signal value to within 12-bit accuracy before performing an A/D conversion, or else it will not achieve 12-bit accuracy. The maximum data acquisition rate for both single-channel and multichannel operation is 50 kS/s. The signal will settle to ±1 LSB for any range if you do not exceed a signal sampling frequency of 50 kS/s. If you exceed the recommended data acquisition rate, the analog input circuitry may not perform at 12-bit accuracy. If you exceed this rate, an error condition called *overrun* occurs and you will lose some conversion data.

This recommended rate of 50 kS/s assumes that voltage levels on all the channels included in the scan sequence are within range and are driven by low-impedance sources. Signal levels outside the ranges on the channels included in the scan sequence adversely affect the input settling time. Similarly, channels driven by high-impedance signal sources should be allowed for greater settling time.

# Digital I/O Circuitry

The PC-LPM-16PnP has 16 digital I/O lines that are TTL-compatible. Pins DIN<0..7> of the I/O connector are digital input lines, and pins DOUT<0..7> are digital output lines. These lines are monitored or driven by the Digital Input Register or the Digital Output Register, respectively. Reading the Digital Input Register returns the current state of the DIN<0..7> lines. Writing to the Digital Output Register drives the new value onto the DOUT<0..7> lines. The external device may drive the EXTINT* signal to indicate the readiness of data transfer.

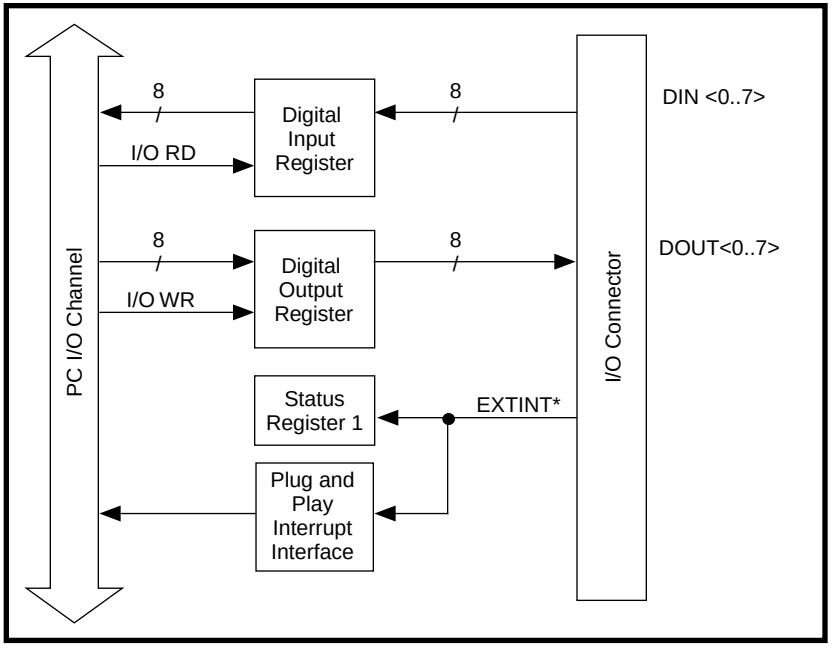



**Figure 3-4.** Digital I/O Circuitry Block Diagram

# Timing I/O Circuitry

The PC-LPM-16PnP uses an MSM82C53 Counter/Timer integrated circuit for data acquisition timing and for general-purpose timing I/O functions. Three counters on the circuit are available for general use, but the board can use only one of them, counter 0, internally for data acquisition timing. Figure 3-5 shows a block diagram of both groups of timing I/O circuitry.

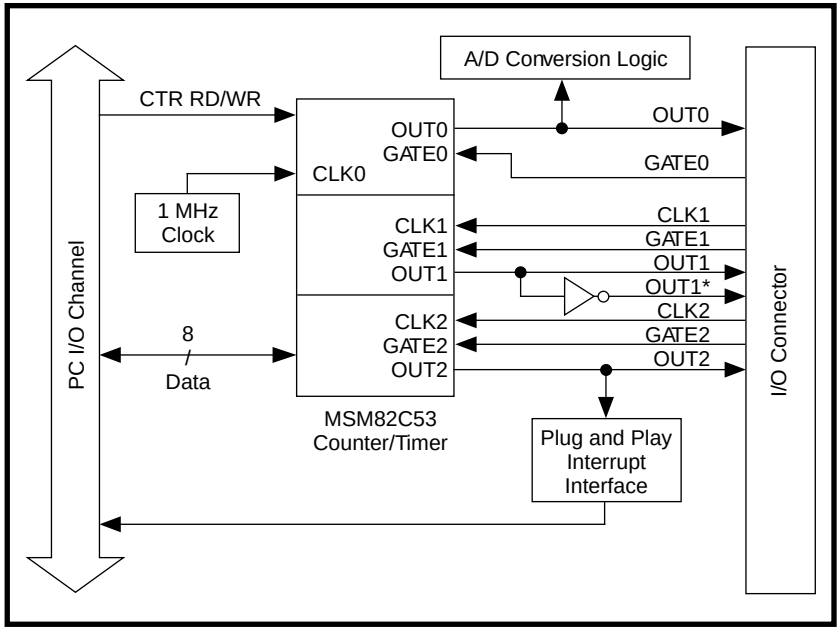



**Figure 3-5.** Timing I/O Circuitry Block Diagram

The MSM82C53 contains three independent 16-bit counter/timers and one 8-bit Mode Register. As shown in Figure 3-5, you can use counter 0 for data acquisition timing, and counters 1 and 2 are free for general use. You can program all three counter/timers to operate in several useful timing modes. The programming and operation of the MSM82C53 is presented in detail both in Appendix B, *MSM82C53 Data Sheet*, and Appendix D, *Register-Level Programming*.

The timebase for counter 0 uses a 1 MHz clock generated from an onboard oscillator. You must externally supply the timebases for counters 1 and 2 through the 50-pin I/O connector. Figure 3-6 diagrams the 16-bit counters in the MSM82C53.

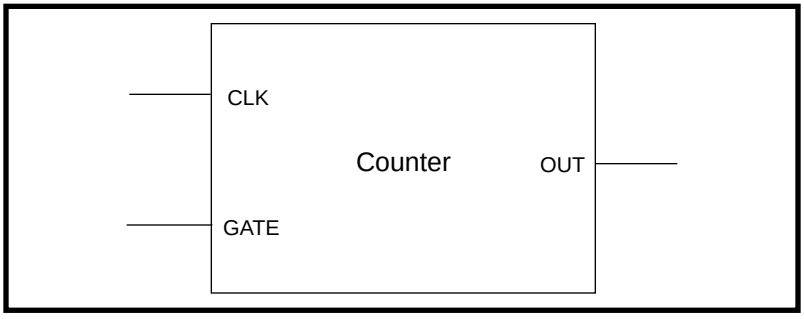



**Figure 3-6.** Counter Block Diagram

Each counter has a clock input pin, a gate input pin, and an output pin labeled CLK, GATE, and OUT, respectively. The MSM82C53 counters are numbered zero through two, and their GATE, CLK, and OUT pins are labeled GATE*N*, CLK*N*, and OUT*N*, where *N* is the counter number.

Chapter 4

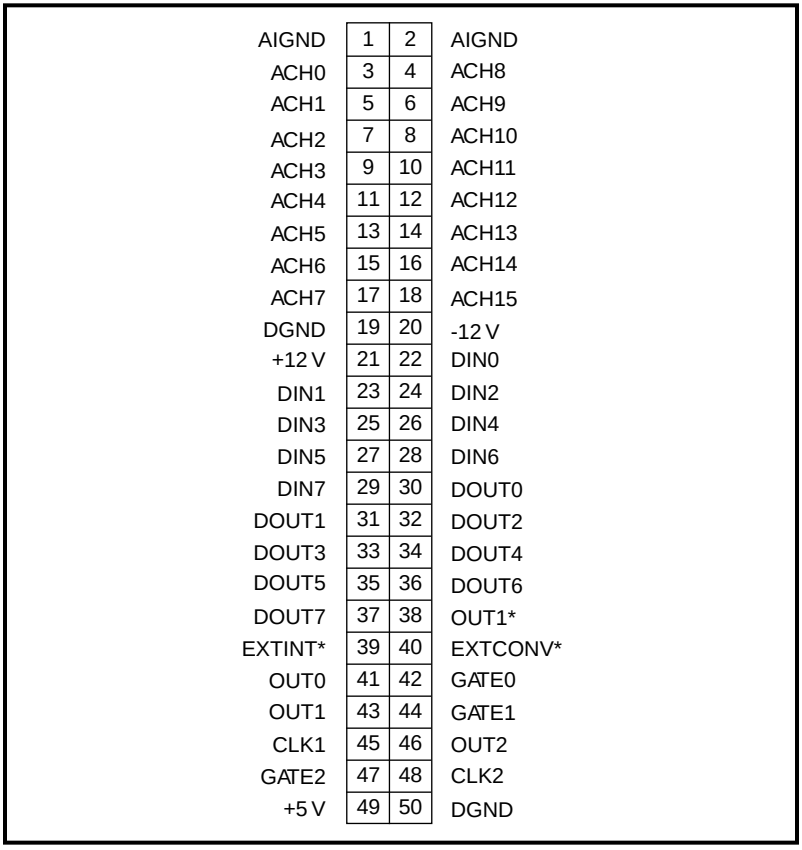
# Signal Connections

This chapter describes how to make input and output signal connections to your PC-LPM-16PnP board via the I/O connector.

## I/O Connector

Figure 4-1 shows the pin assignments for the PC-LPM-16PnP I/O connector. This connector is located on the back panel of the board and is accessible from the back of your computer after you have properly installed the board. Installation instructions are in Chapter 2, *Installation and Configuration*.

**Warning:** ***Connections that exceed any of the maximum ratings of input or output signals on the PC-LPM-16PnP can damage the board and the computer. This includes connecting any power signals to ground and vice versa. Each signal description in this section includes information about maximum input ratings. National Instruments is NOT liable for any damages resulting from any such signal connections.***



| | | | |
|---|---|---|---|
| AIGND | 1 | 2 | AIGND |
| ACH0 | 3 | 4 | ACH8 |
| ACH1 | 5 | 6 | ACH9 |
| ACH2 | 7 | 8 | ACH10 |
| ACH3 | 9 | 10 | ACH11 |
| ACH4 | 11 | 12 | ACH12 |
| ACH5 | 13 | 14 | ACH13 |
| ACH6 | 15 | 16 | ACH14 |
| ACH7 | 17 | 18 | ACH15 |
| DGND | 19 | 20 | -12 V |
| +12 V | 21 | 22 | DIN0 |
| DIN1 | 23 | 24 | DIN2 |
| DIN3 | 25 | 26 | DIN4 |
| DIN5 | 27 | 28 | DIN6 |
| DIN7 | 29 | 30 | DOUT0 |
| DOUT1 | 31 | 32 | DOUT2 |
| DOUT3 | 33 | 34 | DOUT4 |
| DOUT5 | 35 | 36 | DOUT6 |
| DOUT7 | 37 | 38 | OUT1* |
| EXTINT* | 39 | 40 | EXTCONV* |
| OUT0 | 41 | 42 | GATE0 |
| OUT1 | 43 | 44 | GATE1 |
| CLK1 | 45 | 46 | OUT2 |
| GATE2 | 47 | 48 | CLK2 |
| +5 V | 49 | 50 | DGND |

**Figure 4-1.** PC-LPM-16PnP I/O Connector Pin Assignments

# Signal Connection Descriptions

**Table 4-1.** Signal Connection Descriptions

| Pin | Signal | Reference | Description |
|---|---|---|---|
| 1–2 | AIGND | N/A | Analog Input Ground—The pins are connected to the analog input ground signal. ACH<0..15> signals should be referenced to AIGND. |
| 3–18 | ACH<0..15> | AGND | Analog Input Channels 0 through 15—These channels are single-ended. |
| 19 | DGND | N/A | Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply. |
| 20 | -12 V | DGND | -12 VDC Power Supply Output Pin—The maximum current is 5.0 mA. |
| 21 | +12 V | DGND | +12 VDC Power Supply from the Computer Bus—This power line has a 0.5 A self-resetting fuse in series. |
| 22–29 | DIN<0..7> | DGND | Digital Input Data Lines—These signals are TTL-compatible, digital input lines. DIN7 is the MSB, DIN0 the LSB. |
| 30–37 | DOUT<0..7> | DGND | Digital Output Data Lines—These signals are TTL-compatible, digital output lines. DOUT7 is the MSB, DOUT0 the LSB. |
| 38 | OUT1* | DGND | Output of Counter 1—This signal outputs the inverted programmed waveform of counter 1. |
| 39 | EXTINT* | DGND | External Interrupt—This pin is used for input of the external interrupt signal. |

**Table 4-1.** Signal Connection Descriptions (Continued)

| Pin | Signal | Reference | Description |
|---|---|---|---|
| 40 | EXTCONV* | DGND | External Convert Signal—This input signal externally initiates an A/D conversion. |
| 41 | OUT0 | DGND | Output of Counter 0—This signal outputs the programmed waveform of counter 0. |
| 42 | GATE0 | DGND | Counter 0 Gate Input—This signal controls the starting, interruption, and restarting of counter 0. |
| 43 | OUT1 | DGND | Output of Counter 1—This signal outputs the programmed waveform of counter 1. |
| 44 | GATE1 | DGND | Counter 1 Gate Input—This signal controls the starting, interruption, and restarting of counter 1. |
| 45 | CLK1 | DGND | Counter 1 Clock Input—This pin is the clock input for counter 1. |
| 46 | OUT2 | DGND | Counter 2 Output—This pin is the output of counter 2. |
| 47 | GATE2 | DGND | Counter 2 Gate Input—This signal controls the starting, interruption, and restarting of counter 2. |
| 48 | CLK2 | DGND | Counter 2 Clock Input—This pin is the clock input for counter 2. |
| 49 | +5 V | DGND | +5 Volts—This is the +5 VDC power supply from the computer bus. This power line has a 1.0 A self-resetting fuse in series. |
| 50 | DGND | N/A | Digital Ground—This pin is connected to the digital ground signal. |
| **Note:** ***An asterisk (*) indicates that the signal is active low.*** | | | |

The connector pins can be grouped into categories of analog input signal pins, digital I/O signal pins, and timing I/O signal pins. Signal connection guidelines for each of these groups follow.

## Analog Input Signal Connections

Pins 3 through 18 are analog input signal pins for the ADC. Pins 1 and 2 are analog common signals. You can use these pins for a general analog power ground tie to the PC-LPM-16PnP. Pins 3 through 18 are tied to the 16 single-ended analog input channels of the input multiplexer through 4.7 kΩ series resistors. These resistors limit input current to the multiplexer. Pin 40 triggers conversions slightly after this signal makes a low-to-high transition. You can only use this pin to cause conversions, not as a monitor to detect conversions caused by the onboard sample-interval timer. Refer to Figure 4-4 for more information about EXTCONV* timing.

The following input ranges and maximum ratings apply to inputs ACH<0..15>:

| | |
|---|---|
| Input signal range | Bipolar input: ±5 V or ±2.5 V<br>Unipolar input: 0 to 10 V<br>or 0 to 5 V |
| Maximum input voltage rating | ±45 V powered on<br>±35 V powered off |

**Warning:** ***Exceeding the input signal range, even on unused analog input channels, distorts other input signals. Exceeding the maximum input voltage rating can damage your board and the computer. National Instruments is NOT liable for any damages resulting from such signal connections.***

### Connections for Signal Sources

Figure 4-2 shows how to connect a signal source to your PC-LPM-16PnP. When you connect grounded signal sources, carefully observe the polarity to avoid shorting the signal source output.

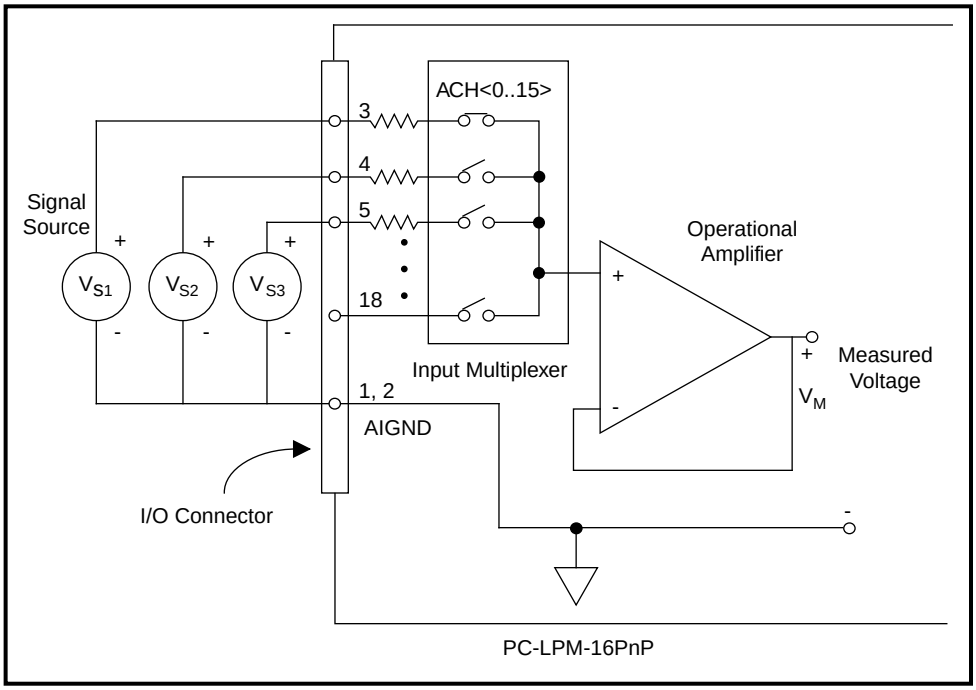



**Figure 4-2.** Analog Input Signal Connections

## Digital I/O Signal Connections

See Table 4-1 for the digital I/O pin descriptions.

The following specifications and ratings apply to the digital I/O lines:

- Absolute maximum voltage input rating — +7.0 V with respect to DGND; -0.5 V with respect to DGND
- Digital input compatibility — TTL-compatible
- Input current (high or low level) — ±10 μA
- Digital output compatibility — TTL-compatible
- Output current source capability — 8 mA, at $V_{OH}$ = 2.7 V
- Output current sink capability — 6 mA, at $V_{OL}$ = 0.5 V

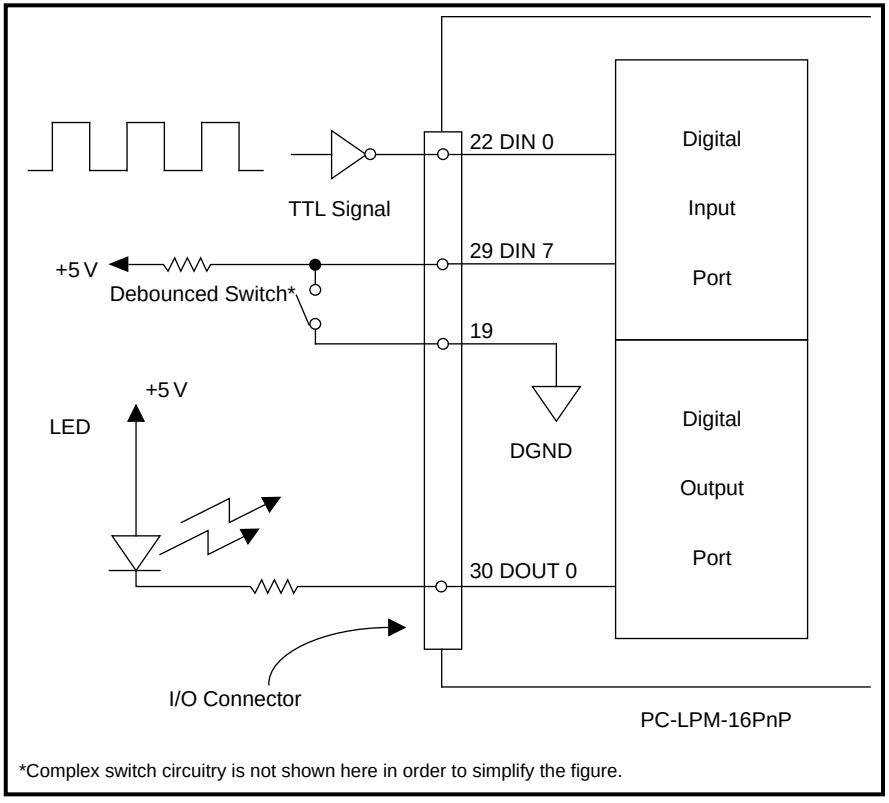



**Figure 4-3.** Analog Input Signal Connections

Figure 4-3 shows the connections of the digital input port and digital output port. Digital input applications include receiving TTL signals and sensing external device states such as the switch in Figure 4-3. Digital output applications include sending TTL signals and driving external devices such as the LED shown in Figure 4-3.

## Power Connections

Pin 49 of the I/O connector supplies +5 V from the computer I/O channel power supply. Pin 20 of the I/O connector supplies +12 V from the computer I/O channel power supply. The -12 V is supplied from the computer I/O power supply with a resistor in series. These pins are referenced to DGND and can be used to power external digital circuitry. The +5 V supply at the I/O connector has a 1.0 A protection fuse in series. The +12 V supply at the I/O connector has a 0.5 A protection

fuse in series. Both fuses are self-resetting; simply remove the circuit causing the heavy current load and the fuse will reset itself.

## Power Rating

The following table shows the maximum current for each power line at the I/O connector.

| Power Line | Maximum Current |
|---|---|
| +5 V (self-resetting fuse at 1.0 A) | 1.0 A* |
| +12 V (self-resetting fuse at 0.5 A) | 0.5 A* |
| -12 V | 5.0 mA |
| * The actual current available from these signals may be less, depending on your computer. Notice also that any current drawn from these lines adds to the power requirements from the computer. | |

## Timing Connections

Pins 38 through 48 of the I/O connector are connections for timing I/O signals. The timing input and output of the PC-LPM-16PnP is designed around an MSM82C53 counter/timer integrated circuit. All three counters of the circuit are available at the I/O connector. One of these counters, counter 0, is used for data acquisition timing. Pin 39 carries an external signal that can be used for data acquisition timing in place of counter 0. Pins 38 and 41 through 48 carry general-purpose timing signals. These signals are explained in the *General-Purpose Timing Signal Connections and General-Purpose Counter Timing Signals* section later in this chapter.

### Data Acquisition Timing Connections

Counter 0 on the MSM82C53 counter/timer is used as a sample-interval counter in timed A/D conversions. In addition to counter 0, EXTCONV* can externally time conversions. See Appendix D, *Register-Level Programming*, for the programming sequence needed to enable this input. Figure 4-4 shows the timing requirements for the EXTCONV* input. An A/D conversion is initiated by a rising edge on the EXTCONV*. The data from this conversion is latched into the FIFO memory within 20 µs. The EXTCONV* input is a TTL-compatible signal.

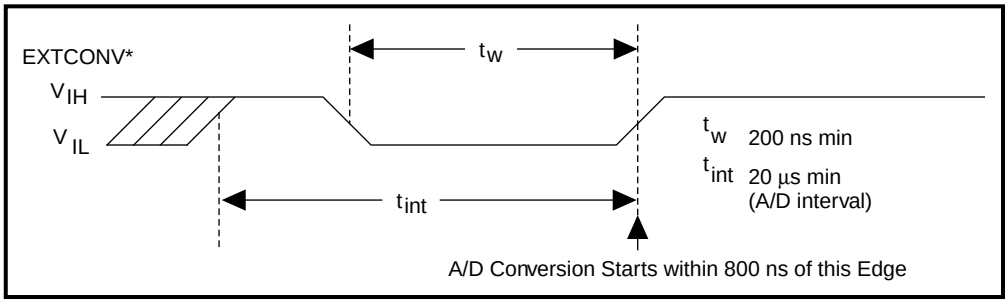



**Figure 4-4.** EXTCONV* Signal Timing

## General-Purpose Timing Signal Connections and General-Purpose Counter Timing Signals

The general-purpose timing signals include the GATE, CLK, and OUT signals for the three MSM82C53 counters, except CLK of counter 0 is not available on the I/O connector. You can use the counter/timers for general-purpose applications such as pulse and square wave generation, event counting, and pulse-width, time-lapse, and frequency measurement. For these applications, user signals sent from the I/O connector on the CLK and GATE pins go to the counters, and the counters are user-programmable for various operations. The single exception is counter 0, which has an internal 1 MHz clock.

Chapter 3, *Theory of Operation*, briefly describes the MSM82C53 counter/timer. For detailed information on this counter/timer, see Appendix B, *MSM82C53 Data Sheet*.

For pulse and square wave generation, program a counter to generate a timing signal at its OUT output pin.

For event counting, program a counter to count the rising or falling edges applied to any of the MSM82C53 CLK inputs. You can then read the counter value to determine the number of edges that have occurred. You can gate the counter operation on and off during event counting. Figure 4-5 shows connections for a typical event-counting operation where a switch is used to gate the counter on and off.

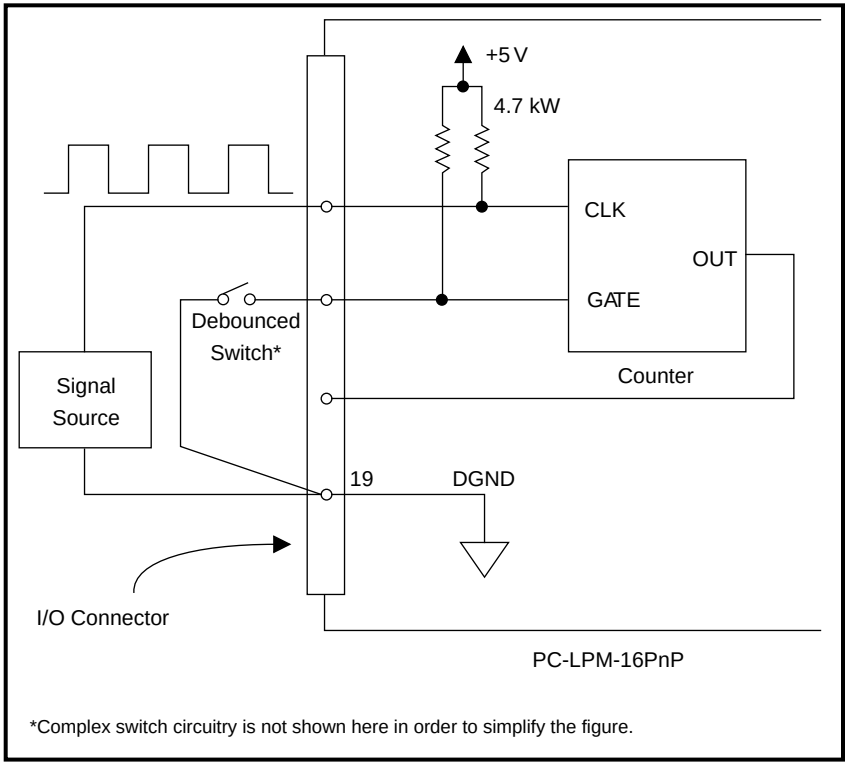



**Figure 4-5.** Event-Counting Application with External Switch Gating

Perform pulse-width measurement by level gating to trigger the counter. Apply the pulse to be measured to the counter GATE input. Load the counter with the known count and program it to count down while the signal at the GATE input is high. The pulse width equals the counter difference (loaded value minus read value) multiplied by the CLK period.

For time-lapse measurement, program a counter to be edge-gated. Apply an edge to the counter GATE input to start the counter. You can program the counter to start counting after receiving a low-to-high edge. The time lapse since receiving the edge equals the counter value difference (loaded value minus read value) multiplied by the CLK period.

For frequency measurement, program a counter to be level-gated and count the number of falling edges in a signal applied to a CLK input. The gate signal you apply to the counter GATE input is of known

duration. In this case, program the counter to count falling edges at the CLK input while the gate is applied. The frequency of the input signal then equals the count value divided by the gate period. Figure 4-6 shows the connections for a frequency measurement application. You could also use a second counter to generate the gate signal in this application.

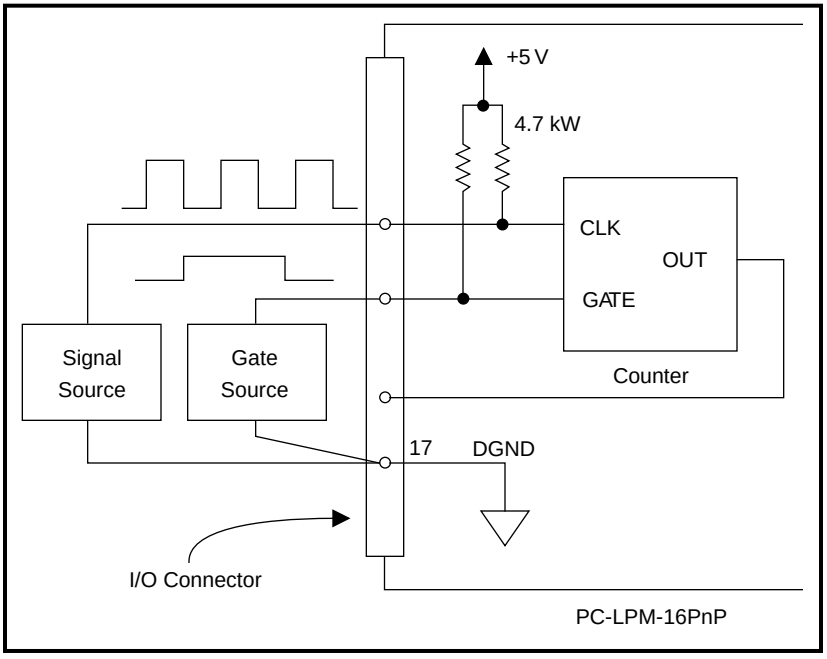



**Figure 4-6.** Frequency Measurement Application

4.7 kΩ resistors pull up the GATE and CLK pins to +5 V.

Figure 4-7 shows the timing requirements for the GATE and CLK input signals and the timing specifications for the OUT output signals.

The following specifications and ratings apply to the MSM82C53 I/O signals:

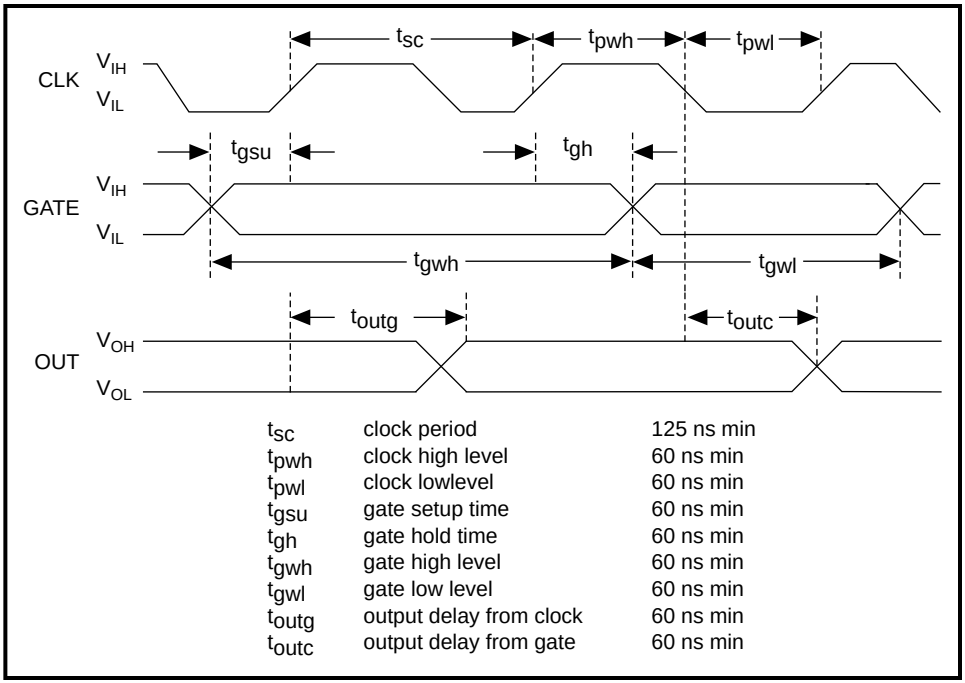
- Absolute maximum voltage input rating -0.5 to 7.0 V with respect to DGND

MSM82C53 digital input specifications (referenced to DGND):

- $V_{IH}$ input logic high voltage 2.2 V min
- $V_{IL}$ input logic low voltage 0.8 V max
- Input load current ±10.0 μA max

MSM82C53 digital output specifications (referenced to DGND):

- $V_{OH}$ output logic high voltage 3.7 V min
- $V_{OL}$ output logic low voltage 0.45 V max
- $I_{OH}$ output source current, at $V_{OH}$ 1.0 mA max
- $I_{OL}$ output sink current, at $V_{OL}$ 4.0 mA max




| | | |
|---|---|---|
| $t_{sc}$ | clock period | 125 ns min |
| $t_{pwh}$ | clock high level | 60 ns min |
| $t_{pwl}$ | clock lowlevel | 60 ns min |
| $t_{gsu}$ | gate setup time | 60 ns min |
| $t_{gh}$ | gate hold time | 60 ns min |
| $t_{gwh}$ | gate high level | 60 ns min |
| $t_{gwl}$ | gate low level | 60 ns min |
| $t_{outg}$ | output delay from clock | 60 ns min |
| $t_{outc}$ | output delay from gate | 60 ns min |

**Figure 4-7.** General-Purpose Timing Signals

The GATE and OUT signals in Figure 4-7 are referenced to the rising edge of the CLK signal.

Appendix A

# Specifications

This appendix lists the PC-LPM-16PnP specifications. These specifications are typical at 25° C unless otherwise specified. The operating temperature range is 0° to 70° C.

## PC-LPM-16PnP Board

### Analog Input

#### Input Characteristics

Number of channels ..... 16 single-ended

Type of ADC..... Successive approximation

Resolution ..... 12 bits, 1 in 4,096

Max sampling rate..... 50 kS/s

Input signal ranges ..... ±5 V, ±2.5 V, 0 to 10 V, or 0 to 5 V, software-selectable

Input coupling ..... DC

Overvoltage protection ..... ±45 V powered on, ±35 V powered off

Inputs protected ..... ACH<0..15>

FIFO buffer size ..... 256 S

Data transfers ..... Interrupts, programmed I/O

#### Transfer Characteristics

Relative accuracy ..... ±1.0 LSB typ, ±1.5 LSB max

Integral nonlinearity ..... ±0.5 LSB max

Differential nonlinearity ..... ±1.0 LSB max

(For more information on nonlinearity and quantization error, see the *Explanation of Analog Input Specifications* section)

Offset error after calibration..... ±1.0 LSB typ, ±2.0 LSB max

Gain error (relative to calibration reference)
After calibration
0 to 5 V and ±5 V range .....±1.0 LSB typ, ±2.0 LSB max
All other ranges.....±2.0 of reading typ, ±4.0 max

☞ **Note:** ***LSB refers to the least significant bit of a 12-bit conversion value in the preceding specifications. LSB is equivalent to 2.44 mV in the 10 V range (0 to 10 V or ±5 V) and 1.22 mV in the 5 V ranges (0 to 5 V or ±2.5 V).***

## Amplifier Characteristics

Input impedance.....0.1 GΩ in parallel with 40 pF typ

## Dynamic Characteristics

Bandwidth
Gain = (-3 dB).....200 kHz typ
Settling time to ±1.0 LSB
for full-scale step .....20 µs max at all ranges
System noise .....0.1 LSB rms for all ranges

## Stability

Recommended warm-up time.....15 min.
Onboard calibration reference
Level .....5.000 V (±2.5 mV)
Temperature coefficient .....20 ppm/°C max
Long-term stability.....15 ppm/$\sqrt{1,000\ \text{h}}$ typ

# Digital I/O

Number of channels .....8 input and 8 output
Compatibility .....TTL
Configuration.....1 8-bit input port, 1 8-bit output port
Absolute max ratings .....+7.0 V with respect to DGND; voltage input rating: -0.5 V with respect to DGND

Digital logic levels .....

| Level | Minimum | Maximum |
|---|---|---|
| Input low voltage | 0 V | 0.8 V |
| Input high voltage | 2 V | 5.0 V |
| Input low current ($V_{in}$ = 0 V) | — | ±10 µA |
| Input high current ($V_{in}$ = 5 V) | — | ±10 µA |

| Level | Minimum | Maximum |
|---|---|---|
| Output low voltage ($I_{out}$ = 4 mA) | — | 0.4 V |
| Output high voltage ($I_{out}$ = 4 mA) | 3.7 V | — |

## Timing I/O

Number of channels ..... 3 counter/timers (1 dedicated to analog input)

Resolution ..... 16 bits

Compatibility ..... TTL, gate and source pulled high with 4.7 kΩ resistors

Input logic low voltage..... 0.8 V max

Input logic high voltage..... 2.2 V min

Output logic low voltage
at output current = 4.0 mA ..... 0.45 V max

Output logic high voltage
at output current = -1.0 mA ..... 3.7 V min

Base clocks available ..... 1 MHz ±0.01%

Max source frequency ..... 8 MHz

Min source pulse duration ..... 60 ns

Min gate pulse duration..... 50 ns

Data transfers ..... Programmed I/O

## Bus Interface

Type..... Slave

## Power Requirement

+5 VDC (±10%)..... 50 mA typ
+12 VDC (±5%)..... 15 mA typ
-12 VDC (±5%) ..... 15 mA typ

☞ **Note:** ***These numbers do not include an additional 1 A from the 5 V power supply. The 50-pin I/O connector can draw 0.5 A from the +12 V supply.***

## Physical

Dimensions ..... 11.0 by 9.9 cm (4.4 by 3.9 in.)
I/O connector ..... 50-pin D male ribbon cable connector

## Environment

Operating temperature..... 0° to 70° C
Storage temperature ..... -55° to 150° C
Relative humidity..... 5% to 90% noncondensing

## Explanation of Analog Input Specifications

*Relative accuracy* is a measure of the linearity of an ADC. However, relative accuracy is a tighter specification than a *nonlinearity* specification. Relative accuracy indicates the maximum deviation from a straight line for the analog-input-to-digital-output transfer curve. If a ADC has been calibrated perfectly, then this straight line is the ideal transfer function, and the relative accuracy specification indicates the worst deviation from the ideal that the ADC permits.

A relative accuracy specification of ±1 LSB is roughly equivalent to (but not the same as) a ±1/2 LSB nonlinearity or integral nonlinearity specification because relative accuracy encompasses both nonlinearity and variable quantization uncertainty, a quantity often mistakenly assumed to be exactly ±1/2 LSB. Although quantization uncertainty is ideally ±1/2 LSB, it can be different for each possible digital code and is actually the analog width of each code. Thus, it is more specific to use relative accuracy as a measure of linearity than it is to use what is normally called nonlinearity, because relative accuracy ensures that the

*sum* of quantization uncertainty and A/D conversion error does not exceed a given amount.

*Integral nonlinearity* in a ADC is an often ill-defined specification that is supposed to indicate a converter's overall A/D transfer linearity. The manufacturers of the ADC chips used by National Instruments specify their integral nonlinearity by stating that the analog center of any code will not deviate from a straight line by more than ±1 LSB. This specification is misleading because although a particularly wide code's center may be found within ±1 LSB of the ideal, one of its edges may be well beyond ±1 LSB; thus, the ADC would have a relative accuracy of that amount. National Instruments tests its boards to ensure that they meet all three linearity specifications defined in this appendix; specifications for integral nonlinearity are included primarily to maintain compatibility with a convention of specifications used by other board manufacturers. Relative accuracy, however, is much more useful.

*Differential nonlinearity* is a measure of deviation of code widths from their theoretical value of 1 LSB. The width of a given code is the size of the range of analog values that can be input to produce that code, ideally 1 LSB. A specification of ±1 LSB differential nonlinearity ensures that no code has a width of 0 LSBs (that is, no missing codes) and that no code width exceeds 2 LSBs.

*System noise* is the amount of noise seen by the ADC when there is no signal present at the input of the board. The amount of noise that is reported directly (without any analysis) by the ADC is not necessarily the amount of real noise present in the system, unless the noise is ≥0.5 LSB rms. Noise that is less than this magnitude produces varying amounts of flicker, and the amount of flicker seen is a function of how near the real mean of the noise is to a code transition. If the mean is near or at a transition between codes, the ADC flickers evenly between the two codes, and the noise is seen as very nearly 0.5 LSB. If the mean is near the center of a code and the noise is relatively small, very little or no flicker is seen, and the noise is reported by the ADC as nearly 0 LSB. From the relationship between the mean of the noise and the measured rms magnitude of the noise, the character of the noise can be determined. National Instruments has determined that the character of the noise in the PC-LPM-16PnP is fairly Gaussian, so the noise specifications given are the amounts of pure Gaussian noise required to produce our readings.

To illustrate these definitions, Figure A-1 shows a portion of the analog-input-to-digital-output transfer curve for an ideal, ADC overlaid on the transfer curve of a hypothetical, typical, ADC. As shown in Figure A-1, the relative accuracy is the deviation of the code transition voltage from the center of the code for an ideal ADC, expressed in terms of LSBs. Notice that in this case, an ideal ADC has a relative accuracy of ±1/2 LSB, because this definition of relative accuracy encompasses both nonlinearity and quantization uncertainties. Integral nonlinearity is the worst case deviation of the center of the code from the ideal center, expressed in terms of LSBs. Finally, the differential nonlinearity is deviation of a code width from ideal code width, expressed in terms of LSBs.

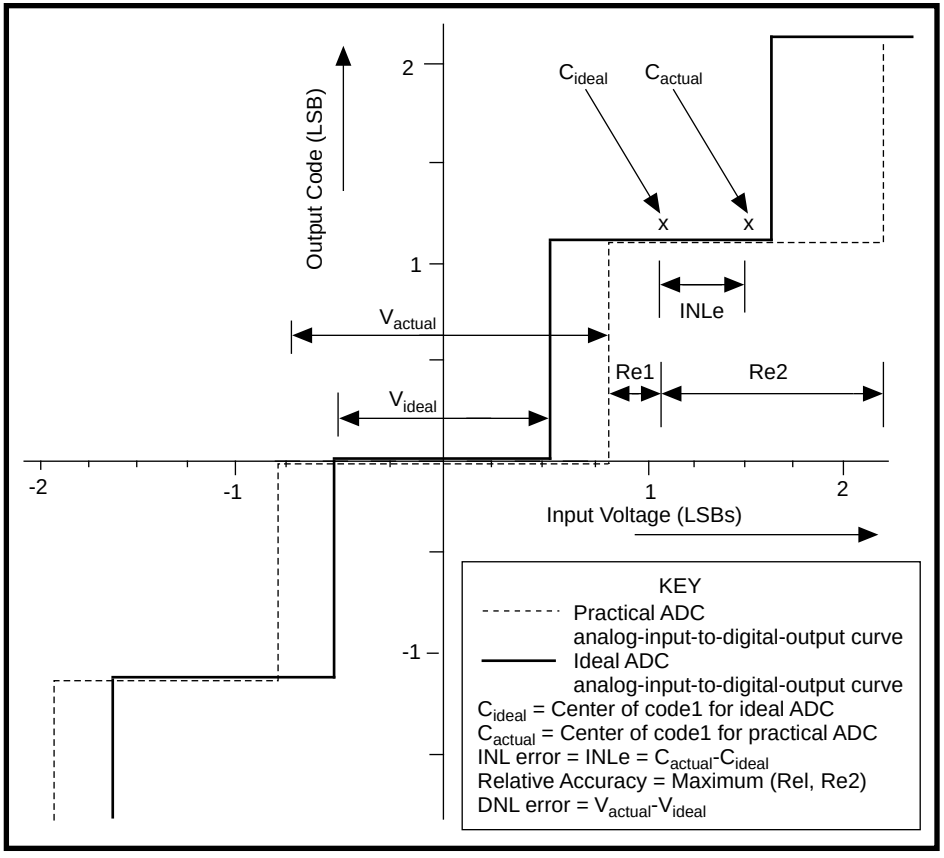



**Figure A-1.** ADC Errors

# MSM82C53 Data Sheet

*Appendix*
**B**

This appendix contains a manufacturer data sheet for the MSM82C53* CMOS programmable interval timer (OKI Semiconductor). This timer is used on the PC-LPM-16PnP board.

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**OKI semiconductor**

# MSM82C53-2RS/GS/JS

## CMOS PROGRAMMABLE INTERVAL TIMER

## GENERAL DESCRIPTION

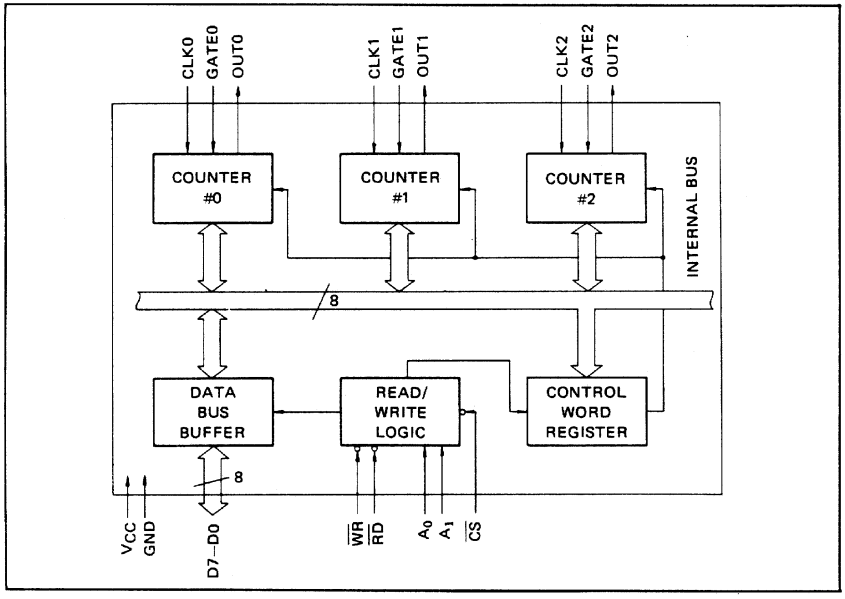
The MSM82C53-2RS/GS/JS is programmable universal timers designed for use in microcomputer systems. Based on silicon gate CMOS technology, it requires a standby current of only 100 μA (max.) when the chip is in the nonselected state. During timer operation, power consumption is still very low with only 8 mA (max.) at 8 MHz of current required.

The device consists of three independent counters, and can count up to a maximum of 8 MHz (MSM82C53-2) The timer features six different counter modes, and binary count/BCD count functions. Count values can be set in byte or word units, and all functions are freely programmable.

## FEATURES

- Maximum operating frequency of 8 MHz (MSM82C53-2)
- High speed and low power consumption achieved through silicon gate CMOS technology
- Completely static operation
- Three independent 16-bit down-counters
- 3V to 6V single power supply
- Six counter modes abailable for each counter
- Binary and decimal counting possible
- 24 pin Plastic DIP (DIP24-P-600): MSM82C53-2RS
- 28 pin Plastic QFJ (QFJ28-P-S450): MSM82C53-2JS
- 32 pin-V Plastic SOP (SSOP32-P-430-VK): MSM82C53-2GS-VK

## FUNCTIONAL BLOCK DIAGRAM

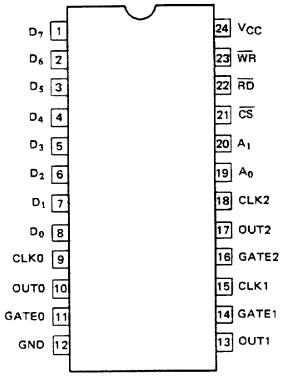



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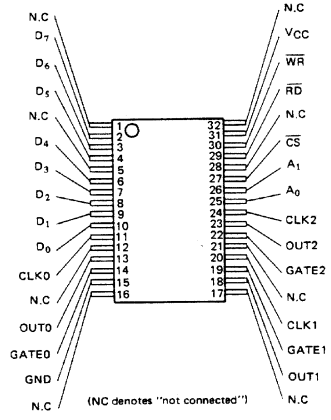
■ I/O-MSM82C53-2RS/GS/JS ■

## PIN CONFIGURATION (Top View)

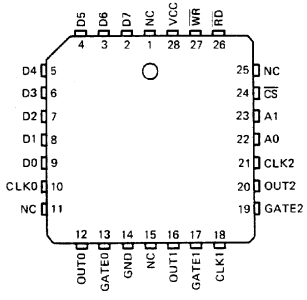
24 pin Plastic DIP




32 pin Plastic SOP




28 pin Plastic QFJ




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■ I/O-MSM82C53-2RS/GS/JS ■

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | MSM82C53-2RS | MSM82C53-2GS | MSM82C53-2JS | |
| Ssupply Voltage | $V_{CC}$ | Respect to GND | −0.5 to +7 | | | V |
| Input Voltage | $V_{IN}$ | | −0.5 to $V_{CC}$ + 0.5 | | | V |
| Output Voltage | $V_{OUT}$ | | −0.5 to $V_{CC}$ + 0.5 | | | V |
| Storage Temperature | $T_{stg}$ | | −55 to +150 | | | °C |
| Power Dissipation | $P_D$ | Ta = 25°C | 0.9 | 0.7 | 0.9 | W |

## OPERATING RANGES

| Parameter | Symbol | Limits | Conditions | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 3 to 6 | $V_{IL}$ = 0.2V, $V_{IH}$ = $V_{CC}$ − 0.2V, operating frequency 2.6 MHz | V |
| Operating Temperature | $T_{OP}$ | −40 to +85 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5 | 5.5 | V |
| Operating Temperature | $T_{OP}$ | −40 | +25 | +85 | °C |
| "L" Input Voltage | $V_{IL}$ | −0.3 | | +0.8 | V |
| "H" Input Voltage | $V_{IH}$ | 2.2 | | $V_{CC}$ + 0.3 | V |

## DC CHARACTERISTICS

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| "L" Output Voltage | $V_{OL}$ | $I_{OL}$ = 4mA | | | | 0.45 | V |
| "H" Output Voltage | $V_{OH}$ | $I_{OH}$ = −1mA | | 3.7 | | | V |
| Input Leak Current | $I_{LI}$ | $0 \leq V_{IN} \leq V_{CC}$ | $V_{CC}$=4.5V to 5.5V | −10 | | 10 | μA |
| Output Leak Current | $I_{LO}$ | $0 \leq V_{OUT} \leq V_{CC}$ | Ta=−40°C to +85°C | −10 | | 10 | μA |
| Standby Supply Current | $I_{CCS}$ | $\overline{CS} \geq V_{CC}$ −0.2V<br>$V_{IH} \geq V_{CC}$ − 0.2V<br>$V_{IL} \leq$ 0.2V | | | | 100 | μA |
| Operating Supply Current | $I_{CC}$ | $t_{CLK}$ = 125 ns $C_L$ = 0pF | | | | 8 | mA |

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■ I/O-MSM82C53-2RS/GS/JS ■

## AC CHARACTERISTICS

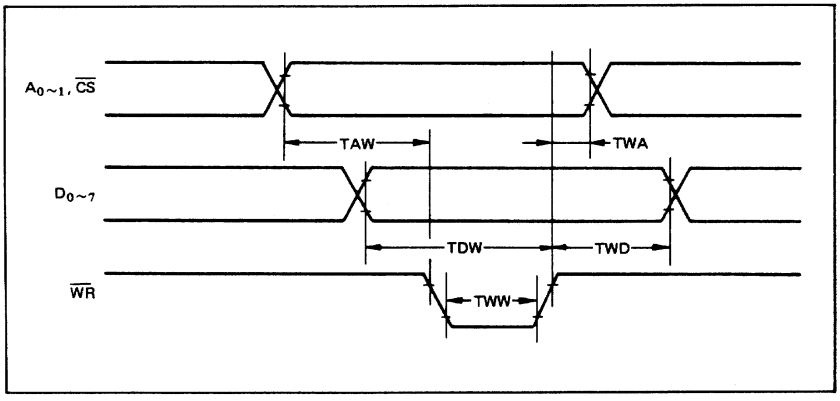
($V_{CC}$ = 4.5V ~ 5.5V, Ta = –40 ~ +85°C)

| Parameter | Symbol | MSM82C53-2 Min. | MSM82C53-2 Max. | Unit | Conditions | |
|---|---|---|---|---|---|---|
| Address Set-up Time before reading | TAR | 30 | | ns | Read cycle | $C_L$ = 150pF |
| Address Hold Time after reading | TRA | 0 | | ns | | |
| Read Pulse Width | TRR | 150 | | ns | | |
| Read Recovery Time | TRVR | 200 | | ns | | |
| Address Set-up Time before writing | TAW | 0 | | ns | Write cycle | |
| Address Hold Time after writing | TWA | 20 | | ns | | |
| Write Pulse Width | TWW | 150 | | ns | | |
| Data Input Set-up Time before writing | TDW | 100 | | ns | | |
| Data Input Hold Time after writing | TWD | 20 | | ns | | |
| Write Recovery time | TRVW | 200 | | ns | | |
| Clock Cycle Time | TCLK | 125 | D.C. | ns | Clock and gate timing | |
| Clock "H" Pulse Width | TPWH | 60 | | ns | | |
| Clock "L" Pulse Width | TPWL | 60 | | ns | | |
| "H" Gate Pulse Width | TGW | 50 | | ns | | |
| "L" Gate Pulse Width | TGL | 50 | | ns | | |
| Gate Input Set-up Time before clock | TGS | 50 | | ns | | |
| Gate Input Hold Time after clock | TGH | 50 | | ns | | |
| Output Delay Time after reading | TRD | | 120 | ns | Delay time | |
| Output Floating Delay Time after reading | TDF | 5 | 90 | ns | | |
| Output Delay Time after gate | TODG | | 120 | ns | | |
| Output Delay Time after clock | TOD | | 150 | ns | | |
| Output Delay Time after address | TAD | | 180 | ns | | |

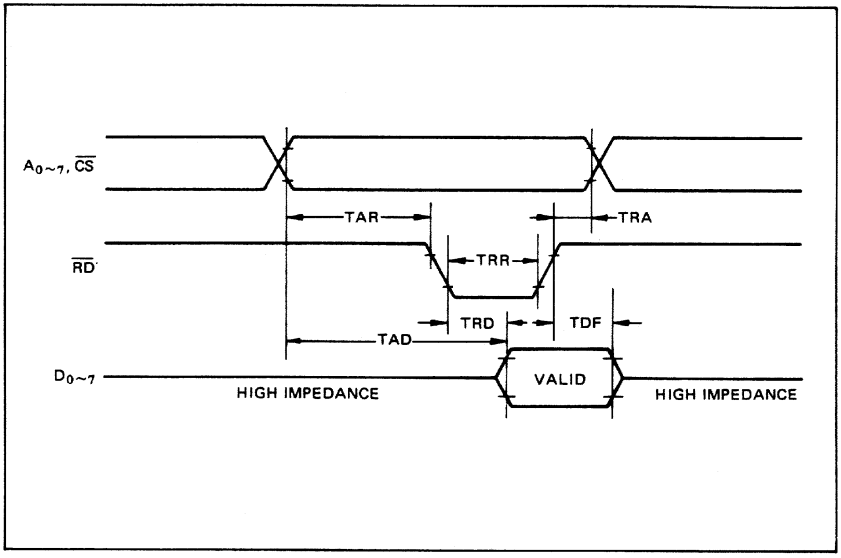
**Note:** Timing measured at $V_L$ = 0.8V and $V_H$ = 2.2V for both inputs and outputs.

## TIME CHART

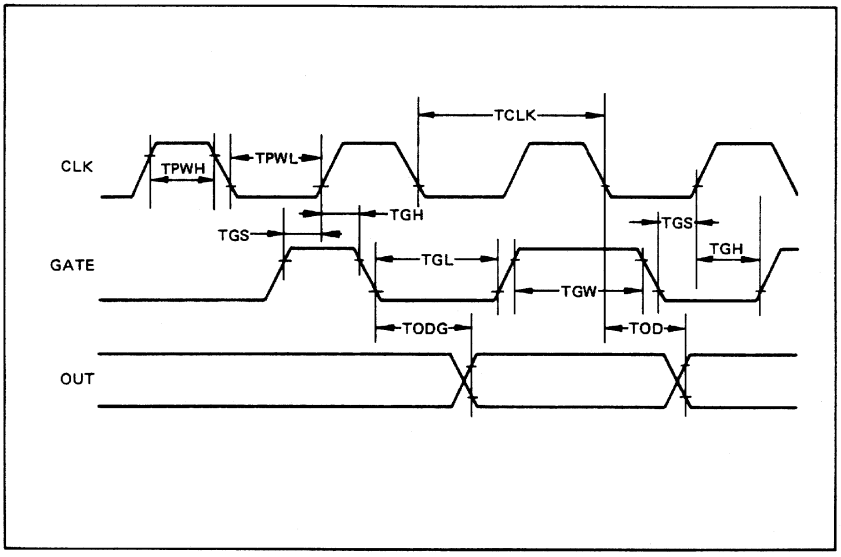
**Write Timing**



**Read Timing**




**Clock & Gate Timing**

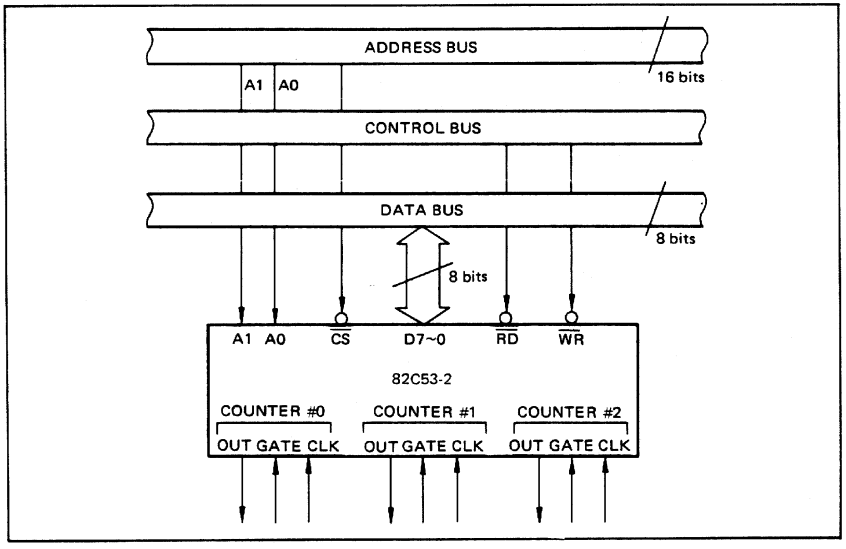


■ I/O-MSM82C53-2RS/GS/JS ■

## DESCRIPTION OF PIN FUNCTIONS

| Pin Symbol | Name | Input/output | Function |
|---|---|---|---|
| D7 ~ D0 | Bidirectional data bus | Input/output | Three-state 8-bit bidirectional data bus used when writing control words and count values, and reading count values upon reception of $\overline{WR}$ and $\overline{RD}$ signals from CPU. |
| $\overline{CS}$ | Chip select input | Input | Data transfer with the CPU is enabled when this pin is at low level. When at high level, the data bus ($D_0$ thru $D_7$) is switched to high impedance state where neither writing nor reading can be executed. Internal registers, however, remain unchanged. |
| $\overline{RD}$ | Read input | Input | Data can be transferred from MSM82C53 to CPU when this pin is at low level. |
| $\overline{WR}$ | Write input | Input | Data can be transferred from CPU to MSM82C53 when this pin is at low level. |
| A0, A1 | Address input | Input | One of the three internal counters or the control word register is selected by A0/A1 combination. These two pins are normally connected to the two lower order bits of the address bus. |
| CLK0~2 | Clock input | Input | Supply of three clock signals to the three counters incorporated in MSM82C53. |
| GATE0~2 | Gate input | Input | Control of starting, interruption, and restarting of counting in the three respective counters in accordance with the set control word contents. |
| OUT0~2 | Counter output | Output | Output of counter output waveform in accordance with the set mode and count value. |

## SYSTEM INTERFACING




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## DESCRIPTION OF BASIC OPERATIONS

Data transfers between the internal registers and the external data bus is outlined in the following table.

| $\overline{CS}$ | $\overline{RD}$ | $\overline{WR}$ | A1 | A0 | Function |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | Data bus to counter # 0 Writing |
| 0 | 1 | 0 | 0 | 1 | Data bus to counter # 1 Writing |
| 0 | 1 | 0 | 1 | 0 | Data bus to counter # 2 Writing |
| 0 | 1 | 0 | 1 | 1 | Data bus to control word register Writing |
| 0 | 0 | 1 | 0 | 0 | Data bus from counter # 0 Reading |
| 0 | 0 | 1 | 0 | 1 | Data bus from counter # 1 Reading |
| 0 | 0 | 1 | 1 | 0 | Data bus from counter # 2 Reading |
| 0 | 0 | 1 | 1 | 1 | Data bus in high impedance status |
| 1 | x | x | x | x | |
| 0 | 1 | 1 | x | x | |

x denotes "not specified.".

## DESCRIPTION OF OPERATION

82C53 functions are selected by a control word from the CPU. In the required program sequence, the control word setting is followed by the count value setting and execution of the desired timer operation.

**Control Word and Count Value Program**

Each counter operation mode is set by control word programming. The control word format is outlined below.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| SC1 | SC0 | RL1 | RL0 | M2 | M1 | M0 | BCD |
| Select Counter | | Read/Load | | Mode | | | BCD |

($\overline{CS}$ = 0, A0, A1 = 1,1, $\overline{RD}$ = 1, $\overline{WR}$ = 0)

- **Select Counter (SC0, SC1):** Selection of set counter

| SC1 | SC0 | Set Contents |
|---|---|---|
| 0 | 0 | Counter # 0 selection |
| 0 | 1 | Counter # 1 selection |
| 1 | 0 | Counter # 2 selection |
| 1 | 1 | Illegal combination |

- **Read/Load (RL1, RL0):** Count value Reading/Loading format setting

| RL1 | RL0 | Set Contents |
|---|---|---|
| 0 | 0 | Counter Latch operation |
| 0 | 1 | Reading/Loading of Least Significant byte (LSB) |
| 1 | 0 | Reading/Loading of Most Significant byte (MSB) |
| 1 | 1 | Reading/Loading of LSB followed by MSB |

- **Mode (M2, M1, M0):** Operation waveform mode setting

| M2 | M1 | M0 | Set Contents |
|---|---|---|---|
| 0 | 0 | 0 | Mode 0 (Interrupt on Terminal Count) |
| 0 | 0 | 1 | Mode 1 (Programmable One-Shot) |
| x | 1 | 0 | Mode 2 (Rate Generator) |
| x | 1 | 1 | Mode 3 (Square Wave Generator) |
| 1 | 0 | 0 | Mode 4 (Software Triggered Strobe) |
| 1 | 0 | 1 | Mode 5 (Hardware Triggered Strobe) |

x denotes "not specified".

- **BCD:** Operation count mode setting

| BCD | Set Contents |
|---|---|
| 0 | Binary Count (16-bits Binary) |
| 1 | BCD Count (4-decades Binary Coded Decimal) |

After setting Read/Load, Mode, and BCD in each counter as outlined above, next set the desired count value. (In some Modes, counting is started immediately after the count value has been written). This count value setting must conform with the Read/Load format set in advance. Note that the internal counters are reset to OOOOH during control word setting. The counter value (OOOOH) can.t be read.

If the two bytes (LSB and MSB) are written at this stage (RL0 and RL1 = 1,1), take note of the following precaution.

Although the count values may be set in the three counters in any sequence after the control word has been set in each counter, count values must be set consecutively in the LSB – MSB order in any one counter.

■ I/O-MSM82C53-2RS/GS/JS ■

- **Example of control word and count value setting**

  Counter #0: Read/Load LSB only, Mode 3, Binary count, count value 3H
  Counter #1: Read/Load MSB only, Mode 5, Binary count, count value AA00H
  Counter #2: Read/Load LSB and MSB, Mode 0, BCD count, count value 1234

```
MVI A, 1EH
OUT n3      ] Counter #0 control word setting
MVI A, 6AH
OUT n3      ] Counter #1 control word setting
MVI A, B1H
OUT n3      ] Counter #2 control word setting
MVI A, 03H
OUT n0      ] Counter #0 count value setting
MVI A, AAH
OUT n1      ] Counter #1 count value setting
MVI A, 34H
OUT n2
MVI A, 12H  ] Counter #2 count value setting (LSB then MSB)
OUT n2
```

**Notes:** n0: Counter #0 address
n1: Counter #1 address
n2: Counter #2 address
n3: Control word register address

- **The minimum and maximum count values which can be counted in each mode are listed below.**

| Mode | Min. | Max. | Remarks |
|---|---|---|---|
| 0 | 1 | 0 | 0 executes 10000H count (ditto in other modes) |
| 1 | 1 | 0 | |
| 2 | 2 | 0 | 1 cannot be counted |
| 3 | 2 | 1 | 1 executes 10001H count |
| 4 | 1 | 0 | |
| 5 | 1 | 0 | |

**Mode Definition**

- **Mode 0 (terminal count)**
  The counter output is set to "L" level by the mode setting. If the count value is then written in the counter with the gate input at "H" level (that is, upon completion of writing the MSB when there are two bytes), the clock input counting is started. When the terminal count is reached, the output is switched to "H" level and is maintained in this status until the control word and count value are set again.
  Counting is interrupted if the gate input is switched to "L" level, and restarted when switched back to "H" level.
  When Count Values are written during counting, the operation is as follows:
  1-byte Read/Load.... When the new count value is written, counting is stopped immediately, and then restarted at the new count value by the next clock.
  2-byte Read/Load.... When byte 1 (LSB) of the new count value is written, counting is stopped immediately. Counting is restarted at the new count value when byte 2 (MSB) is written.

- **Mode 1 (programmable one-shot)**
  The counter output is switched to "H" level by the mode setting. Note that in this mode, counting is not started if only the count value is written. Since counting has to be started in this mode by using the leading edge of the gate input as a trigger, the counter output is switched to "L" level by the next clock after the gate input trigger. This "L" level status is maintained during the set count value, and is switched back to "H" level when the terminal count is reached.
  Once counting has been started, there is no interruption until the terminal count is reached, even if the gate input is switched to "L" level in the meantime. And although counting continues even if a new count value is written during the counting, counting is started at the new count value if another trigger is applied by the gate input.

- **Mode 2 (rate generator)**
  The counter output is switched to "H" level by the mode setting. When the gate input is at "H" level, counting is started by the next clock after the count value has been written. And if the gate input is at "L" level, counting is started by using the rising edge of the gate input as a trigger after the count value has been set.
  An "L" level output pulse appears at the counter output during a single clock duration once every n clock inputs where n is the set count value. If a new count value is written during while counting is in progress, counting is started at the new count value following output of the pulse currently being counted. And if the gate input is switched to "L" level during counting, the counter output is forced to switch to "H" level, the counting being restarted by the rising edge of the gate input.

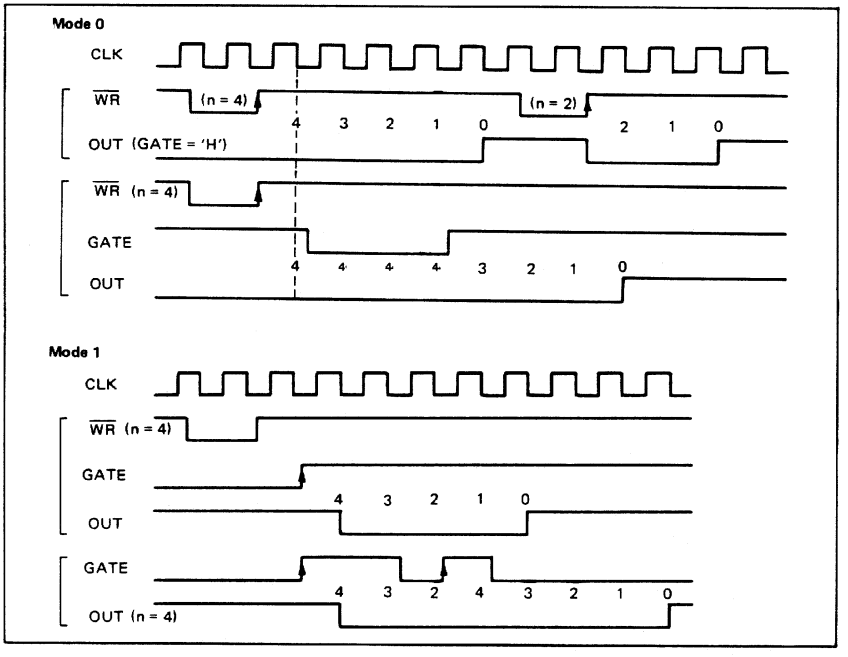
- **Mode 3 (square waveform rate generator)**
  The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 2 above.
  The repeated square wave output appearing at the counter output contains half the number of counts as the set count value. If the set count value (n) is an odd number, the repeated square wave output consists of only (n + 1)/2 clock inputs at "H" level and (n – 1)/2 clock inputs at "L" level.
  If a new count value is written during counting, the new count value is reflected immediately after the

change ("H" to "L" or "L" to "H") in the next counter output to be executed. The counting operation at the gate input is done the same as in mode 2.

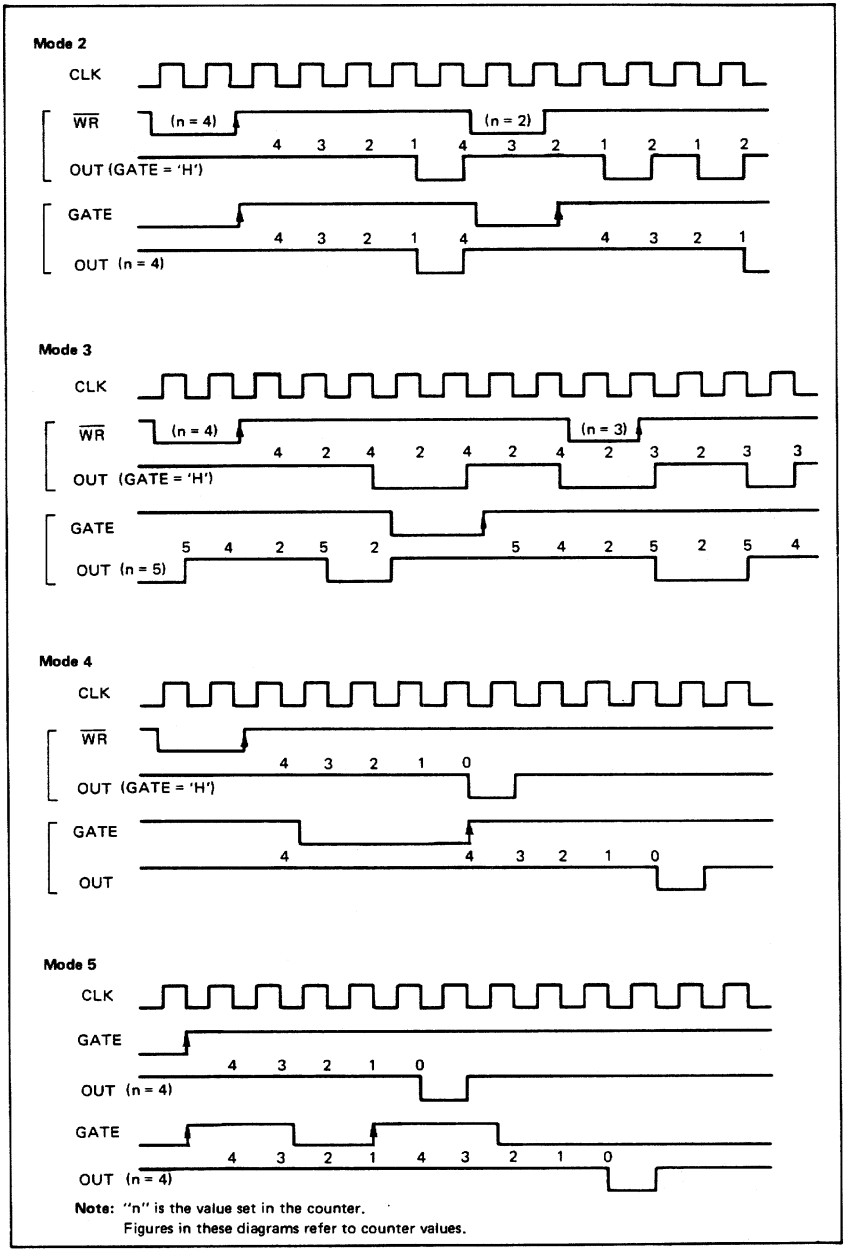
- **Mode 4 (software trigger strobe)**
  The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 0. A single "L" pulse equivalent to one clock width is generated at the counter output when the terminal count is reached.
  This mode differs from 2 in that the "L" level output appears one clock earlier in mode 2, and that pulses are not repeated in mode 4. Counting is stopped when the gate input is switched to "L" level, and restarted from the set count value when switched back to "H" level.

- **Mode 5 (hardware trigger strobe)**
  The counter output is switched to "H" level by the mode setting. Counting is started, and the gate input used, in the same way as in mode 1.
  The counter output is identical to the mode 4 output.
  The various roles of the gate input signals in the above modes are summarized in the following table.

| Mode \ Gate | "L" Level Falling Edge | Rising Edge | "H" Level |
|---|---|---|---|
| 0 | Counting not possible | | Counting possible |
| 1 | | (1) Start of counting<br>(2) Retriggering | |
| 2 | (1) Counting not possible<br>(2) Counter output forced to "H" level | Start of counting | Counting possible |
| 3 | (1) Counting not possible<br>(2) Counter output forced to "H" level | Start of counting | Counting possible |
| 4 | Counting not possible | | Counting possible |
| 5 | | (1) Start of counting<br>(2) Retriggering | |



■ I/O-MSM82C53-2RS/GS/JS ■




**Note:** "n" is the value set in the counter.
Figures in these diagrams refer to counter values.

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**Reading of Counter Values**

All 82C53 counting is down-counting, the counting being in steps of 2 in mode 3. Counter values can be read during counting by (1) direct reading, and (2) counter latching ("read on the fly").

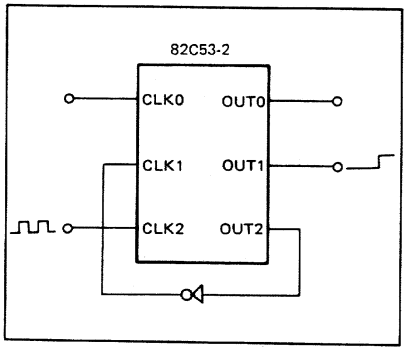
- **Direct reading**
  Counter values can be read by direct reading operations.
  Since the counter value read according to the timing of the $\overline{RD}$ and CLK signals is not guaranteed, it is necessary to stop the counting by a gate input signal, or to interrupt the clock input temporarily by an external circuit to ensure that the counter value is correctly read.

- **Counter latching**
  In this method, the counter value is latched by writing a counter latch command, thereby enabling a stable value to be read without effecting the counting in any way at all. An example of a counter latching program is given below.
  Counter latching executed for counter #1 (Read/Load 2-byte setting)

```
MVI A  01 00 x x x x
          └── Denotes counter latching
OUT n3 ──┬── Write in control word address (n3)
         └── The counter value at this point is latched
IN n1  ──┬── Reading of the LSB of the counter value latched from counter #1.
         └── n1: Counter #1 address
MOV B, A
IN n1  ──── Reading of MSB from counter #1.
MOV C, A
```

**Example of Practical Application**

- **82C53 used as a 32-bit counter.**




Use counter #1 and counter #2

Counter #1: mode 0, upper order 16-bit counter value

Counter #2: mode 2, lower order 16-bit counter value

This setting enables counting up to a maximum of $2^{32}$

# Using Your PC-LPM-16 (Non-PnP) Board

Appendix C

This appendix describes the differences between the PC-LPM-16PnP and the PC-LPM-16 non-PnP boards, the PC-LPM-16 board configuration, and installing the PC-LPM-16 into your computer.

## Differences between the PC-LPM-16PnP and the PC-LPM-16

The PC-LPM-16PnP is a Plug and Play upgrade from a legacy board, the PC-LPM-16. A National Instruments *legacy* product refers to an older board with switches and jumpers used to set the addresses. The original board has been replaced with a backwards-compatible, revised PC-LPM-16. This revised board has the same functionality as the Plug and Play version (except for the base address and interrupt selection), but differs somewhat from the legacy board. The following list compares the specifications and functionality of the newer boards with the obsolete board.

**Table C-1.** Comparison of Characteristics

| Functional Changes | Legacy PC-LPM-16 | Revised PC-LPM-16 | PC-LPM-16PnP |
|---|---|---|---|
| Assembly Number | 181215-01 | 183527*X*-02 | 183527*X*-01 |
| I/O Space Required | 32 bytes | 16 bytes | 16 bytes |
| I/O Base Address Selection | Uses switches | Uses switches | Plug and Play compatible |
| I/O Base Address Alignment | Located on 32-byte boundary | Located on 32-byte boundary | Located on 16-byte boundary |
| IRQ Selection | Uses jumpers | Uses jumpers | Plug and Play compatible |
| Gain Selection | Selectable with jumpers | Selectable with jumpers | Software selectable |

**Table C-1.** Comparison of Characteristics (Continued)

| Functional Changes | Legacy PC-LPM-16 | Revised PC-LPM-16 | PC-LPM-16PnP |
|---|---|---|---|
| Data FIFO Size | 16 words | 512 words | 256 words |
| Dummy reads to A/D and FIFO high-byte and low-byte registers after clearing data FIFO | Required | Not required, but allowed | Not required, but allowed |
| ADC FIFO Data Reading Order | Low byte before high byte preferred | Low byte must be read before high byte | Low byte must be read before high byte |
| Overflow Error Bit Location | Status Register 1, bit 1 | Status Register 1, bit 1 | Status Register 2, bit 1 |
| Overrun Error Bit Location | Not implemented | Not implemented | Status Register 2, bit 0 |
| Data Error Bit Location | Not implemented | Not implemented | Status Register 1, bit 1 |
| 5 and 12 V Supply Fuses | Nonresettable | Self-resetting | Self-resetting |
| -12 V Supply Power Requirements | 0 mA | 15 mA typ | 15 mA typ |
| **Performance Specification Changes** | | | |
| INL | ±1 LSB max | ±0.5 LSB max | ±0.5 LSB max |
| Gain Error, ±2.8 V or to 10 V Range | ±3 LSB typ, ±7 LSB max | ±2 LSB typ, ±4 LSB max | ±2 LSB typ, ±4 LSB max |
| Calibration Time | 700 µs typ | 10 ms typ | 10 ms typ |
| Overvoltage Protection or Analog Input Powered Off | ±45 V | ±35 V | ±35 V |

**Table C-1.** Comparison of Characteristics (Continued)

| Functional Changes | Legacy PC-LPM-16 | Revised PC-LPM-16 | PC-LPM-16PnP |
|---|---|---|---|
| Interrupt Enable/ Disable Control | Through Command Register 1 | Through Command Register 1 | Through Plug and Play BIOS or NI-DAQ Configuration Utility |
| Delay Between Rising EXTCONV* Edge and A/D Conversion | 2–4 µs | 800 ns max | 800 ns max |

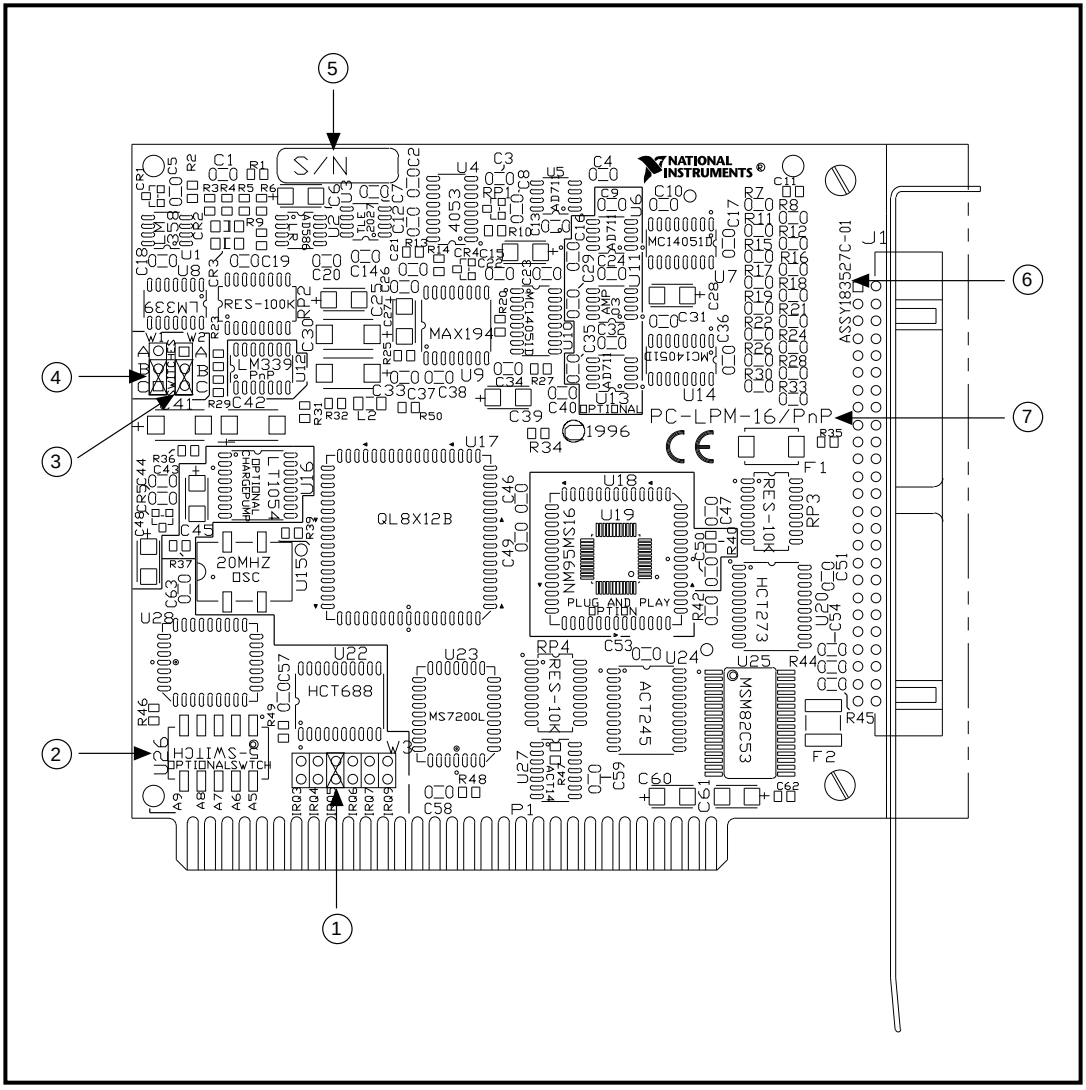
To determine which PC-LPM-16 board you have, refer to the *Assembly Number* row in Table C-1 and compare it to the assembly number displayed on your circuit board (see Figure C-1).

# Configuration and Installation of the PC-LPM-16 (non-PnP)

## Board Configuration

The PC-LPM-16 contains three jumpers and one DIP switch to configure the PC bus interface and analog input settings. Use the DIP switch to set the base I/O address. Jumper W3 selects the interrupt level. Jumpers W1 and W2 configure the analog input circuitry. The DIP switch and jumpers are shown in the parts locator diagram in Figure C-1.

The PC-LPM-16 is factory-configured to a base I/O address of hex 260 and to interrupt level 5. These settings (shown in Table C-1) are suitable for most systems. However, if your system has other hardware at this base I/O address or interrupt level, you need to change these settings on the PC-LPM-16 (as described in the following pages) or on the other hardware. Record your settings in the *Hardware and Software Configuration Form* in Appendix E, *Customer Communication*.



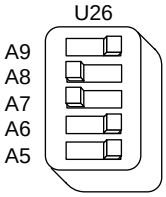

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | W3 | 3 | W2 | 5 | Serial Number | 7 | Product Name |
| 2 | Switch U26 | 4 | W1 | 6 | Assembly Number | | |

**Figure C-1.** PC-LPM-16 Parts Locator Diagram

## Base I/O Address Selection

The base I/O address for the PC-LPM-16 is determined by the switches at position U26 (see Figure C-2). The switches are set at the factory for the base I/O address hex 260. This factory setting is used as the default base I/O address value by National Instruments software packages for use with the PC-LPM-16. The PC-LPM-16 uses the base I/O address space hex 260 through 26F with the factory setting. See Table C-2 for the board factory settings.

**Table C-2.** PC Bus Interface Factory Settings

| PC-LPM-16 Board | Default Settings | Hardware Implementation |
|---|---|---|
| Base I/O Address | Hex 260 |  |
| Interrupt Level | Interrupt level 5 selected (factory setting) | **W3:** Row 5 |
| Analog Input | Bipolar input selected (±5 V) (factory setting) | **W1:** B-C<br>**W2:** B-C |

Verify that this base I/O address space is not already used by other equipment installed in your computer.

☞ **Note:** ***If any equipment in your computer already uses this base I/O address space, you must change the base I/O address of the PC-LPM-16 or of the other device.***

If you change the PC-LPM-16 base I/O address, you must make a corresponding change to any software packages you use with the PC-LPM-16. For more information about the I/O address of your computer, refer to your computer's technical reference manual.

Each switch in U26 corresponds to one of the address lines A9 through A5. Slide the switch to the side labeled *A9* to *A5* to select a binary value of *zero* for the corresponding address bit. Slide the switch to the side of the switch labeled *ON* to select a binary value of *one* for the corresponding address bit. Figure C-2 shows two possible switch settings.

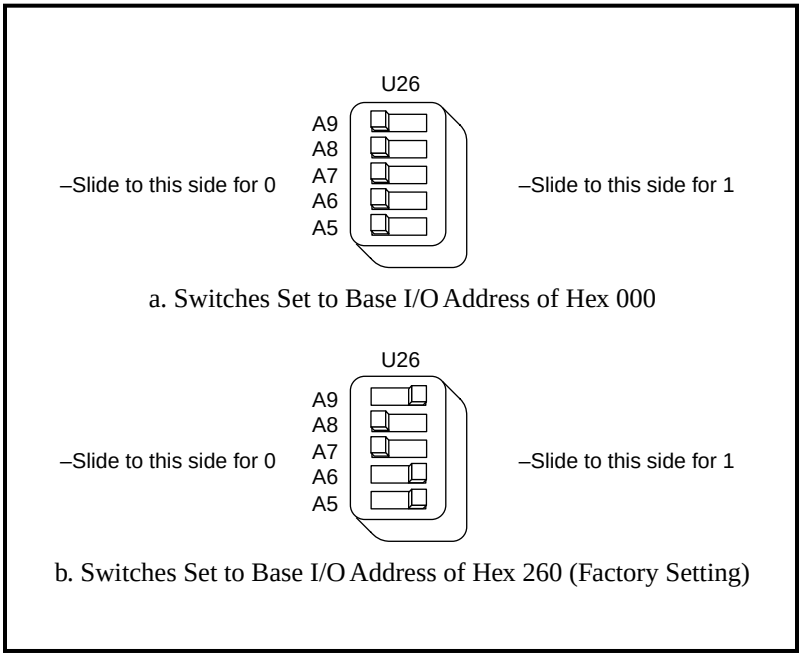



**Figure C-2.** Example Base I/O Address Switch Settings

The PC-LPM-16 decodes the five LSBs of the address (A4 through A0) to select the appropriate PC-LPM-16 register. To change the base I/O address:

1. Remove the plastic cover on U26.
2. Slide each switch to the desired position.
3. Check each switch to verify that the switch is pressed entirely to the side.
4. Replace the plastic cover.

Note the new PC-LPM-16 base I/O address for use when configuring the PC-LPM-16 software in the *Hardware and Software Configuration Form* in Appendix E, *Customer Communication*. Table C-3 lists the

possible switch settings, the corresponding base I/O address, and the base I/O address space used for that setting.

**Table C-3.** Switch Settings with Corresponding Base I/O Address and Base I/O Address Space

| Switch Setting | | | | | Base I/O Address (hex) | Base I/O Address Space Used (hex) |
|---|---|---|---|---|---|---|
| A9 | A8 | A7 | A6 | A5 | | |
| 0 | 1 | 0 | 0 | 0 | 100 | 100–10F |
| 0 | 1 | 0 | 0 | 1 | 120 | 120–13F |
| 0 | 1 | 0 | 1 | 0 | 140 | 140–14F |
| 0 | 1 | 0 | 1 | 1 | 160 | 160–16F |
| 0 | 1 | 1 | 0 | 0 | 180 | 180–18F |
| 0 | 1 | 1 | 0 | 1 | 1A0 | 1A0–1AF |
| 0 | 1 | 1 | 1 | 0 | 1C0 | 1C0–1CF |
| 0 | 1 | 1 | 1 | 1 | 1E0 | 1E0–1EF |
| 1 | 0 | 0 | 0 | 0 | 200 | 200–20F |
| 1 | 0 | 0 | 0 | 1 | 220 | 220–22F |
| 1 | 0 | 0 | 1 | 0 | 240 | 240–24F |
| 1 | 0 | 0 | 1 | 1 | 260 | 260–26F |
| 1 | 0 | 1 | 0 | 0 | 280 | 280–28F |
| 1 | 0 | 1 | 0 | 1 | 2A0 | 2A0–2AF |
| 1 | 0 | 1 | 1 | 0 | 2C0 | 2C0–2CF |
| 1 | 0 | 1 | 1 | 1 | 2E0 | 2E0–2EF |
| 1 | 1 | 0 | 0 | 0 | 300 | 300–30F |
| 1 | 1 | 0 | 0 | 1 | 320 | 320–32F |

**Table C-3.** Switch Settings with Corresponding Base I/O Address and Base I/O Address Space (Continued)

| Switch Setting | | | | | Base I/O Address (hex) | Base I/O Address Space Used (hex) |
|---|---|---|---|---|---|---|
| A9 | A8 | A7 | A6 | A5 | | |
| 1 | 1 | 0 | 1 | 0 | 340 | 340–34F |
| 1 | 1 | 0 | 1 | 1 | 360 | 360–36F |
| 1 | 1 | 1 | 0 | 0 | 380 | 380–38F |
| 1 | 1 | 1 | 0 | 1 | 3A0 | 3A0–3AF |
| 1 | 1 | 1 | 1 | 0 | 3C0 | 3C0–3CF |
| 1 | 1 | 1 | 1 | 1 | 3E0 | 3E0–3EF |

☞ **Note:** ***Base I/O address values hex 000 through 0FF are reserved for system use. Base I/O address values hex 100 through 3FF are available on the I/O channel.***

## Interrupt Selection

The PC-LPM-16 connects to any one of the six interrupt lines of the computer I/O channel. A jumper selects the interrupt line on one of the double rows of pins located above the I/O slot edge connector on the PC-LPM-16 (see Figure C-1). To use the PC-LPM-16 interrupt capability, select an interrupt line and place the jumper in the appropriate position to enable that particular interrupt line.

The interrupt lines that the PC-LPM-16 hardware supports are IRQ<3..7>, and IRQ9.

☞ **Note:** ***Using interrupt line 6 is not recommended. The diskette drive controller uses interrupt line 6 on most IBM PC and compatible computers.***

After you select an interrupt level, place the interrupt jumper on the appropriate pins to enable the interrupt line.

The interrupt jumper setting is *W3*. The default interrupt line is IRQ5, which you select by placing the jumper on the pins in row 5, as shown in Figure C-3. To change to another line, remove the jumper from IRQ5 and place it on the new pins.

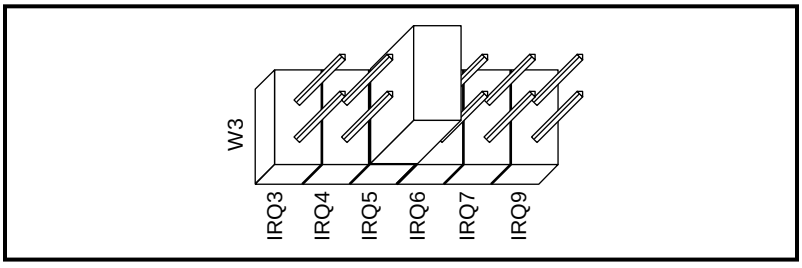



**Figure C-3.** Interrupt Jumper Setting IRQ5 (Factory Setting)

If you do not want to use interrupts, set the jumper on W3 as shown in Figure C-4. This setting disables the PC-LPM-16 from asserting an interrupt line on the computer I/O channel.

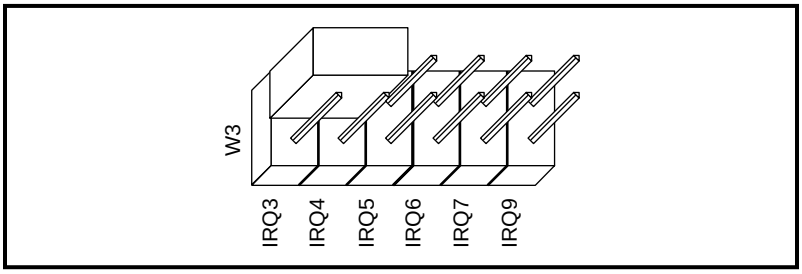



**Figure C-4.** Interrupt Jumper Setting for Disabling Interrupts

## Analog Input Jumper Settings

The PC-LPM-16 is factory-configured for the ±5 V input range.

Four ranges are available for analog input: bipolar ±5 V, bipolar ±2.5 V, unipolar 0 to 10 V, and unipolar 0 to 5 V. Jumpers W1 and W2 control the input range for all 16 analog input channels.

## Bipolar Input Selection 1 (±5 V)

Select the bipolar (±5 V) input configuration by setting jumpers W1 and W2 as shown in Figure C-5.

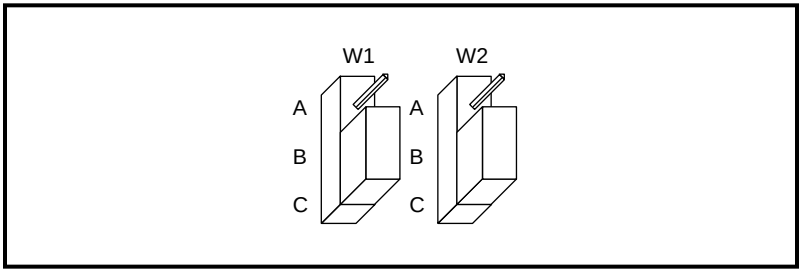



**Figure C-5.** Bipolar Input (±5 V) Jumper Configuration (Factory Setting)

## Bipolar Input Selection 2 (±2.5 V)

Select the bipolar (±2.5 V) input configuration by setting jumpers W1 and W2 as shown in Figure C-6.

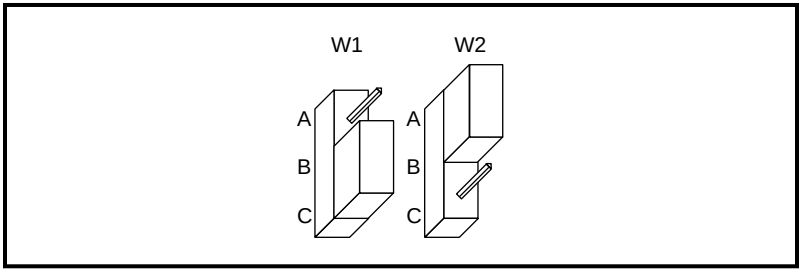



**Figure C-6.** Bipolar Input (±2.5 V) Jumper Configuration

## Unipolar Input Selection 1 (0 to 10 V)

Select the unipolar (0 to 10 V) input configuration by setting jumpers W1 and W2 as shown in Figure C-7.

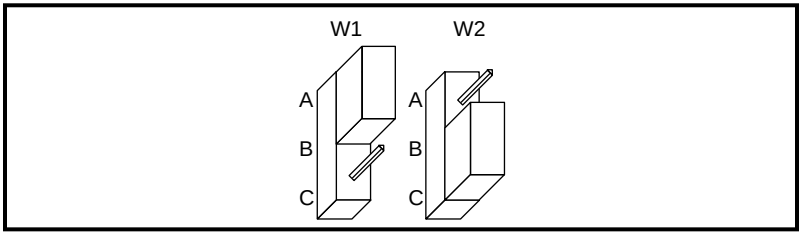



**Figure C-7.** Unipolar Input (0 to 10 V) Jumper Configuration

### Unipolar Input Selection 2 (0 to 5 V)

Select the unipolar (0 to 5 V) input configuration by using the same setting as the ±5 V range setting shown in Figure C-5. You can use this setting because the ADC is 12-bit. Therefore, 12-bit resolution data is obtained in both the 0 to +5 V signal range and the 0 to -5 V signal range while keeping the input configuration for ±5 V input range. The jumper configuration for the 0 to 5 V and ±5 V input signal ranges is the same. The software handles the distinction between the two ranges.

## Installation

You can install the PC-LPM-16 in any available 8-bit or 16-bit expansion slot in your computer. To optimize the board noise performance, install the board away from the video card and leave a slot vacant on each side of the PC-LPM-16, if possible. After you make any necessary changes with the jumper and switch settings, you are ready to install the PC-LPM-16.

The following are general installation instructions, but consult your computer user manual or technical reference manual for specific instructions and warnings.

1. Turn off and unplug your computer.
2. Remove the top cover or access port to the I/O channel.
3. Remove the expansion slot cover on the back panel of the computer.
4. Insert the PC-LPM-16 board into any 8-bit or 16-bit slot. It may be a tight fit, but *do not force* the board into place.
5. Screw the mounting bracket of the PC-LPM-16 board to the back panel rail of the computer.
6. Replace the cover.
7. Plug in and turn on your computer.

The PC-LPM-16 is installed.

# Register-Level Programming

Appendix D

This appendix describes in detail information related to register-level programming the PC-LPM-16/PnP.

☞ **Note:** ***If you plan to use a programming software package such as NI-DAQ, LabVIEW, or LabWindows/CVI with your PC-LPM-16/PnP, you need not read this appendix.***

## Base Address

For information on the base address, see Chapter 2, *Installation and Configuration.*

## Register Map

The register map for the PC-LPM-16/PnP is given in Table D-1. This table gives the register name, the register address offset from the board's base address, the type of the register (read only, write only, or read and write), and the size of the register in bits.

**Table D-1.** PC-LPM-16/PnP Register Map

| Register Name | Offset Address (Hex) | Type | Size |
|---|---|---|---|
| Configuration and Status Register Group | | | |
| Command Register 1 | 0 | Write-only | 8-bit |
| Command Register 2 | 7 | Read-and-write | 8-bit |
| Command Register 3 | 5 | Write-only | 8-bit |
| Status Register 1 | 0 | Read-only | 8-bit |
| Status Register 2* | 1 | Read-only | 8-bit |
| Analog Input Register Group | | | |
| A/D FIFO Low-Byte Register | 2 | Read-only | 8-bit |
| A/D FIFO High-Byte Register | 3 | Read-only | 8-bit |
| A/D Clear Register | 1 | Write-only | 8-bit |

**Table D-1.** PC-LPM-16/PnP Register Map (Continued)

| Register Name | Offset Address (Hex) | Type | Size |
|---|---|---|---|
| Counter/Timer (MSM82C53) Register Group | | | |
| Counter 0 Data Register | 8 | Read-and-write | 8-bit |
| Counter 1 Data Register | 9 | Read-and-write | 8-bit |
| Counter 2 Data Register | A | Read-and-write | 8-bit |
| Counter Mode Register | B | Write-only | 8-bit |
| Timer Interrupt Clear Register | 6 | Write-only | 8-bit |
| Digital I/O Register Group | | | |
| Digital Output Register | 4 | Write-only | 8-bit |
| Digital Input Register | 5 | Read-only | 8-bit |

*PC-LPM-16PnP only.

# Register Size

The PC-LPM-16/PnP registers are 8-bit registers. To transfer 16-bit data, you need two consecutive I/O read or write operations. For example, to read the 16-bit A/D conversion result, read the low byte of FIFO first, then the high byte of FIFO.

# Register Descriptions

Table D-1 divides the PC-LPM-16/PnP registers into four different register groups. A bit description of each of the registers making up these groups is included later in this appendix.

The Configuration and Status Register Group controls the overall operation of the PC-LPM-16/PnP and the D/A circuitry. The Analog Input Register Group reads output from the successive-approximation ADC. The Counter/Timer Register Group accesses the onboard MSM82C53 counter/timer integrated circuit. The Digital I/O Register Group consists of the digital output and input registers.

## Register Description Format

The remainder of this appendix discusses each of the PC-LPM-16/PnP registers in the order shown in Table D-1. Each register group is introduced, followed by an individual register description. The individual register description includes the address, type, word size, and bit map of the register.

The register bit map shows a diagram of the register with the MSB (bit 7 for an 8-bit register) shown on the left, and the LSB (bit 0) shown on the right. Each bit is represented by a square with the bit name inside. An asterisk (*) after the bit name indicates that the bit is inverted (negative logic).

In many of the registers, several bits are labeled with an *X*, indicating *don't care* bits. When reading a register, these bits may appear set or cleared, but should be ignored because they have no significance. When writing to a register, setting or clearing these bit locations has no effect on the PC-LPM-16PnP hardware. Take special note of the bits labeled *reserved for future use*. The board may not function if you don't write the designated value to these register bits.

The bit map field for some write-only registers states *not applicable, no bits used*. Writing to these registers causes an event to occur on the PC-LPM-16PnP, such as clearing the analog input circuitry. The data is ignored when writing to these registers; therefore, any bit pattern will suffice.

For a detailed bit description of each register concerning the MSM82C53 chip on the PC-LPM-16/PnP, refer to Appendix B, *MSM82C53 Data Sheet*.

## Configuration and Status Register Group

The three registers making up the Configuration and Status Register Group allow general control and monitoring of the PC-LPM-16/PnP A/D circuitry. Command Register 1 and Command Register 2 contain bits that control the operation modes of the A/D circuitry and enable or disable the interrupt operations. Command Register 3 sets the board input range. The Status Register reports the A/D conversion status, A/D conversion error, and the interrupt status.

Bit descriptions for the registers in the Configuration and Status Register Group are given on the following pages.

## Command Register 1

Command Register 1 indicates the input channel to be read and the interrupt enable bits.

**Address:** Base address + 00 (hex)

**Type:** Write-only

**Word Size:** 8-bit

**Bit Map:**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCANEN* | CNTINTEN | EXTINTEN | FIFOINTEN | MA3 | MA2 | MA1 | MA0 |

| Bit | Name | Description |
|---|---|---|
| 7 | SCANEN* | Scan Enable Bit—This bit enables or disables multichannel scanning during data acquisition. The power-on value is 1. If this bit is cleared, analog channels MA<3..0> through 0 are sampled alternately. If this bit is set, a single analog channel selected by MA<3..0> is sampled during the entire data acquisition operation. In order to perform single-channel sampling, the UP/DOWN bit in Command Register 2 must be clear before setting SCANEN* to 1. To set up a scanning mode, two consecutive writings of this register are necessary. First, write the desired valve to the UP/DOWN bit in Command Register 2 if the UP/DOWN bit is not currently set to its proper value. Then write MA<3..0> with SCANEN* set to load the scan counter. Then write MA<3..0> with SCANEN* cleared to enable scanning.<br><br>For example, if the UP/DOWN bit is 0 and MA<3..0> is 0011 and SCANEN* is first set, then cleared, analog input channels 3 through 0 are sampled alternately during subsequent data conversions. If SCANEN* is set and is not cleared (with MA<3..0> still set to 0011), only analog input channel 3 is sampled during the subsequent data conversions.<br><br>See the *Programming Multiple A/D Conversions with Channel Scanning* section later in this appendix for more information. |

## Command Register 1

**(Continued)**

| | | |
|---|---|---|
| 6 | CNTINTEN | Counter Interrupt Enable Bit—With this bit, the counter 2 output can cause interrupts. The power-on value is 0. If this bit is set, an interrupt occurs when counter 2 output makes a low-to-high transition. Clear this interrupt by writing to the Timer Interrupt Clear Register. If this bit is cleared, interrupts from counter 2 output are ignored. |
| 5 | EXTINTEN | External Interrupt Enable Bit—This bit enables and disables the generation of an interrupt when the EXTINT* signal on the I/O connector is asserted low externally. The power-on value is 0. When this bit is set, the external interrupt is enabled. The external device that asserts this signal is responsible for keeping EXTINT* low until the interrupt is acknowledged, and is then responsible for releasing it. EXTINT* is pulled up to +5 V on the board. |
| 4 | FIFOINTEN | First In First Out Interrupt Enable Bit—This bit enables and disables the interrupt generation when A/D conversion results are available. The power-on value is 0. If FIFOINTEN is set, an interrupt is generated whenever an A/D conversion can be read from the FIFO. |
| 3–0 | MA<3..0> | Channel Select Bits 3 through 0—These four bits select which of the 16 input channels are read. The power-on value is 0000. The analog input multiplexer depends on these four bits to select the input channel. The input channel is selected as follows: |

| MA<3..0> | Selected Channel |
|---|---|
| 0000 | 0 |
| 0001 | 1 |
| 0010 | 2 |
| 0011 | 3 |

# Command Register 1

**(Continued)**

| MA<3..0> | Selected Channel |
|---|---|
| 0100 | 4 |
| 0101 | 5 |
| 0110 | 6 |
| 0111 | 7 |
| 1000 | 8 |
| 1001 | 9 |
| 1010 | 10 |
| 1011 | 11 |
| 1100 | 12 |
| 1101 | 13 |
| 1110 | 14 |
| 1111 | 15 |

If SCANEN* is cleared, analog channels MA<3..0> through channel 0 are sampled. Sampling order, whether from channel 0 to MA<3..0> or from MA<3..0> to channel 0, is determined by the SCANORDER bit in Command Register 2. If SCANEN* is set, a single analog channel specified by MA<3..0> is sampled during the entire data acquisition operation. See the *Programming Multiple A/D Conversions with Channel Scanning* section later in this appendix for the correct sequence involved in setting the SCANEN* bit.

## Command Register 2

Command Register 2 contains only one bit that enables the auto-calibration operation of the ADC.

**Address:** Base address + 07 (hex)

**Type:** Read-and-write

**Word Size:** 8-bit

**Bit Map:**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | SCANORDER | DISABDAQ | CALEN |

| Bit | Name | Description |
|---|---|---|
| 7–3 | 0 | Reserved bits—These bits must be set to zero for future board compatibility. |
| 2 | SCANORDER | Scan Order Bit—If this bit is cleared, the scan order is from the channel in Command Register 1 MA<3..0> to channel 0. The power-on value is 0. If this bit is set, the scan order begins with channel 0 and ends with the channel number in MA<3..0>. This bit is cleared upon power up. To ensure proper scanning, this bit should be correctly programmed before writing to the SCANEN* and Channel Selection bits in Command Register 1. This bit is only present on the PC-LPM-16PnP. |

☞ **Note:** ***The UP function is not yet supported by NI-DAQ. NI-DAQ will support the UP function in a future release.***

| | | |
|---|---|---|
| 1 | DISABDAQ | Disable Data Acquisition Bit—This bit is used to disable the data acquisition operation. The power-on value is 0. Upon startup, this bit is cleared and, as a result, the data acquisition operation is enabled. Writing a one to this bit disables both A/D conversion source signals OUT0* and EXTCONV*. |

## Command Register 2

**(Continued)**

| Bit | Name | Description |
|---|---|---|
| 0 | CALEN | Calibration Enable Bit—If this bit is set, the auto-calibration of the 12 bit ADC is enabled. The power-on value is 0. To start the auto-calibration, first write one to this bit, then read this register. The result of the reading is ignored. An auto-calibration lasts about 10 ms. By checking the CONVPROG bit of the Status Register, the completion of auto-calibration can be detected. After the auto-calibration, you must clear this bit for the A/D conversion operation. |

## Command Register 3

Command Register 3 contains other range setting configuration bits.

**Address:** 05 (hex)

**Type:** Write-only

**Word Size:** 8-bit

**Bit Map:**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | ARNG<1> | ARNG<0> |

| Bit | Name | Description |
|---|---|---|
| 7–2 | 0 | Reserved Bits—These bits must be set to zero. |
| 1–0 | ARNG<1..0> | Analog Input Voltage Range—These bits control the analog input voltage range setting as follows: |

| ARNG<1..0> | Input Voltage Range |
|---|---|
| 00 | 0 to 10 V |
| 10 | ±5 V, 0 to 5 V |
| 11 | ±2.5 V |

The power-on value for ARNG<1..0> is 10.

## Status Register 1

Status Register 1 indicates the status of the current A/D conversion. The bits in this register determine if a conversion is being performed, if data is available, if any errors have been found, and the interrupt status.

**Address:** Base address + 00 (hex)

**Type:** Read-only

**Word Size:** 8-bit

**Bit Map:**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| REVID | X | X | CONVPROG | EXTINT* | CNTINT | DATAERR/ OVERFLOW | DAVAIL |

| Bit | Name | Description |
|---|---|---|
| 7 | REVID | Revision ID Bit—This bit identifies the board revision. If this bit is cleared, the board is a revision A legacy PC-LPM-16 board. If this bit is set, the board is a revision B or later PC-LPM-16 board. The revision B board has one more bit in Command Register 2 to disable the data acquisition operation. This bit is always set for the PC-LPM-16PnP board. |
| 6–5 | X | Don't care bits. |
| 4 | CONVPROG | Conversion Progress Status Bit—When an A/D conversion is in progress or the auto-calibration operation of the ADC is in progress, this bit is set. Otherwise, it is cleared. |

## Status Register 1

**(Continued)**

| Bit | Name | Description |
|---|---|---|
| 3 | EXTINT* | External Interrupt Status Bit—This bit reflects the status of the EXTINT* signal on the I/O connector. If the EXTINTEN bit in Command Register 1 is set and this bit is cleared, the external EXTINT* signal has caused the current interrupt. When the interrupt caused by the EXTINT* signal is served, your external device should drive EXTINT* to inactive state (logic high), or undrive it. |
| 2 | CNTINT | Counter Interrupt Bit—This bit reflects the interrupt status caused by the counter 2 output signal. If the CNTINTEN bit in Command Register 3 is set, a low-to-high transition on counter 2 output sets this bit and generates an interrupt request. Clear this bit by writing to the CNTINTCLR Register. |
| 1 | DATAERR /OVERFLOW | Data Error/Overflow Bit—This bit indicates if an overflow or overrun error has occurred. On the PC-LPM-16PnP, this bit is the data error bit. If this bit is cleared, no error was encountered. If this bit is set, the A/D FIFO has overflowed because the data acquisition servicing operation could not keep up with the sampling rate, or an A/D conversion was initiated before the previous A/D conversion was complete. To distinguish between the overflow and overrun error conditions, examine the OVERFLOW and OVERRUN bits in Status Register 2. Clear this bit by writing to the A/D Clear Register.<br><br>On the PC-LPM-16PnP, this bit only indicates that an overflow has occurred. |

| | | |
|---|---|---|
| 0 | DAVAIL | Data Available Bit—This bit indicates whether conversion output is available. If this bit is set, the ADC is finished with the last conversion and the result can be read from the FIFO. This bit is cleared if the FIFO is empty.<br><br>Writing to the ADCLR Register sets this bit on the PC-LPM-16 only. You need a FIFO (low and high bytes) reading to completely empty the PC-LPM-16 FIFO. On the PC-LPM-16PnP, the DAVAIL bit always exactly represents whether data is in the FIFO. |

## Status Register 2

Status Register 2 contains supplementary error information. This register is only on the PC-LPM-16PnP.

**Address:** 01(hex)

**Type:** Read-only

**Word Size:** 8-bit

**Bit Map:**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | OVERFLOW | OVERRUN |

| Bit | Name | Description |
|---|---|---|
| 7–2 | X | Don't care bits. |
| 1 | OVERFLOW | Overflow Bit—This bit indicates if an overflow error has occurred. If this bit is cleared, no error was encountered. If this bit is set, the A/D FIFO has overflowed because the data acquisition servicing operation could not keep up with the sampling rate. To clear this bit, write to the A/D Clear Register. |
| 0 | OVERRUN | Overrun Bit—This bit indicates whether an A/D conversion was initiated before the previous A/D conversion was complete. OVERRUN is an error condition that will occur if the data acquisition sample interval is too small (sample rate is too high). If OVERRUN is set, one or more conversions was skipped. If OVERRUN is cleared, no overrun condition has occurred. To clear this bit, write to the A/D Clear Register. |

## Analog Input Register Group

The three registers that make up the Analog Input Register Group control the analog input circuitry and can be used to read the FIFO. Reading the FIFO Register returns stored A/D conversion results. Writing to the A/D Clear Register clears the data acquisition circuitry.

Bit descriptions for the registers making up the Analog Input Register Group are given on the following pages.

## A/D FIFO Low-Byte Register and A/D FIFO High-Byte Register

The 13-bit A/D conversion results are sign-extended to 16-bit data in two's complement format and are stored in a 16-word deep A/D FIFO buffer. Two 8-bit registers, the A/D FIFO Low-Byte Register and the A/D FIFO High-Byte Register, must be read to return an A/D conversion value stored in the A/D FIFO. The A/D FIFO Low-Byte Register, which must be read first, contains the low byte of the 16-bit value, and the A/D FIFO High-Byte Register contains the high byte of the 16-bit value.

☞ **Note:** ***The A/D FIFO Low-Byte Register MUST be read first.***

The value read is removed from the A/D FIFO, thereby freeing space to store another A/D conversion value.

The A/D FIFO is empty after reading all the values it contains. The Status Register should be checked before the A/D FIFO Register is read. If the A/D FIFO contains one or more A/D conversion values, the DAVAIL bit is set in the Status Register, and the external device can read the A/D FIFO Register to retrieve a value. If the DAVAIL bit is cleared, the A/D FIFO is empty, in which case reading the A/D FIFO Register returns meaningless information.

The values returned by reading the A/D FIFO Registers are available in two's complement binary format. When the analog input range is unipolar, any small negative value returned from FIFO should be explained as zero.

**Address:** A/D FIFO Low-Byte Register — Base address + 02 (hex)
A/D FIFO High-Byte Register — Base address + 03 (hex)

**Type:** Read-only

**Word Size:** 8-bit

**Bit Map:** Two's complement binary mode

**High Byte**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

{---Sign and Sign Extension Bits---}

**Low Byte**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

## A/D FIFO Low-Byte Register and A/D FIFO High-Byte Register

**(Continued)**

| Bit | Name | Description |
|---|---|---|
| **High Byte** | | |
| 7–0 | D<15..8> | A/D Conversion Data Bits 15 through 8—These bits contain the high byte of the 16-bit, sign-extended two's complement result of a 13-bit A/D conversion. Values made up of D<15..0>, therefore, range from -4096 to +4095 decimal (F000 to 0FFF hex). Two's complement mode is useful for bipolar analog input readings because the values read reflect the polarity of the input signal. In unipolar mode only the positive value is used. |
| **Low Byte** | | |
| 7–0 | D<7..0> | A/D Conversion Data Bits 7 through 0—These bits contain the low byte of the 16-bit, sign-extended two's complement result of a 12-bit A/D conversion. |

☞ **Note:** ***The ADC resolution is actually 13 bits, not 12 bits. NI-DAQ only returns a 12-bit value, and the PC-LPM-16/PnP boards are tested only to 12-bit accuracy. However, by writing register-level programming, you can use the full 13 bits. The ADC always returns values from -4,096 to +4,095. For unipolar mode, if you want 12-bit resolution instead of 13-bit, you should ignore any negative value, giving a range of 0 to +4.095. For bipolar mode, you can divide the value returned by the ADC by two, giving a range of -2,048 to +2.047. Refer to the*** *A/D FIFO Output Binary Modes* ***section in this appendix for more information about 13- and 12-bit conversions.***

## A/D Clear Register

Write to this register to reset the ADC. This operation clears the data FIFO. All error bits in the Status Register are cleared as well. For the PC-LPM-16 (non PnP only), writing to this register clears the data FIFO and loads a single conversion into the FIFO. After writing to the A/D Clear Register, it is necessary to read both the High- and Low-Byte FIFOs. The data that is read back should be ignored.

**Address:** Base address + 01 (hex)

**Type:** Write-only

**Word Size:** 8-bit

**Bit Map:** Not applicable, no bits used

## Counter/Timer (MSM82C53) Register Group

The five registers making up the Counter/Timer Register Group access the onboard MSM82C53 counter/timer. The MSM82C53 has three counters: counter 0, counter 1, and counter 2. Counter 0 controls onboard data acquisition timing, and all three counters are available for general-purpose timing functions.

The MSM82C53 has three independent 16-bit counters and one 8-bit Mode Register. The Mode Register sets the mode of operation for each of the three counters. Writing to the Timer Interrupt Clear Register clears the interrupt request asserted when a low pulse is detected on the output of counter 2.

Bit descriptions for the registers in the Counter/Timer Register Group are given in the following pages.

## Counter 0 Data Register

Use the Counter 0 Data Register to load and read back contents of MSM82C53 counter 0.

**Address:** Base address + 08 (hex)

**Type:** Read-and-write

**Word Size:** 8-bit

**Bit Map:**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| Bit | Name | Description |
|---|---|---|
| 7–0 | D<7..0> | A/D Conversion Data Bits 7 through 0—8-bit counter 0 contents. |

## Counter 1 Data Register

Use the Counter 1 Data Register to load and read back contents of MSM82C53 counter 1.

**Address:** Base address + 09 (hex)

**Type:** Read-and-write

**Word Size:** 8-bit

**Bit Map:**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| Bit | Name | Description |
|---|---|---|
| 7–0 | D<7..0> | A/D Conversion Data Bits 7 through 0—8-bit counter 1 contents. |

## Counter 2 Data Register

Use the Counter 2 Data Register to load and read back contents of MSM82C53 counter 2.

**Address:** Base address + 0A (hex)

**Type:** Read-and-write

**Word Size:** 8-bit

**Bit Map:**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| Bit | Name | Description |
|---|---|---|
| 7–0 | D<7..0> | A/D Conversion Data Bits 7 through 0—8-bit counter 2 contents. |

## Counter Mode Register

The Counter Mode Register determines the operation mode for each of the three counters on the MSM82C53 chip. The Counter Mode Register selects the counter involved, the counter's read/load mode, its operation mode (that is, any of the six operation modes of the MSM82C53), and the counting mode (binary or BCD).

The Counter Mode Register is an 8-bit register. Bit descriptions for each of these bits are included in Appendix B, *MSM82C53 Data Sheet*.

**Address:** Base address + 0B (hex)

**Type:** Write-only

**Word Size:** 8-bit

**Bit Map:**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SC1 | SC0 | RL1 | RL0 | M2 | M1 | M0 | BCD |

| Bit | Name | Description |
|---|---|---|
| 7–6 | SC<1..0> | Counter Select Bits—These bits select the counter on which the command operates. |

| SC1 | SC0 | Operation |
|---|---|---|
| 0 | 0 | Select counter 1 |
| 0 | 1 | Select counter 2 |
| 1 | 0 | Select counter 3 |
| 1 | 1 | Read-back command |

## Counter Mode Register

**(Continued)**

5–4 RL<1..0> Read/Write Select Bits—These bits select data written to or read from a counter, or these bits send a Counter Latch command.

| RL1 | RL0 | Operation |
|---|---|---|
| 0 | 0 | Counter Latch command |
| 0 | 1 | Read and write least significant byte only |
| 1 | 0 | Read and write most significant byte only |
| 1 | 1 | Read and write least significant byte then most significant byte |

The Counter Latch command latches the current count of the register selected by SC1 and SC0. The next read from the selected counter returns the latched data.

## Counter Mode Register

**(Continued)**

3–1 M<2..0> Counter Mode Select Bits—These bits select the counting mode of the selected counter. The following table lists six available modes and the corresponding bit settings. Refer to Appendix B, *MSM82C53 Data Sheet*, for additional information.

| M2 | M1 | M0 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | Mode 0—Interrupt on terminal count |
| 0 | 0 | 1 | Mode 1—Hardware retriggerable one shot |
| 0 | 1 | 0 | Mode 2—Rate generator |
| 0 | 1 | 1 | Mode 3—Square wave mode |
| 1 | 0 | 0 | Mode 4—Software retriggerable strobe |
| 1 | 0 | 1 | Mode 5—Hardware retriggerable strobe |

0 BCD Binary Coded Decimal Select Bit—If BCD is set, the selected counter keeps count in BCD. If BCD is cleared, the selected counter keeps count in 16-bit binary.

## Timer Interrupt Clear Register

Write to the Timer Interrupt Clear Register to clear the interrupt request asserted when a low pulse is detected on the counter 2 output.

**Address:** Base address + 06 (hex)

**Type:** Write-only

**Word Size:** 8-bit

**Bit Map:** Not applicable, no bits used.

## Digital I/O Register Group

The Digital I/O Register Group contains two registers, the Digital Output Register and the Digital Input Register. The Digital Output Register drives the eight digital output lines of the I/O connector. The Digital Input Register returns the digital state of the eight digital input lines of the I/O connector.

Bit descriptions for the register in the Digital I/O Register Group follow.

## Digital Output Register

Write to the Digital Output Register to control the eight digital output lines of the I/O connector. The pattern contained in the Digital Output Register is driven onto the eight digital output lines of the I/O connector.

**Address:** Base address + 04 (hex)

**Type:** Write-only

**Word Size:** 8-bit

**Bit Map:**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| Bit | Name | Description |
|---|---|---|
| 7–0 | D<7..0> | 8-Bit Output Data 7 through 0—These eight bits control the digital output lines DOUT 0 through DOUT 7. |

## Digital Input Register

Read the Digital Input Register to return the logic state of the I/O connector's eight digital input lines.

**Address:** Base address + 05 (hex)

**Type:** Read-only

**Word Size:** 8-bit

**Bit Map:**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| Bit | Name | Description |
|---|---|---|
| 7–0 | D<7..0> | 8-Bit Input Data Bit—These eight bits represent the logic state of the digital input lines DIN 0 through DIN 7. |

# Programming Considerations

Following are programming instructions for operating the circuitry on the PC-LPM-16/PnP. To program the PC-LPM-16/PnP, you must write to and read from the various registers on the board. The following programming instructions are language-independent; that is, they tell you to write a value to a given register, to set or clear a bit in a given register, or to detect whether a given bit is set or cleared without presenting the actual code.

## Register Programming Considerations

The PC-LPM-16/PnP can only be used for 8-bit I/O transfers, so all the I/O read-and-write operations are 8-bit operations.

Several write-only registers on the PC-LPM-16/PnP contain bits that control several independent pieces of the onboard circuitry. In the set or clear instructions provided, you should set or clear specific register bits without changing the current state of the remaining bits in the register. However, writing to these registers affects all register bits simultaneously. You cannot read these registers to determine which bits have been set or cleared in the past; therefore, you should maintain a software copy of the write-only registers. You can then read this software copy to determine the status of the write-only registers. To change the state of a single bit without disturbing the remaining bits, set or clear the bit in the software copy and then write the software copy to the register.

## Initializing the PC-LPM-16/PnP

You must initialize the PC-LPM-16/PnP hardware for the circuitry to operate properly. To initialize the PC-LPM-16/PnP hardware, complete the following steps:

1. Write 00 (hex) to the Command Register 2.
2. Write 80 (hex) to the Command Register 1.
3. Write 34 (hex) to the Counter Mode Register.
4. Write 00 (hex) to the Timer Interrupt Clear Register.
5. Write 00 (hex) to the A/D Clear Register.
6. Read from A/D FIFO High-Byte and Low-Byte Registers and ignore the data.

This sequence leaves the PC-LPM-16/PnP circuitry in the following state:

- Counter 0 output is high.
- Multichannel scan is disabled.
- All interrupts are disabled.
- Analog input circuitry is initialized to channel 0.
- The A/D FIFO is cleared.

For additional details concerning the MSM82C53 counter/timer, see Appendix B, *MSM82C53 Data Sheet*.

## Programming the A/D Calibration

The ADC is a self-calibration converter and a self-calibration cycle adjusts positive linearity and full-scale errors. To start a self-calibration cycle, perform the following steps:

1. Write 01 to Command Register 2 to enable the self-calibration cycle.
2. Read Command Register 2 to start the self-calibration cycle and ignore the result of the reading.
3. Read the Status Register and check the CONVPROG bit. After starting the self-calibration, checking this bit can detect the completion of the self-calibration cycle. A one in this bit indicates the calibration is in progress, and zero indicates the completion of the calibration.
4. After the self-calibration cycle, write 0 to Command Register 2 to enable the A/D conversion.

The ADC should be calibrated after the reference has stabilized, although you may recalibrate it later to adjust to changes over time or temperature.

## Programming the Analog Input Circuitry

This section describes the analog input circuitry programming sequence and explains the A/D conversion results and how to clear the analog input circuitry.

## Analog Input Circuitry Programming Sequence

1. Initiate an A/D conversion.

   A low to high transition on OUT0 or on EXTCONV* initiates A/D conversion. Clear the CALEN bit in Command Register 2 to enable counter 0 and the EXTCONV*.

   When an A/D conversion is initiated, the ADC stores the result in the A/D FIFO at the end of its conversion cycle. If EXTCONV* initiates the conversion, OUT0 must be set high.

2. Read the A/D conversion result.

   Read the A/D FIFO Register to get the A/D conversion results. Before you read the A/D FIFO, however, you must read the Status Register to determine whether the A/D FIFO contains any results.

   To read the A/D conversion results, complete the following steps:

   a. Read the Status Register (8-bit read).

   b. If the DAVAIL bit is set (bit 0), read the A/D FIFO Low-Byte Register first, then read the A/D FIFO High-Byte Register to get the result. The first reading returns the low byte of 16-bit data, and the second reading returns the high byte.

Reading the Low and High-Byte A/D FIFO Registers removes the A/D conversion result from the A/D FIFO.

The DAVAIL bit indicates whether one or more A/D conversion results are stored in the A/D FIFO. If the DAVAIL bit is cleared, the A/D FIFO is empty and reading the A/D FIFO Register returns meaningless data. When an A/D conversion is initiated, the DAVAIL bit should be set after 20 µs. If you use EXTCONV* for A/D timing, the DAVAIL bit should be set 20 µs after a rising edge in EXTCONV*.

An A/D FIFO overflow condition occurs if you initiate more than 256 conversions and store them in the A/D FIFO before reading the A/D FIFO Register. If this condition occurs, the OVERFLOW bit is set in the Status Register 2 to indicate that one or more A/D conversion results have been lost because of FIFO overflow. Write to the A/D Clear Register to reset this error flag.

## A/D FIFO Output Binary Modes

The A/D conversion result stored in the A/D FIFO is a 16-bit two's complement value. It is made of 13-bit magnitude and 3-bit sign extension. If the analog input range is unipolar 0 to +10 V or unipolar 0 to +5 V, use the positive values only, making the resolution 12-bit. If the analog input range is ±5 V or ±2.5 V, you can divide the result by two to yield a 12-bit resolution reading. Also, if you want, the full 13-bit resolution can be used with the bipolar ranges. Notice, however, that in Appendix A, *Specifications*, LSB refers to the least significant bit of a 12-bit conversion value. Table D-2 shows input voltage versus A/D conversion values for the 0 to +10 V input range. Table D-3 shows input voltage versus A/D conversion values for -5 to +5 V input range.

**Table D-2.** Unipolar Input Mode A/D Conversion Values

| Input Voltage | A/D Conversion Result Range: 0 to +10 V | |
|---|---|---|
| | (Decimal) | (Hex) |
| 0 | 0 | 0000 |
| 2.5 | 1,024 | 0400 |
| 5.0 | 2,048 | 0800 |
| 7.5 | 3,072 | 0C00 |
| 9.9976 | 4,095 | 0FFF |

**Table D-3.** Bipolar Input Mode A/D Conversion Values

| Input Voltage | A/D Conversion Result Range: -5 to +5 V (13-bit values) | | A/D Conversion Result Divided by 2 (12-bit values) | |
|---|---|---|---|---|
| | (Decimal) | (Hex) | (Decimal) | (Hex) |
| -5.0 | -4,096 | F000 | -2,048 | F800 |
| -2.5 | -2,048 | F800 | -1,024 | FC00 |
| 0 | 0 | 0000 | 0 | 0000 |
| 2.5 | 2,048 | 0800 | 1,024 | 0400 |
| 4.9976 | 4,095 | 0FFF | 2,047 | 07FF |

## Clearing the Analog Input Circuitry

Write to the A/D Clear Register to clear the analog input circuitry, which leaves the analog input circuitry in the following state:

- Analog input error flag OVERFLOW is cleared.
- Pending interrupt requests are cleared.

To empty the A/D FIFO before starting any A/D conversions, perform two 8-bit reads on the A/D FIFO Registers and ignore the data read. This operation guarantees that the A/D conversion results read from the A/D FIFO are from the initiated conversions rather than leftover results from previous conversions.

To clear the analog input circuitry and the A/D FIFO:

- Write 0 to the A/D Clear Register (8-bit write).

# Programming Multiple A/D Conversions on a Single Input Channel Using Counter 0

This manual refers to a sequence of timed A/D conversions as a data acquisition operation. Counter 0 of the MSM82C53 is used as the sample-interval counter. In a data acquisition operation, counter 0 continuously generates the conversion pulses. The software keeps track of the number of conversions that have occurred and turns off counter 0

after getting the required number of conversions. The number of conversions in a single data acquisition operation in this case is unlimited. Counter 0 is clocked by a 1 MHz clock upon start up.

Each of these programming steps is explained as follows.

1. Select the Analog Input Channel.

   Write to Command Register 1 to select the analog input channel. The SCANEN* bit must be set for data acquisition operations on a single channel. See the *Command Register 1* bit descriptions earlier in this appendix for analog input channel bit patterns.

   Write to Command Register 1 only when the analog input channel, scanning mode, or interrupt mode needs to be changed.

   To enable the data acquisition operation, clear the CALEN bit of Command Register 2.

2. Program the Sample-Interval Counter (counter 0).

   Counter 0 of the MSM82C53 counter/timer is used as the sample-interval counter. A low-to-high transition on OUT0 (counter 0 output) initiates a conversion. You can program counter 0 to generate a pulse once every *N* µs. *N* is referred to as the sample interval; that is, the time between successive A/D conversions. *N* can be between 20 and 65,535. The sample interval is equal to the period of the timebase clock used by counter 0 multiplied by *N*. A 1 MHz clock is internally connected to CLK0 (the clock used by counter 0).

   Use the following programming sequence to program counter 0, the sample-interval counter. All writes are 8-bit write operations. All values given are hexadecimal.

   a. Write 34 to the Counter Mode Register (select counter 0, mode 2).

   b. Write the least significant byte of the sample interval to the Counter 0 Data Register.

   c. In Step a., writing to the Counter Mode Register forces OUT0 to high. To finish programming counter 0, you must also write the most significant byte. However, this writing starts the counting, so perform this writing in step 4.

3. Clear the A/D circuitry.

   Before starting the data acquisition operation, empty the A/D FIFO to clear out any old A/D conversion results. You must do this after programming the counters in case any spurious edges were caused

during the programming. Write 0 to the A/D Clear Register to empty the FIFO (8-bit write), then read the low and high bytes from the A/D FIFO (PC-LPM-16 only).

4. Start and service the data acquisition operation.

   To start the data acquisition operation, write the most significant byte of the sample interval to the Counter 0 Data Register. This enables counter 0 to start counting.

   When the data acquisition operation starts, service the operation by reading the A/D FIFO Register every time an A/D conversion result becomes available. Perform the following sequence until you have read the desired number of conversion results:

   a. Read the Status Register (8-bit read).

   b. If the DAVAIL bit is set (bit 0), read the A/D FIFO Register to get the result.

You can also use interrupts to service the data acquisition operation. This topic is discussed in the *A/D Interrupt Programming* section later in this appendix.

An overflow error condition may occur during a data acquisition operation. This error condition is reported through the Status Register, and the overflow should be checked every time the Status Register is read.

An overflow condition occurs if more than 256 A/D conversions have been stored in the A/D FIFO since the A/D FIFO was last read; that is, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, at least one A/D conversion result is lost. An overflow condition has occurred if the OVERFLOW bit in the Status Register is set.

Clear the OVERFLOW bit in the Status Register by writing to the A/D Clear Register.

To stop the A/D conversion sequence, write 34 to the Counter 0 Mode Register. This stops the generation of pulses on OUT0.

## Programming Multiple A/D Conversions Using External Timing

You can use the external timing signal EXTCONV* for multiple A/D conversions. A low-to-high transition of EXTCONV* initiates an A/D conversion. Software can also initiate a data acquisition operation. Setting the DISABDAQ bit in Command Register 2 disables the EXTCONV* signal. Clearing the DISABDAQ bit in Command Register 2 enables the EXTCONV* signal and starts the data acquisition operation. To use the EXTCONV* signal, the OUT0 of counter 0 must be driven high. Otherwise, EXTCONV* is disabled.

Each of these programming steps is explained as follows:

1. Disable the A/D conversion.

   Writing 2 to Command Register 2 to set the DISABDAQ bit disables the A/D conversion. The pulse on the EXTCONV* line is ignored.

2. Program counter 0.

   High output of counter 0 enables the EXTCONV* signal. Write 34 to the Counter Mode Register to force OUT0 high (enable EXTCONV*). Writing 30 to the Counter Mode Register forces OUT0 low, which disables the EXTCONV* and stops the data acquisition operation.

3. Select the analog input channel.

   Write to Command Register 1 to select the analog input channel. The SCANEN* bit must be set for data acquisition operation on a single channel. See Command Register 1 bit descriptions earlier in this appendix for analog input channel bit descriptions.

4. Clear the A/D circuitry.

   Before starting the data acquisition operation, empty the A/D FIFO to clear any old A/D conversion results. Write 0 to the A/D Clear Register and read the A/D FIFO Low- and High-Byte registers to empty the FIFO. Ignore the data.

5. Start and service the data acquisition operation.

   Clear the DISABDAQ bit in Command Register 2 to start the data acquisition sequence.

   a. Write 0 to Command Register 2 to enable the A/D conversion.

   b. The next EXTCONV* signal initiates an A/D conversion. The operation must be serviced by reading the A/D FIFO Register every time an A/D conversion result becomes available. To

service the data acquisition, perform the following sequence until you have read the desired number of conversion results:

1. Read the Status Register
2. If the DAVAIL bit is set, read the A/D FIFO Low-Byte Register first, then read the A/D FIFO High-Byte Register, to get the result.

Interrupts can also be used to service the data acquisition operation. This topic is discussed under *A/D Interrupt Programming* later in this appendix.

An overflow error condition may occur during a data acquisition operation. This error condition is reported through the Status Register and the OVERFLOW bit should be checked every time the Status Register is read to check the DAVAIL bit.

An overflow condition occurs if more than 256 A/D conversions have been stored in the A/D FIFO since the A/D FIFO was last read; that is, the A/D FIFO is full and cannot accept any more data. This condition occurs if the software loop reading the A/D FIFO Register is not fast enough to keep up with the A/D conversion rate. When an overflow occurs, you lose at least one A/D conversion result. An overflow condition has occurred if you clear the OVERFLOW bit in the Status Register.

Reset the OVERFLOW bit in the Status Register by writing to the A/D Clear Register.

## Programming Multiple A/D Conversions with Channel Scanning

The data acquisition programming sequences given earlier in this appendix are for programming the PC-LPM-16PnP for multiple A/D conversions on a single input channel. You can also program the PC-LPM-16/PnP for scanning analog input channels during the data acquisition operation. Analog channels *N* through 0 can be scanned, where *N* can be 1 through 15. Also, 0 through *N* can be scanned. Programming scanned multiple A/D conversions involves the same sequence of steps as single-channel data acquisition operations except that the SCANEN* bit is cleared in Command Register 1. When the SCANEN* bit is cleared in Command Register 1, the analog channel-select bits MA<3..0> select the highest numbered channel in the scan sequence. For example, if MA<3..0> is 0011 (binary)—that is, channel 3 is selected and the SCANEN* bit is cleared, and the

UP/DOWN bit in Command Register 2 is cleared—the software uses the following scan sequence:

channel 3, channel 2, channel 1, channel 0, channel 3, channel 2, channel 1, channel 0, channel 3, and so on.

Perform the following steps to select the analog input channel:

1. Program the UP/DOWN bit in Command Register 2 if the bit is not already set to the desired value. Common Register 2 must always be programmed before Command Register 1.

☞ **Note:** ***The UP function is not yet supported by NI-DAQ. NI-DAQ will support the UP function in a future release.***

2. Write the configuration value indicating the highest channel number in the scan sequence to Command Register 1. You must set the SCANEN* bit during this first write to Command Register 1.
3. Write the same configuration value again to Command Register 1. The SCANEN* bit, however, must be cleared during the second write to Command Register 1.

Use either counter 0 or EXTCONV* to control the scanning interval.

## A/D Interrupt Programming

You can use an interrupt to service the data acquisition operation. To use the conversion interrupt, set the FIFOINTEN bit in Command Register 1. If this bit is set, an interrupt is generated whenever the DAVAIL bit in the Status Register is set. Clear this interrupt condition by reading the FIFO, which empties its contents.

## Programming the Digital I/O Circuitry

DIN0 through DIN7 (pins 22 through 29) of the I/O connector are dedicated digital input lines. They are monitored by the Digital Input Register. An 8-bit reading of the Digital Input Register returns the current state of these digital input lines. DOUT0 through DOUT7 (pins 30 through 37) of the I/O connector are dedicated digital output lines. These lines are always driven by the Digital Output Register. An 8-bit writing to the Digital Output Register drives the new digital value to these lines. At startup, all of the digital output lines are initiated to zero state.

## Programming the MSM82C53 Counter/Timer

Counters 0, 1, and 2 of the MSM82C53 counter/timer (except the CLK0 signal of counter 1) are available for general-purpose timing applications. Counter 0 has a fixed 1 MHz clock input and can be used as the sample interval counter of A/D conversion. Write and read operations to the MSM82C53 are 8-bit operations. For general programming details, refer to Appendix B, *MSM82C53 Data Sheet*.

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Appendix E

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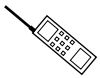
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Instruments used _____

_____

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Configuration _____

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Configuration _____

The problem is: _____

_____

_____

_____

_____

List any error messages: _____

_____

_____

The following steps reproduce the problem: _____

_____

_____

_____

_____

_____

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| Prefix | Meaning | Value |
|---|---|---|
| p- | pico- | $10^{-12}$ |
| n- | nano- | $10^{-9}$ |
| μ- | micro- | $10^{-6}$ |
| m- | milli- | $10^{-3}$ |
| k- | kilo- | $10^{3}$ |
| M- | mega- | $10^{6}$ |
| G- | giga- | $10^{9}$ |

## Symbols

| | |
|---|---|
| ° | degrees |
| – | negative of, or minus |
| Ω | ohms |
| / | per |
| % | percent |
| ± | plus or minus |
| + | positive of, or plus |
| $\sqrt{\ }$ | square root of |
| +5 V | +5 VDC source signal |

# A

| | |
|---|---|
| A | amperes |
| AC | alternating current |
| ACH | analog input channel signal |
| A/D | analog-to-digital |
| ADC | A/D converter |
| AI | analog input |
| AIGATE | analog input gate signal |
| AIGND | analog input ground signal |
| AISENSE | analog input sense signal |
| ANSI | American National Standards Institute |
| AOGND | analog output ground signal |
| ASIC | application-specific integrated circuit |
| AWG | American Wire Gauge |

# B

| | |
|---|---|
| BBS | bulletin board support |
| BCD | binary-coded decimal |
| BIOS | basic input/output system or built-in operating system |

# C

| | |
|---|---|
| C | Celsius |
| cm | centimeter |
| CMOS | complementary metal-oxide semiconductor |

| | |
|---|---|
| CTR | counter |

## D

| | |
|---|---|
| DAQ | data acquisition |
| DC | direct current |
| DMA | direct memory access |

## E

| | |
|---|---|
| EISA | Extended Industry Standard Architecture |
| ESP | Engineering Software Package |

## F

| | |
|---|---|
| F | farads |
| FIFO | first-in-first-out |
| ft | feet |

## H

| | |
|---|---|
| h | hour |
| hex | hexadecimal |
| Hz | hertz |

## I

| | |
|---|---|
| I/O | input/output |
| $I_{OH}$ | current, output high |
| $I_{OL}$ | current, output low |

| | |
|---|---|
| ISA | Industry Standard Architecture |

## L

| | |
|---|---|
| LED | light emitting diode |
| LSB | least significant bit |

## M

| | |
|---|---|
| m | meter |
| MB | megabytes of memory |
| MSB | most significant bit |

## P

| | |
|---|---|
| PC | personal computer |

## R

| | |
|---|---|
| RAM | random access memory |
| rms | root mean square |

## S

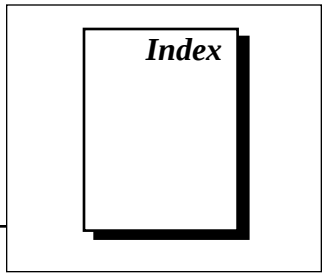
| | |
|---|---|
| s | seconds |
| S | samples |
| SCANCLK | scan clock signal |
| SCXI | Signal Conditioning eXtensions for Instrumentation |
| SISOURCE | SI counter clock signal |
| STARTSCAN | start scan signal |

## T

| | |
|---|---|
| TTL | transistor-transistor logic |

## V

| | |
|---|---|
| V | volts |
| VDC | volts direct current |
| VI | virtual instrument |
| $V_{IH}$ | volts, input high |
| $V_{IL}$ | volts, input low |
| $V_{in}$ | volts in |
| $V_{OH}$ | volts, output high |
| $V_{OL}$ | volts, output low |




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