# 5

# Common-Source Amplifier Stage

Two types of common-source amplifiers will be investigated in lab projects. One is with the source grounded and the other is with a current-source bias (dual power supply). In Units 5.1 and 5.2 we discuss various aspects of the common-source stage with grounded source, in Unit 5.3 we take up circuit-linearity considerations, and in Unit 5.4 we cover the basics of the dual-power-supply amplifier. Both amplifiers are based on the PMOS, as in the projects. The first two units are mostly a review of the basic amplifier as presented in previous units, to reinforce the basic concepts. The PMOS replaces the NMOS (Units 2 and 4) in this unit, to provide familiarity with the opposite polarity in bias considerations and to illustrate that the linear model applies in the same manner for both transistor types.

## 5.1 DC (Bias) Circuit

Dc circuits for the grounded-source amplifier are shown in Fig. 5.1 (PMOS). The circuit in (a) is based on a single power supply, and the gate bias is obtained with a resistor voltage-divider network. The circuit in (b) is for a laboratory project amplifier. Both $V_{GG}$ and $V_{SS}$ are negative, since the source is at ground. There is no voltage drop across $R_G$ since there is negligible gate current. $R_G$ is necessary only to prevent shorting the input signal, $v_i$. The bias current $I_D$ for a given applied $V_{SG}$ will respond according to (3.8), which is

$$I_D = k_p (V_{SG} - V_{tpo})^2 (1 + \lambda_p V_{SD})$$

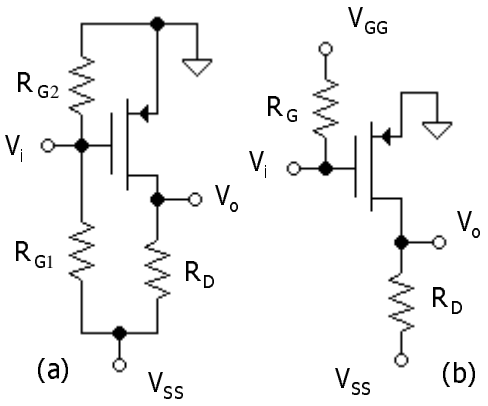


**Fig. 5.1** Basic PMOS common-source amplifiers. Single-power-supply amplifier (a) and laboratory amplifier (b) with $V_{SG}$ (= $V_{GG}$) and $V_{SS}$ controlled by DAQ output channels. Note that either end of the circuit of (a) can be at ground.

The two circuits are equivalent, as $V_{GG}$ and $R_G$ of Fig. 5.1.b are the Thévenin equivalent of the bias network of the Fig. 5.1(a). In the project on the amplifier, they are actually a voltage and a resistor. This is not a bias-stable circuit, as a slight change in $V_{SG}$ or the transistor parameters can result in a significant change in $I_D$. The dual-power-supply circuit of Unit 5.4 is considerably better in this respect.

# 5.2 Amplifier Voltage Gain

This dc (bias) circuit becomes an amplifier now simply by adding a signal source at the gate as in Fig. 5.2. This requires a coupling capacitor, as shown here in the complete circuit, to prevent disturbing the bias upon connecting the input signal to the circuit.

In the amplifier of Project 5, the signal will be superimposed on the bias voltage at the node of $V_{GG}$. This can be facilitated with LabVIEW and the DAQ. A capacitor, as in an actual amplifier, is therefore not required. The requirement for having LabVIEW control over both $V_{GG}$ and $V_{SS}$, and the limitation of two output channels, dictates this configuration.

In Project 5 we measure the gain as a function of bias current, $I_D$. For a SPICE comparison, we need an expression for the gain. For the ideal case, which neglects the output conductance, $g_{ds}$, the output current is related to the input voltage by (4.1), which is

$$I_d = g_m V_{gs} = g_m V_i$$

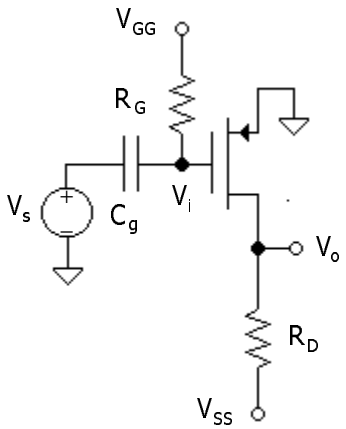


**Fig. 5.2** A signal source is connected to the gate through a coupling capacitor. The capacitor is necessary to isolate the dc circuit from the signal source.

The output signal voltage is, in general,

$$V_{ds} = V_o = -I_d R_D \tag{5.1}$$

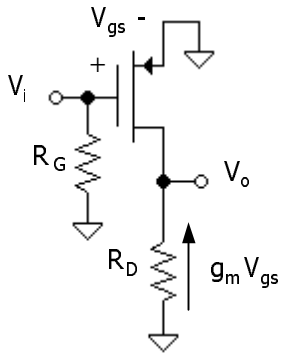


**Fig. 5.3** Signal-equivalent version of the amplifier stage. Dc nodes are set to zero volts (circuit reference). The reactance of $C_g$ is assumed to be zero.

The convention used here for subscript order for signal (linear) variables is common to the NMOS and PMOS. This is consistent with the fact that the linear model does not distinguish between the two types. Thus, for example, the dc terminal voltage for a PMOS is $V_{SG}$, but the signal equivalent is $V_{gs}$ (Fig. 5.3) and the signal input voltage is positive at the input terminal (common-source, gate input). For the PMOS, $i_D$ is defined as positive out of the drain, but the signal output current is into the drain (as in the NMOS). We note that a positive $V_{gs}$ ($V_{gs} = -V_{sg}$) corresponds to a decrease in the total gate – source voltage, $v_{SG}$, which is consistent with a decrease of $i_D$ and positive $I_d$.

Thus, the negative sign in (5.1) is consistent with the flow of current $I_d$ up through the resistor (Fig. 5.3) for positive $V_i = V_{gs}$. The common-source stage is an inverting amplifier and has an inherent $180°$ phase shift. From (4.1) and (5.1), the gain is

$$a_v = \frac{V_o}{V_i} = -g_m R_D \tag{5.2}$$

where both $V_i = V_{gs}$ and $V_o = V_{ds}$ are with respect to ground or the source terminal for the common-source stage.

If the output resistance, $1/g_{ds}$, cannot be neglected (which is the case for the project on PMOS amplifiers), the transistor current, $g_m V_i$, is shared between the output resistance and $R_D$. The portion that flows through $R_D$ is (Fig. 5.4)

$$I_{R_D} = g_m V_i \frac{1}{1 + g_{ds} R_D} \tag{5.3}$$

Note again that the signal schematic transistor represents a current source with value $g_m V_i$, as established in connection with Fig. 4.1. The additional feature of the transistor model is included with the addition of $1/g_{ds}$. This resistance is actually part of the transistor and is between the drain and source of the transistor, but the circuit as given is equivalent, as the source is at ground. Since the output voltage is $V_o = -I_{R_D} R_D$, the new gain result is

$$a_v = -g_m \frac{R_D}{1 + g_{sd} R_D} \tag{5.4}$$

Note that this form evolves from ideal transistor current, $g_m V_{gs}$, flowing through the parallel combination of the output resistance and $R_D$.

To facilitate an intuitive grasp of the magnitude of the effect of $g_{ds}$, we use the expression for $g_{ds}$ (4.13) in (5.4), to obtain

$$a_v = -g_m \frac{R_D}{1 + \lambda_p I_D R_D} \tag{5.5}$$

Note that $I_D R_D$ is the voltage drop across $R_D$. For example, for a $-10$-V power supply, we choose $I_D R_D \approx 5$ V. A measurement of $\lambda_p$ for our devices will show that

$\lambda_p \approx 1/20$ V, which results in $\lambda_p I_D R_D \approx 1/4$. Thus, the effect of $g_{ds}$ $(= \lambda_p I_D)$ for this case is significant.

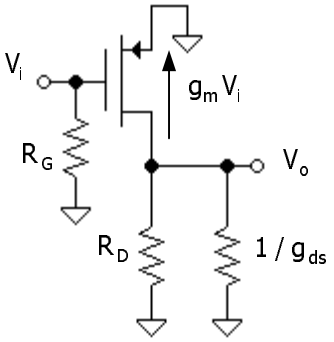


**Fig. 5.4** Common-source amplifier stage signal circuit, with all dc nodes set to zero volts. The transistor model includes output resistance $1/g_{ds}$, which appears directly in parallel with $R_D$ with the source grounded.

Finally, we can get an overall current dependence for $a_v$ with the elimination of $g_m$, using (4.5) with $k_p' \approx k_p$, which results in

$$a_v = -2\sqrt{k_p I_D}\,\frac{R_D}{1+\lambda_p I_D R_D} \tag{5.6}$$

Using an alternative form for $g_m$ $(= 2I_D / V_{effp})$, also (4.5), the gain expression is

$$a_v = -2\frac{I_D}{V_{effp}}\,\frac{R_D}{1+\lambda_p I_D R_D} \tag{5.7}$$

where

$$V_{effp} = \sqrt{\frac{I_D}{k_p(1+\lambda_p V_{SD})}} \approx \sqrt{\frac{I_D}{k_p}}$$

For simplicity, approximate forms of (4.5) and (4.13) of $g_m$ and $g_{ds}$ are used here, which are independent of $V_{SD}$. For reference, the "exact" and approximate forms of (4.5) and (4.13), respectively, are repeated here:

$$g_m = 2\sqrt{k_p(1+\lambda_p V_{SD})I_D} \approx 2\sqrt{k_p I_D}$$

and

$$g_{ds} = \lambda_p \frac{I_D}{1 + \lambda_p V_{SD}} \approx \lambda_p I_D$$

The "exact" equations of $g_m$ and $g_{ds}$ are used in conjunction with the amplifier projects to compare the computed gain with the measured gain plotted against $I_D$. This is done in both LabVIEW and Mathcad. Parameters $k_p$ and $V_{tpo}$ (to get $V_{effp}$) will be extracted from the measured dc data, and $\lambda_p$ will be used as an adjustable parameter to fit the SPICE and measured gain data.

# 5.3 Linearity of the Gain of the Common-Source Amplifier

The connection between $I_d$ and $V_{gs}$ is linear provided that $V_{gs}$ is small enough, as considered in the following units. Use of the linear relations also assumes that the output signal remains in the active region (i.e., neither in the linear region nor near cutoff). This is discussed below. NMOS subscripts are used. The results are the same for the PMOS, with a "p" subscript substituted for "n" and the subscript order reversed for all bias-voltage variables.

## 5.3.1 Nonlinearity Referred to the Input

The general equation again is (3.8)

$$i_D = k_n' (v_{GS} - V_{tno})^2$$

Then using $I_d = i_D - I_D$ and $v_{GS} = V_{GS} + V_{gs}$, the equation for the incremental drain current becomes

$$I_d = k_n' \left[ 2 (V_{GS} - V_{tno}) V_{gs} + V_{gs}^2 \right] \tag{5.8}$$

which leads to a nonlinear (variable) transconductance, $g_m'$, given by

$$g_m' = \frac{I_d}{V_{gs}} = \frac{k_n' \left( 2 V_{effn} V_{gs} + V_{gs}^2 \right)}{V_{gs}} = g_m \left( 1 \pm \frac{|V_{gs}|}{2 V_{effn}} \right) \tag{5.9}$$

Therefore, the condition for linearity is that $V_{gs} << 2V_{eff}$, with $V_{effn} = V_{GS} - V_{tno}$

and using $g_m = 2k_n' V_{effn}$.

With this condition not satisfied, an output signal is distorted. However, for the purpose of measuring the amplifier gain, our signal voltmeter will take the average of the positive and negative peaks, which is

$$I_{davg} = \frac{k_n'\left(2V_{eff}V_{gs} + V_{gs}^2\right) + k_n'\left(2V_{eff}V_{gs} - V_{gs}^2\right)}{2} \tag{5.10}$$

In the parabolic relationship, the squared terms cancel entirely. In general, though, the output signal contains harmonic content (distortion) when $V_{gs}$ is too large compared to $V_{effn}$.

## 5.3.2 Nonlinearity Referred to the Output

The discussion above of limits imposed on $V_{gs}$ assumes that the transistor remains in the active mode. To clarify this point, reference is made to the output characteristics of Fig. 5.5. The graph has plots of the output characteristic for three values of $v_{GS}$ in addition to the load line. The characteristic plot in the midrange is for no signal. Operating point variables are $V_{DS} \approx 2.5\ V$ and $I_D \approx 40\ \mu A$. With a large, positive $V_{gs}$, the characteristic moves up to the high-level plot ($i_{Dhi}$) and the opposite occurs for a large but negative $V_{gs}$ ($i_{Dlo}$). The high-level plot is shown for when the transistor is about to move out of the active region and into the linear region. Attempts to force $v_{DS}$ to lower values will create considerable distortion in the output signal voltage. The lower curve suggests that the positive output signal is on the verge of being cut off (clipped) for an additional increase in the negative-input signal voltage.

According to the discussion above, the negative signal output voltage is limited to

$$V_{dsminus} = V_{DS} - V_{effn} \tag{5.11}$$

Technically, $V_{effn}$ is from the high-current signal state, but for simplicity, a reasonable estimate can be made from the dc case; that is, $V_{effn} = V_{GS} - V_{tno}$. The positive signal limit is

$$V_{dsplus} = V_{DD} - V_{DS} = I_D R_D \tag{5.12}$$

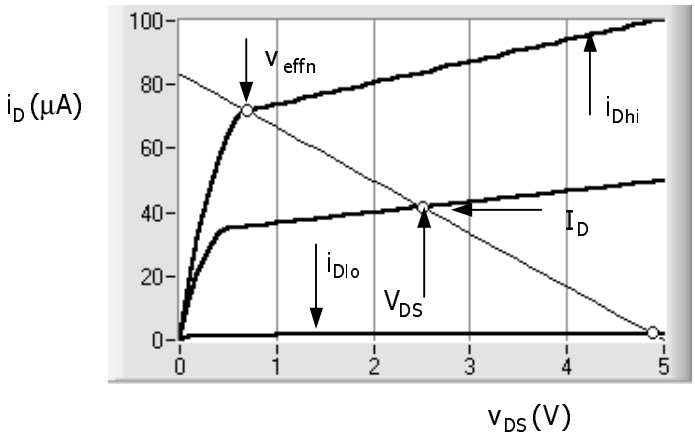


**Fig. 5.5** Common-source amplifier stage output characteristics. Output characteristics are from top to bottom, large high-current signal swing, $i_{Dhi}$, dc bias, $I_D$, low-current signal swing, $i_{Dlo}$. Also shown is the load line. The current – voltage circuit solution is always the intersection between a given characteristic and the load line.

The actual output-signal limit is dictated by the smaller of the two for a symmetrical periodic signal such as a sine-wave. In the example shown in Fig. 5.5, $V_{effn} \approx 0.5\ V$, $V_{DS} \approx 2.5\ V$, and $V_{DD} = 5\ V$. The plus and minus signal-voltage limits are about $2.5\ V$ and $2.0\ V$, respectively. Depending on the dc bias, the limit could be dictated by one or the other. In the amplifier projects, the gain will typically be measured over a range of dc bias current for a fixed resistor. This means that for the low-current end of the scan, the signal will be limited by the magnitude of $I_D R_D$ and, by design, the plus and minus swings will be made to be about equal at the highest dc current.

Distortion associated with the nonlinear $I_d - V_{gs}$ relation and that due to signal limits at the output may be taking place simultaneously. This is seen from the gain expression (5.7) $(g_{ds} = 0)$

$$|a_v| \approx 2\frac{V_{R_D}}{V_{effp}}$$

where $a_v \equiv V_{ds} / V_{gs}$ and where the approximation is for the case of neglecting the $\lambda_n$ factor. Thus, for a given $V_{ds}$, $V_{gs}$ is

$$V_{gs} = \frac{V_{effp}}{2V_{R_D}} V_{ds} \tag{5.13}$$

If, for example, $V_{ds}$ is pushed to the positive output-signal limit, then $V_{ds} \approx V_{R_D}$. According to (5.13), $V_{gs} = V_{effp}/2$, and $V_{gs}$ exceeds the condition for a linear $I_d - V_{gs}$ relation as given in (5.9),

$$g'_m = \frac{I_d}{V_{gs}} = g_m \left(1 \pm \frac{|V_{gs}|}{2V_{effn}}\right)$$

# 5.4 Current-Source Common-Source Amplifier: Common-Source Amplifier with a Source Resistor

The bias circuit of the current-source bias amplifier, shown in Fig. 5.6, has a dual power supply. One advantage of this is that the input is at zero dc volts such that the signal can be connected directly without interfering with the bias. The dc circuit equation for setting up the bias is

$$I_D = \frac{V_{DD} - V_{SG}}{R_S} \tag{5.14}$$

where ($k'_p \approx k_p$) $V_{SG} \approx \sqrt{I_D / k_p} + V_{tp}$.

This circuit is more bias stable than the grounded source amplifier, as slight changes in $V_{SG}$ (due to device parameter variations or temperature) are usually small compared to $V_{DD}$. Note that $V_{tp}$ is used in lieu of $V_{tpo}$ as $V_{BS} \neq 0$. The chip (CD4007) used in the projects is a p-well device (as noted in Unit 3), with the NMOS transistors in the well. The well is connected to $V_{SS}$, while the body of the chip is connected, as in Fig. 5.6, to $V_{DD}$. The pn junction formed by the well and the bulk is thus reverse-biased with a voltage $|V_{SS}| + V_{DD}$.

In the amplifier projects, however, we have the latitude to connect the body and source as there is only one transistor in the circuit and the body can float along with the source. Thus we can assume that $V_{tp} = V_{tpo}$. As shown in Fig. 5.7, the signal circuit requires the addition of a bypass capacitor, $C_s$. This places the source at signal ground provided that the capacitor is large enough. The criterion

for this is discussed in Unit 6. The voltage-gain equation is the same as in the amplifier, with the source actually grounded.

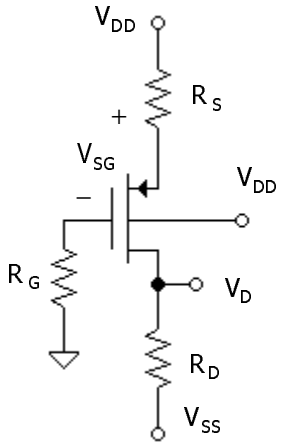


**Fig. 5.6** Dc circuit of the dual-power-supply common-source amplifier. The gate is at ground potential, allowing the signal to be connected directly to the gate. $R_G$ is necessary only to prevent shorting out the input signal.

Without the bypass capacitor, $R_S$ is in the signal circuit and a fraction of the applied signal voltage at the gate is dropped across the resistor. The signal circuit for this case is shown in Fig. 5.8. The circuit transconductance of the amplifier with $R_S$ was discussed initially in Unit 4. This is reviewed in the following.

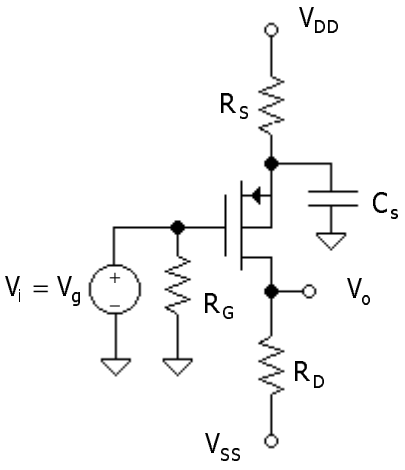


**Fig. 5.7** Amplifier circuit with a bypass capacitor attached between the source and ground to tie the source to signal ground. Signal input is attached directly to the gate. Body and source are connected internally in the project chip for the transistor used in the amplifier.

An applied input signal, $V_i = V_g$, divides between the gate – source terminals and the source resistor according to [(4.6)]

$$V_g = V_{gs} + I_d R_S$$

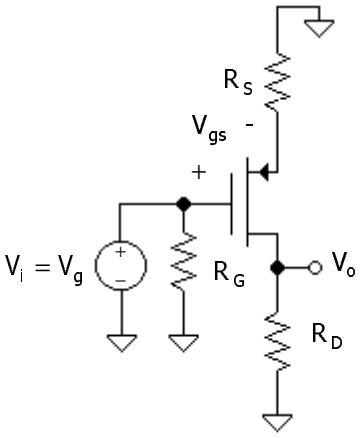


**Fig. 5.8** Signal circuit for dual-power supply common-source amplifier. Input signal voltage, $V_i$, is divided between $V_{gs}$, the control voltage, and the source resistor according to the ratio $1 : g_m R_S$.

When combing this with $I_d = g_m V_{gs}$, we obtain [(4.7)]

$$V_g = V_{gs} + g_m V_{gs} R_S = (1 + g_m R_S) V_{gs} = (1 + g_m R_S) \frac{I_d}{g_m}$$

The circuit transconductance, $G_m$, is then [(4.8)]

$$G_m = \frac{I_d}{V_g} = \frac{g_m}{1 + g_m R_S}$$

The gain for this case is thus (neglecting $g_{ds}$)

$$a_v = \frac{V_d}{V_g} = -G_m R_D = -\frac{g_m R_D}{1 + g_m R_S} \tag{5.15}$$

In one of the amplifier projects, $R_S = R_D$, and the gain without the bypass capacitor is actually less than unity.

# 5.5 Design of a Basic Common-Source Amplifier

Unlike in the laboratory environment, an actual practical common-source amplifier would have a single power supply for the base and collector circuit bias. Also, the circuit design requires a tolerance to a wide range of parameter

variation, including that due to temperature change. In this unit, the design process for a possible common-source amplifier is discussed. Emphasis is on dc bias stability, that is, on tolerance to device parameter and circuit component variations.

The common-source amplifier to be designed is shown in Fig. 5.9. Source resistor, $R_S$, is included for bias (and gain) stabilization. The goal is for the circuit to function properly for any NMOS transistor, which has device parameters $k_n$ and $V_{tno}$ that fall into a wide range of values, as is normally expected. Tolerance to component variation, such as resistor values, could also be built into the design.

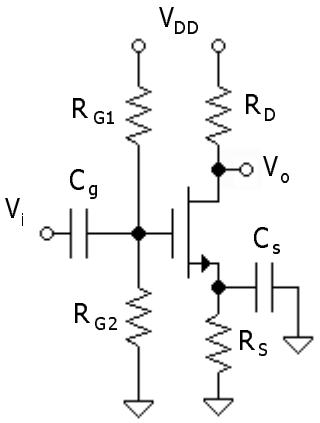


**Fig. 5.9** NMOS common-source amplifier with $R_S$ for bias and gain stabilization. Gate bias is provided by a voltage-divider network consisting of $R_{G1}$ and $R_{G2}$. The body and source terminals are connected.

Gate voltage $V_G$ is provided by the voltage divider, consisting of resistors $R_{G1}$ and $R_{G2}$. Since there is no gate current, the gate bias voltage is [(1.2)]

$$V_G = \frac{R_{G2}}{R_{G2} + R_{G1}} V_{DD}$$

Voltage $V_G$ is thus relatively stable and can be considered constant. Once $V_G$ has been established, the drain current will be dictated by

$$I_D = \frac{V_G - V_{GS}}{R_S} \tag{5.16}$$

Since the gate – source voltage is given by

$$V_{GS} = \sqrt{\frac{I_D}{k_n}} + V_{tno} \tag{5.17}$$

the drain current, $I_D$, may be expressed in terms of the device parameters as

$$I_D = \frac{V_G - \sqrt{\frac{I_D}{k_n}} - V_{tno}}{R_S} \tag{5.18}$$

This result reveals the dependence of $I_D$ on the magnitudes of $k_n$ and $V_{tno}$. (Again, for simplicity, as in the amplifier projects, we will assume that the body and source are connected such that $V_{tn} = V_{tno}$.)

Bias current $I_D$ is assumed to be a given. The initial design then is conducted for the NMOS nominal, average values for $k_n$ and $V_{tno}$. Any combination of $V_G$ and $R_S$ that satisfies (5.18) will provide the design $I_D$. Specific values for $V_G$ and $R_S$ will be dictated by stability requirements. Suppose that $k_n$ is expected to fall within $k_{no} \pm \delta k_n$ and $V_{tno}$ within $V_{tnoo} \pm \delta V_{tno}$, where $k_{no}$ and $V_{tnoo}$ are the nominal values of the original design. Assume that the design bias current associated with $k_{no}$ and $V_{tnoo}$ is $I_{Do}$. At the extremes for the parameters, the low and high currents will be

$$I_{Dlo,Dhi} = \frac{V_G - \sqrt{\frac{I_D}{k_{no} \mp \delta k_n}} - (V_{tnoo} \pm \delta V_{tno})}{R_S} \tag{5.19}$$

Resistor $R_S$, for the given $V_G$ and design drain current, is

$$R_S = \frac{V_G - V_{GSo}}{I_{Do}} \tag{5.20}$$

$V_{GSo}$ is obtained from (5.17), using the nominal parameter values. The low and high current limits tend to converge on $V_G / R_S$ as $V_G$ becomes large. That is, in the limit, $V_G$ dominates the voltages in the numerator of (5.19), thus rendering the expression insensitive to the minor contributions from changes in $k_n$ and $V_{tno}$.

An important design consideration is drain – source voltage, $V_{DS}$, as this dictates the output signal range. This is calculated from

$$V_{DS} = V_{DD} - I_D(R_D + R_S) \tag{5.21}$$

In the design of the amplifier, drain resistor $R_D$ is normally selected for equal positive and negative peak-signal maximums. This configuration is illustrated in Fig. 5.10, which shows the output characteristic of the transistor in the circuit. The signal is limited by $V_{DD} - V_{R_S}$ and $V_{effno} = V_{GSo} - V_{tno}$ at the high and low ends of the voltage range, respectively. Therefore, nominal bias should be set at

$$V_{DSo} = \frac{V_{DD} - I_{Do}R_S + V_{effno}}{2} \tag{5.22}$$

For simplicity, it is assumed that $v_{effn} \approx V_{effno}$. $V_{effno}$, $V_{DDo}$, and $I_{Do}$ are the bias values at the nominal parameter values. The bias drain voltage is $V_{DSo}$ plus the drop across $R_S$, that is,

$$V_{Do} = V_{DSo} + I_{Do}R_S \tag{5.23}$$

Knowing $V_{Do}$ then provides for the calculation of $R_D$ from

$$R_D = \frac{V_{DD} - V_{Do}}{I_{Do}} \tag{5.24}$$

where $V_{Do}$ and $I_{Do}$ are for the initial design with $k_{no}$ and $V_{tnoo}$.

An optimization design sequence plots the limits for a range of $V_G$ and for specified $\delta V_{tno}$ and $\delta k_n$. An example is shown in Fig. 5.11. The plot of $V_{DSo}$ corresponds to the nominal $k_{no}$ and $V_{tnoo}$. The curve slopes downward as $I_D R_S$ increases for increasing $V_G$ at constant nominal bias current, $I_{Do}$. $V_{DShi}$ is for the combination of $\delta V_{tno}$ and $\delta k_n$, which gives the maximum positive deviation from the nominal, and $V_{DSlo}$ is the opposite. The example of Fig. 5.11 is for $V_{DD} = 10$ V and design bias current of $I_{Do} = 100\,\mu A$ and nominal parameters $k_{no} = 300\ \mu A/V^2$, $V_{tnoo} = 1.5$ V, $\delta V_{tno} = 0.1$ V, and $\delta k_n = 100\ \mu A/V^2$. Experience with the CMOS chip of our amplifier project (Project 7) indicates that these are representative.

Figure 5.12 shows plots of the computed positive and negative signal-peak limits. Due to the increasing $V_{R_S}$ with increasing $V_G$, the signal range decreases, as shown by the plots. Thus, the signal-peak limits have a maximum, as is evident in the graph. The design of the amplifier uses $V_G$ at the maximum of the lower

curve. The value of $V_G$ is consistent with the maximum $V_{DSlo}$ in the plot of Fig. 5.11. In the example, $V_G \approx 3$ V.

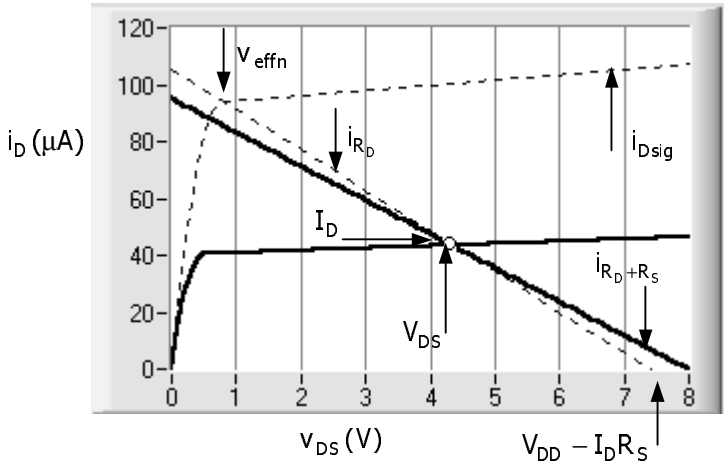


**Fig. 5.10** Output characteristic of the transistor of the amplifier with bias $V_{DS}$ set approximately according to (5.22). The signal is restricted within the range $V_{DD} - V_{R_S}$ and approximately $v_{effn}$. The characteristic curves are for no signal (solid plot) and for the signal at a maximum (dashed plot), as limited by the transistor going into the inactive (linear) region. The load lines are dc (solid line) and signal (ac, dashed line).

Once $V_G$ is determined, the selection of $R_{G1}$ is made from (1.2), which is

$$V_G = \frac{R_{G2}}{R_{G2} + R_{G1}} V_{DD} = \frac{R_G}{R_{G1}} V_{DD}$$

where $R_G$ is the parallel combination

$$R_G = \frac{R_{G2} R_{G1}}{R_{G2} + R_{G1}}$$

$R_G$ can be selected somewhat arbitrarily but could be dictated by the coupling capacitor, $C_g$, requirement. Associated with the coupling capacitor is the 3-dB frequency (6.2), which is

$$f_{3dB} = \frac{1}{2\pi R_G C_g}$$

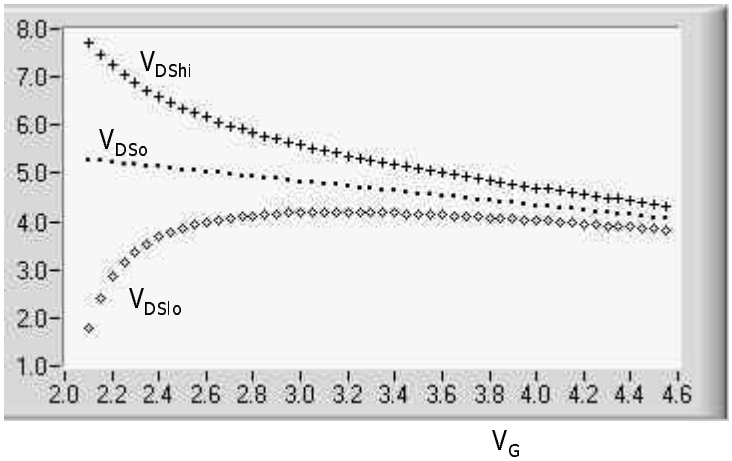


**Fig. 5.11** Computed high and low range of $V_{DS}$ as a function of gate-bias voltage $V_G$. The computation is with $k_{no} = 300\ \mu A/V^2$, $V_{tnoo} = 1.5\ V$, $\delta V_{tno} = 0.1\ V$, and $\delta k_n = 100\ \mu A/V^2$.

$R_{G2}$ is then calculated from

$$R_{G2} = \frac{R_{G1}R_G}{R_{G1} - R_G}$$

The gain equations for the circuit of Fig. 5.9, with and without a bypass capacitor, are (5.2) and (5.15), respectively. These are

$$a_v = -g_m R_D$$

and

$$a_v = -\frac{g_m R_D}{1 + g_m R_S}$$

In the design procedure outlined in this unit, emphasis is on stability and the gain falls out. This would typically be the case for this type of amplifier. We note that due to the characteristically small $g_m$ of MOSFETs, the voltage gain is

relatively small. Gain can be improved considerably through the use a current-source load, as in the amplifier of Unit 10.

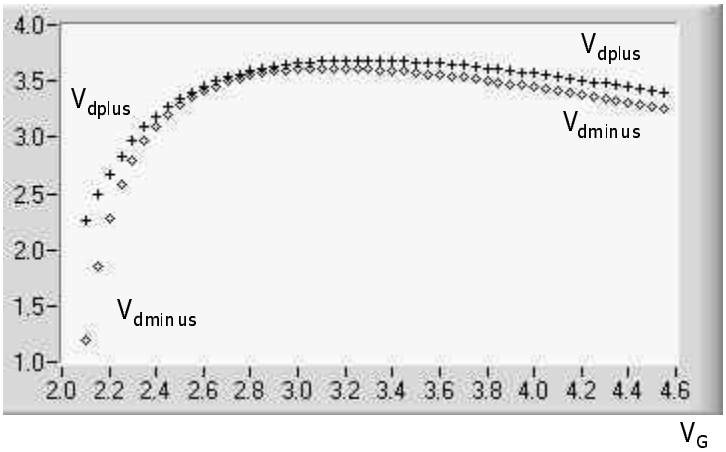


**Fig. 5.12** Computed maximums for negative and positive output voltage signal peaks as a function of $V_G$: $V_{dplus}$, positive maximum; $V_{dminus}$, negative maximum.

# 5.6 Summary of Equations

| | |
|---|---|
| $a_v = -g_m R_D$ | Common-source amplifier-stage voltage gain. |
| $a_v = -g_m \frac{R_D}{1 + \lambda_p I_D R_D}$ | Common-source amplifier gain including output resistance, PMOS. (Same for NMOS with $\lambda_n$.) |
| $g_m' = g_m \left(1 \pm \frac{\lvert V_{gs} \rvert}{2V_{effn}}\right)$ | Nonlinear transconductance for large input signals. (Same for PMOS with $V_{effp}$.) |
| $V_{dsminus} = V_{DS} - V_{effn}$ | Negative output signal limit, NMOS. |
| $V_{dsminus} = V_{SD} - V_{effp}$ | Negative output signal limit, PMOS. |
| $V_{dsplus} = V_{DD} - V_{DS} = I_D R_D$ | Positive output signal limit, NMOS. |
| $V_{dsplus} = \lvert V_{SS} \rvert - V_{SD} = I_D R_D$ | Positive output signal limit, PMOS. |
| $a_v = -\frac{g_m R_D}{1 + g_m R_S}$ | Voltage gain of common-source stage with source resistor. |
| $G_m = \frac{g_m}{1 + g_m R_S}$ | Circuit transresistance of common-source stage with source resistor. |

# 5.7 Exercises and Projects

Project Mathcad Files Exercise05.mcd - Project05.mcd

**Laboratory Project 5** PMOS Common-Source Amplifier

P5.2 PMOS Common-Source Amplifier DC Setup

P5.3 Amplifier Gain at One Bias Current

P5.4 Amplifier Gain versus Bias Current