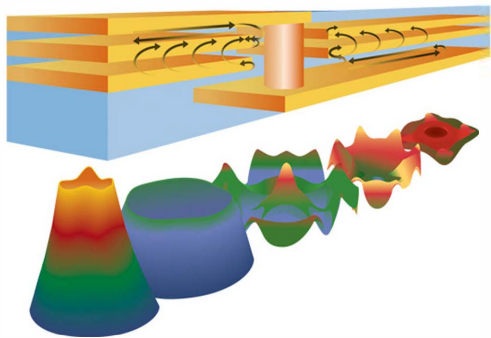


Signal and Power Integrity—

SIMPLIFIED

Second Edition



Eric Bogatin

Modern Semiconductor Design Series
Signal Integrity Library

FREE SAMPLE CHAPTER



SHARE WITH OTHERS

SIGNAL AND POWER INTEGRITY—

SIMPLIFIED

SECOND EDITION

Modern Semiconductor Design Series

James R. Armstrong and F. Gail Gray

VHDL Design Representation and Synthesis

Mark Gordon Arnold

Verilog Digital Computer Design: Algorithms into Hardware

Jayaram Bhasker

A VHDL Primer, Third Edition

Mark D. Birnbaum

Essential Electronic Design Automation (EDA)

Eric Bogatin

Signal and Power Integrity—Simplified, Second Edition

Douglas Brooks

Signal Integrity Issues and Printed Circuit Board Design

Ken Coffman

Real World FPGA Design with Verilog

Alfred Crouch

Design-for-Test for Digital IC's and Embedded Core Systems

Dennis Derickson and Marcus Müller (Editors)

Digital Communications Test and Measurement

Greg Edlund

Timing Analysis and Simulation for Signal Integrity Engineers

Daniel Foty

MOSFET Modeling with SPICE: Principles and Practice

Tom Granberg

Handbook of Digital Techniques for High-Speed Design

Nigel Horspool and Peter Gorman

The ASIC Handbook

William K. Lam

Hardware Design Verification

Geoff Lawday, David Ireland, and Greg Edlund

A Signal Integrity Engineer's Companion

Mike Peng Li

Jitter, Noise, and Signal Integrity at High-Speed

Farzad Nekoogar and Faranak Nekoogar

From ASICs to SOCs: A Practical Approach

Farzad Nekoogar

Timing Verification of Application-Specific Integrated Circuits (ASICs)

Samir Palnitkar

Design Verification with e

David Pellerin and Scott Thibault

Practical FPGA Programming in C

Christopher T. Robertson

Printed Circuit Board Designer's Reference: Basics

Chris Rowen

Engineering the Complex SOC

Madhavan Swaminathan and A. Ege Engin

Power Integrity Modeling and Design for Semiconductors and Systems

Wayne Wolf

FPGA-Based System Design

Wayne Wolf

Modern VLSI Design, Fourth Edition: IP-Based Design

SIGNAL AND POWER INTEGRITY— SIMPLIFIED

SECOND EDITION

Eric Bogatin

Upper Saddle River, NJ • Boston • Indianapolis • San Francisco
New York • Toronto • Montreal • London • Munich • Paris • Madrid
Capetown • Sydney • Tokyo • Singapore • Mexico City

Many of the designations used by manufacturers and sellers to distinguish their products are claimed as trademarks. Where those designations appear in this book, and the publisher was aware of a trademark claim, the designations have been printed with initial capital letters or in all capitals.

The author and publisher have taken care in the preparation of this book, but make no expressed or implied warranty of any kind and assume no responsibility for errors or omissions. No liability is assumed for incidental or consequential damages in connection with or arising out of the use of the information or programs contained herein.

The publisher offers excellent discounts on this book when ordered in quantity for bulk purchases or special sales, which may include electronic versions and/or custom covers and content particular to your business, training goals, marketing focus, and branding interests. For more information, please contact:

U.S. Corporate and Government Sales
(800) 382-3419
corpsales@pearsontechgroup.com

For sales outside the United States, please contact:

International Sales
international@pearson.com

Visit us on the Web: informit.com

Library of Congress Cataloging-in-Publication Data

Bogatin, Eric.

Signal and power integrity—simplified / Eric Bogatin. —2nd ed.
p. cm.

Rev. ed. of: Signal and power integrity—simplified / Eric Bogatin. c2004.

Includes bibliographical references and index.

ISBN-10: 0-13-234979-5 (hardcover : alk. paper)

ISBN-13: 978-0-13-234979-6 (hardcover : alk. paper)

1. Signal processing—Digital techniques. 2. Impedance (Electricity) 3.

Signal integrity (Electronics) I. Bogatin, Eric. Signal integrity—simplified. II. Title.

TK5102.9.B58 2010

621.382'2—dc22

2009021261

Copyright © 2010 Pearson Education, Inc.

All rights reserved. Printed in the United States of America. This publication is protected by copyright, and permission must be obtained from the publisher prior to any prohibited reproduction, storage in a retrieval system, or transmission in any form or by any means, electronic, mechanical, photocopying, recording, or likewise. To obtain permission to use material from this work, please submit a written request to Pearson Education, Inc., Permissions Department, One Lake Street, Upper Saddle River, New Jersey 07458, or you may fax your request to (201) 236-3290.

ISBN-13: 978-0-13-234979-6

ISBN-10: 0-13-234979-5

Text printed in the United States on recycled paper at Edwards Brothers in Ann Arbor, Michigan.

Fourth printing, November 2013

The dedication of a book is called “The Dedication” because it requires dedication by the author to complete the work. As every author will tell you, writing is a solitary, alone process, the opposite of social activity. It’s easy to become engulfed in the writing and researching and exclude more and more of the real world. Successful authors are either not married or married to an understanding, supportive spouse who sees his or her role as providing a nurturing environment in which creative juices can ferment.

Susan, my wife, patiently put up with my solitary writing, giving me the space to put in the dedication to finish the first and second editions. At the same time, she was also my anchor to the real world and forced me to keep a healthy balance between alone work and social life. The second edition is as much due to her efforts as from mine, and as I get to write the words, I am dedicating the second edition to her.

This page intentionally left blank

C O N T E N T S

Preface to the Second Edition	xv
Preface to the First Edition	xvii
Acknowledgments	xxiii
About the Author	xxv
Chapter 1 Signal Integrity Is in Your Future	1
1.1 What Is Signal Integrity?	2
1.2 Signal Quality on a Single Net	5
1.3 Cross Talk	9
1.4 Rail-Collapse Noise	11
1.5 Electromagnetic Interference (EMI)	13
1.6 Two Important Signal Integrity Generalizations	16
1.7 Trends in Electronic Products	16
1.8 The Need for a New Design Methodology	22
1.9 A New Product Design Methodology	23
1.10 Simulations	24
1.11 Modeling and Models	27
1.12 Creating Circuit Models from Calculation	30
1.13 Three Types of Measurements	35
1.14 The Role of Measurements	38
1.15 The Bottom Line	39
Chapter 2 Time and Frequency Domains	43
2.1 The Time Domain	44
2.2 Sine Waves in the Frequency Domain	46
2.3 Shorter Time to a Solution in the Frequency Domain	48
2.4 Sine Wave Features	49
2.5 The Fourier Transform	51
2.6 The Spectrum of a Repetitive Signal	53

2.7	The Spectrum of an Ideal Square Wave	55
2.8	From the Frequency Domain to the Time Domain	57
2.9	Effect of Bandwidth on Rise Time	58
2.10	Bandwidth and Rise Time	62
2.11	What Does <i>Significant</i> Mean?	63
2.12	Bandwidth of Real Signals	67
2.13	Bandwidth and Clock Frequency	68
2.14	Bandwidth of a Measurement	70
2.15	Bandwidth of a Model	72
2.16	Bandwidth of an Interconnect	74
2.17	The Bottom Line	78
Chapter 3 Impedance and Electrical Models		81
3.1	Describing Signal-Integrity Solutions in Terms of Impedance	82
3.2	What Is Impedance?	84
3.3	Real Versus Ideal Circuit Elements	86
3.4	Impedance of an Ideal Resistor in the Time Domain	88
3.5	Impedance of an Ideal Capacitor in the Time Domain	89
3.6	Impedance of an Ideal Inductor in the Time Domain	92
3.7	Impedance in the Frequency Domain	94
3.8	Equivalent Electrical Circuit Models	99
3.9	Circuit Theory and SPICE	101
3.10	Introduction to Modeling	105
3.11	The Bottom Line	110
Chapter 4 The Physical Basis of Resistance		113
4.1	Translating Physical Design into Electrical Performance	114
4.2	The Only Good Approximation for the Resistance of Interconnects	115
4.3	Bulk Resistivity	118
4.4	Resistance per Length	119
4.5	Sheet Resistance	121
4.6	The Bottom Line	124
Chapter 5 The Physical Basis of Capacitance		127
5.1	Current Flow in Capacitors	128
5.2	The Capacitance of a Sphere	130
5.3	Parallel Plate Approximation	131
5.4	Dielectric Constant	133

5.5	Power and Ground Planes and Decoupling Capacitance	135
5.6	Capacitance per Length	138
5.7	2D Field Solvers	143
5.8	Effective Dielectric Constant	146
5.9	The Bottom Line	150
Chapter 6 The Physical Basis of Inductance		151
6.1	What Is Inductance?	151
6.2	Inductance Principle #1: There Are Circular Rings of Magnetic-Field Lines Around All Currents	152
6.3	Inductance Principle #2: Inductance Is the Number of Webers of Field Line Rings Around a Conductor per Amp of Current Through It	154
6.4	Self-Inductance and Mutual Inductance	156
6.5	Inductance Principle #3: When the Number of Field Line Rings Around a Conductor Changes, There Will Be a Voltage Induced Across the Ends of the Conductor	158
6.6	Partial Inductance	161
6.7	Effective, Total, or Net Inductance and Ground Bounce	167
6.8	Loop Self- and Mutual Inductance	173
6.9	The Power-Distribution Network (PDN) and Loop Inductance	178
6.10	Loop Inductance per Square of Planes	183
6.11	Loop Inductance of Planes and Via Contacts	184
6.12	Loop Inductance of Planes with a Field of Clearance Holes	187
6.13	Loop Mutual Inductance	188
6.14	Equivalent Inductance of Multiple Inductors	189
6.15	Summary of Inductance	191
6.16	Current Distributions and Skin Depth	193
6.17	High-Permeability Materials	202
6.18	Eddy Currents	204
6.19	The Bottom Line	206
Chapter 7 The Physical Basis of Transmission Lines		209
7.1	Forget the Word <i>Ground</i>	210
7.2	The Signal	211
7.3	Uniform Transmission Lines	212
7.4	The Speed of Electrons in Copper	214
7.5	The Speed of a Signal in a Transmission Line	215
7.6	Spatial Extent of the Leading Edge	219

7.7	“Be the Signal”	220
7.8	The Instantaneous Impedance of a Transmission Line	224
7.9	Characteristic Impedance and Controlled Impedance	227
7.10	Famous Characteristic Impedances	230
7.11	<i>The Impedance of a Transmission Line</i>	233
7.12	Driving a Transmission Line	238
7.13	Return Paths	241
7.14	When Return Paths Switch Reference Planes	244
7.15	A First-Order Model of a Transmission Line	257
7.16	Calculating Characteristic Impedance with Approximations	262
7.17	Calculating the Characteristic Impedance with a 2D Field Solver	265
7.18	An n-Section Lumped Circuit Model	270
7.19	Frequency Variation of the Characteristic Impedance	278
7.20	The Bottom Line	279
Chapter 8 Transmission Lines and Reflections		281
8.1	Reflections at Impedance Changes	282
8.2	Why Are There Reflections?	284
8.3	Reflections from Resistive Loads	288
8.4	Source Impedance	290
8.5	Bounce Diagrams	292
8.6	Simulating Reflected Waveforms	295
8.7	Measuring Reflections with a TDR	295
8.8	Transmission Lines and Unintentional Discontinuities	299
8.9	When to Terminate	301
8.10	The Most Common Termination Strategy for Point-to-Point Topology	304
8.11	Reflections from Short Series Transmission Lines	306
8.12	Reflections from Short-Stub Transmission Lines	309
8.13	Reflections from Capacitive End Terminations	311
8.14	Reflections from Capacitive Loads in the Middle of a Trace	314
8.15	Capacitive Delay Adders	317
8.16	Effects of Corners and Vias	319
8.17	Loaded Lines	325
8.18	Reflections from Inductive Discontinuities	327
8.19	Compensation	331
8.20	The Bottom Line	334

Chapter 9 Lossy Lines, Rise-Time Degradation, and Material Properties	337
9.1 Why Worry About Lossy Lines?	338
9.2 Losses in Transmission Lines	340
9.3 Sources of Loss: Conductor Resistance and Skin Depth	342
9.4 Sources of Loss: The Dielectric	346
9.5 Dissipation Factor	351
9.6 The Real Meaning of Dissipation Factor	354
9.7 Modeling Lossy Transmission Lines	360
9.8 Characteristic Impedance of a Lossy Transmission Line	367
9.9 Signal Velocity in a Lossy Transmission Line	369
9.10 Attenuation and the dB	371
9.11 Attenuation in Lossy Lines	376
9.12 Measured Properties of a Lossy Line in the Frequency Domain	385
9.13 The Bandwidth of an Interconnect	390
9.14 Time-Domain Behavior of Lossy Lines	397
9.15 Improving the Eye Diagram of a Transmission Line	400
9.16 Pre-emphasis and Equalization	402
9.17 The Bottom Line	403
Chapter 10 Cross Talk in Transmission Lines	405
10.1 Superposition	406
10.2 Origin of Coupling: Capacitance and Inductance	407
10.3 Cross Talk in Transmission Lines: NEXT and FEXT	409
10.4 Describing Cross Talk	411
10.5 The SPICE Capacitance Matrix	413
10.6 The Maxwell Capacitance Matrix and 2D Field Solvers	417
10.7 The Inductance Matrix	424
10.8 Cross Talk in Uniform Transmission Lines and Saturation Length	425
10.9 Capacitively Coupled Currents	431
10.10 Inductively Coupled Currents	435
10.11 Near-End Cross Talk	438
10.12 Far-End Cross Talk	441
10.13 Decreasing Far-End Cross Talk	448
10.14 Simulating Cross Talk	451
10.15 Guard Traces	457
10.16 Cross Talk and Dielectric Constant	464
10.17 Cross Talk and Timing	466

10.18	Switching Noise	469
10.19	Summary of Reducing Cross Talk	473
10.20	The Bottom Line	474

Chapter 11 Differential Pairs and Differential Impedance 475

11.1	Differential Signaling	476
11.2	A Differential Pair	480
11.3	Differential Impedance with No Coupling	482
11.4	The Impact from Coupling	486
11.5	Calculating Differential Impedance	493
11.6	The Return-Current Distribution in a Differential Pair	496
11.7	Odd and Even Modes	502
11.8	Differential Impedance and Odd-Mode Impedance	507
11.9	Common Impedance and Even-Mode Impedance	508
11.10	Differential and Common Signals and Odd- and Even-Mode Voltage Components	511
11.11	Velocity of Each Mode and Far-End Cross Talk	513
11.12	Ideal Coupled Transmission-Line Model or an Ideal Differential Pair	519
11.13	Measuring Even- and Odd-Mode Impedance	520
11.14	Terminating Differential and Common Signals	522
11.15	Conversion of Differential to Common Signals	529
11.16	EMI and Common Signals	534
11.17	Cross Talk in Differential Pairs	539
11.18	Crossing a Gap in the Return Path	542
11.19	To Tightly Couple or Not to Tightly Couple	544
11.20	Calculating Odd and Even Modes from Capacitance- and Inductance-Matrix Elements	546
11.21	The Characteristic Impedance Matrix	550
11.22	The Bottom Line	553

Chapter 12 S-Parameters for Signal Integrity Applications 555

12.1	S-Parameters, the New Universal Metric	555
12.2	What Are S-Parameters?	557
12.3	Basic S-Parameter Formalism	559
12.4	S-Parameter Matrix Elements	562
12.5	Simulating Return and Insertion Loss	567

12.6	A Transparent Interconnect	570
12.7	Changing the Port Impedance	573
12.8	The Phase of S_{21} for a Uniform 50-Ohm Transmission Line	574
12.9	The Magnitude of S_{21} for a Uniform Transmission Line	577
12.10	Coupling to Other Transmission Lines	582
12.11	Insertion Loss for Non-50-Ohm Transmission Lines	589
12.12	Data-Mining S-Parameters	594
12.13	Single-Ended and Differential S-Parameters	596
12.14	Differential Insertion Loss	601
12.15	The Mode Conversion Terms	605
12.16	Converting to Mixed-Mode S-Parameters	607
12.17	Time and Frequency Domains	609
12.18	The Bottom Line	613
Chapter 13 The Power Distribution Network (PDN)		615
13.1	The Problem	615
13.2	The Root Cause	618
13.3	The Most Important Design Guidelines for the PDN	620
13.4	Establishing the Target Impedance Is Hard	621
13.5	Every Product Has a Unique PDN Requirement	629
13.6	Engineering the PDN	631
13.7	The VRM	633
13.8	Simulating Impedance with SPICE	635
13.9	On-die Capacitance	637
13.10	The Package Barrier	639
13.11	The PDN with No Decoupling Capacitors	644
13.12	The MLCC Capacitor	646
13.13	The Equivalent Series Inductance	650
13.14	Approximating Loop Inductance	652
13.15	Optimizing the Mounting of Capacitors	661
13.16	Combining Capacitors in Parallel	667
13.17	Engineering a Reduced Parallel Resonant Peak by Adding More Capacitors	673
13.18	Selecting Capacitor Values	675
13.19	Estimating the Number of Capacitors Needed	681
13.20	How Much Does a nH Cost?	683
13.21	Quantity or Specific Values?	687

13.22	Sculpting the Impedance Profiles: The Frequency Domain Target Impedance (FDTI) Method	692
13.23	When Every pH Counts	699
13.24	Location, Location, Location	703
13.25	When Spreading Inductance Is the Limitation	707
13.26	The Chip View	710
13.27	Bringing It All Together	713
13.28	The Bottom Line	717
Appendix A 100 General Design Guidelines to Minimize Signal-Integrity Problems		719
Appendix B 100 Collected Rules of Thumb to Help Estimate Signal-Integrity Effects		727
Appendix C Selected References		739
Index		741

P R E F A C E T O T H E S E C O N D E D I T I O N

Since the publication of the first edition of *Signal Integrity—Simplified*, the principles of signal integrity haven't changed. What has changed, though, is the prolific use of high-speed serial links and the critical role power integrity now plays in the success or failure of new product introductions.

In addition to fleshing out more details and examples in many of the chapters, especially on differential pairs and losses, two new chapters have been added to this second edition to provide a strong foundation to meet the needs of today's engineers and designers.

This first new chapter—Chapter 12—provides a thorough introduction to the use of S-parameters in signal integrity applications. If you deal with any high-speed serial links, you will encounter S-parameters. Because they are written in the foreign language of the frequency domain, they are intimidating to the high-speed digital designer. Chapter 12, like all the chapters in this book, provides a solid foundation in understanding this formalism and enables all engineers to harness the great power of S-parameters.

Chapter 13, the second new chapter, is on power integrity. These issues increasingly fall in the lap of the design engineer. With higher speed applications, interconnects in the power distribution path affect not just power delivery, but also signals' return paths and passing an EMC certification test.

We start at the beginning and illustrate the role of the power distribution interconnects and how design and technology selection can make or break the performance of the power distribution network. The essential principles of plane

impedance, spreading inductance, decoupling capacitors, and the loop inductance of capacitors are introduced. This valuable insight helps feed the intuition of engineers enabling them to apply the power of their creativity to synthesize new designs. Hand in hand with the creation of a design is the analysis of its performance so that cost-performance trade-offs can be explored and the PDN impedance profile can be sculpted to perfection.

If you are new to signal integrity, this second edition of *Signal and Power Integrity—Simplified* provides your starting place to build a strong foundation and empowers you to get your new signal integrity designs right the first time, every time.

P R E F A C E T O T H E F I R S T E D I T I O N

“Everything should be made as simple as possible, but not simpler.”

Albert Einstein

Printed circuit-board and IC-package design used to be a field that involved expertise in layout, CAD, logic design, heat transfer, mechanical engineering, and reliability analysis. With modern digital electronic systems pushing beyond the 1-GHz barrier, packaging and board designers must now balance signal integrity and electrical performance with these other concerns.

Everyone who touches the physical design of a product has the potential of affecting the performance. All designers should understand how what they do will affect signal integrity or, at the very least, be able to talk with engineers who are responsible for the signal integrity.

The old design methodology of building prototypes, hoping they work, and then testing them to find out is no longer cost effective when time to market is as important as cost and performance. If signal integrity is not taken into account from the beginning, there is little hope a design will work the first time.

In our new “high-speed” world, where the packaging and interconnect are no longer electrically transparent to the signals, a new methodology for designing a product right the first time is needed. This new methodology is based on predictability. The first step is to use established design guidelines based on engineering discipline. The second step is to evaluate the expected performance by “putting in the numbers.” This is what distinguishes engineering from guesswork. It takes

advantage of four important tools: rules of thumb, analytic approximations, numerical simulation tools, and measurements. With an efficient design and simulation process, many of the trade-offs between the expected performance and the ultimate cost can be evaluated early in the design cycle, where the time, risk, and cost savings will have the biggest impact. The way to solve signal integrity problems is to first understand their origin and then apply all the tools in our toolbox to find and verify the optimum solution.

The design process is an intuitive one. The source of inspiration for a new way of solving a problem is that mysterious world of imagination and creativity. An idea is generated and the analytical powers of our technical training take over to massage the idea into a practical solution. Though computer simulations are absolutely necessary for final verification of a solution, they only rarely aid in our intuitive understanding. Rather, it is an understanding of the mechanisms, principles and definitions, and exposure to the possibilities, that contribute to the creation of a solution. Arriving at that initial guess and knowing the places to look for solutions require understanding and imagination.

This book emphasizes the intuitive approach. It offers a framework for understanding the electrical properties of interconnects and materials that apply across the entire hierarchy from on-chip, through the packages, circuit boards, connectors, and cables.

Those struggling with the confusing and sometimes contradictory statements made in the trade press will use this book as their starting place. Those experienced in electrical design will use this book as the place to finally understand what the equations mean.

In this book, terms are introduced starting at the ground floor. For example, the impedance of a transmission line is the most fundamental electrical property of an interconnect. It describes what a signal will see electrically and how it will interact with the interconnects. For those new to signal integrity, most of the problems arise from confusion over three terms: the *characteristic* impedance, the impedance, and the *instantaneous* impedance a signal sees. This distinction is even important for experienced engineers. This book introduces the reader to each of these terms and their meanings, without complex mathematics.

New topics are introduced at a basic level; most are not covered in other signal integrity books at this level. These include partial inductance (as distinct from loop inductance), the origin of ground bounce and EMI, impedance, transmission line discontinuities, differential impedance, and attenuation in lossy lines affecting

the collapse of the eye diagram. These topics have become critically important for the new high-speed serial links.

In addition to understanding the basic principles, leveraging commercially available tools is critical for the practicing engineer who wants to find the best answer in the shortest time. Tools for solving signal integrity problems fall in two categories: analysis and characterization. Analysis is what we usually refer to as a calculation. Characterization is what we usually refer to as a measurement. The various tools, guidelines on when they should be used, and examples of their value are presented throughout the book.

There are three types of analysis tools: rules of thumb, analytic approximations, and numerical simulation. Each has a different balance between accuracy and effort to use. Each has a right and a wrong place for its appropriate use. And each tool is important and should be in the toolbox of every engineer.

Rules of thumb, such as “the self inductance of a wire is about 25 nH/inch,” are important when having a quick answer NOW! is more important than having an accurate answer later. With very few exceptions, every equation used in signal integrity is either a definition or an approximation. Approximations are great for exploring design space and balancing design and performance trade-offs. However, without knowing how accurate a particular approximation really is, would you want to risk a \$10,000 board-fabrication run and four weeks of your schedule based on an approximation?

When accuracy is important, for example, when signing off on a design, numerical simulation is the right tool to use. In the last five years, a whole new generation of tools has become available. These new tools have the powerful combination of being both easy to use and accurate. They can predict the characteristic impedance, cross talk, and differential impedance of any cross-section transmission line and simulate how a signal might be affected by any type of termination scheme. You don’t have to be a Ph.D. to use this new generation of tools so there is no reason every engineer can’t take advantage of them.

The quality of the simulation is only as good as the quality of the electrical description of the components (i.e., the equivalent circuit models). Engineers are taught about circuit models of gates that perform all the information processing, but rarely are the circuit models of the interconnects reviewed. Fifteen years ago, when interconnects looked transparent to the signals, all interconnects were considered as ideal wires—no impedance and no delay. When these terms were added, they were lumped together as “parasitics.”

Today, in a high-speed digital system with a clock frequency above about 100 MHz, it is the real wires—the wire bonds, the package leads, the pins, the circuit board traces, the connectors, and the cabling—that create signal-integrity problems and can prevent products from working correctly the first time. Understanding these “analog” effects, designing for them, specifying correct values for them, and including them in the system simulations before the design is committed to hardware, can enable moving a more robust product to market more quickly.

This book provides the tools to enable all engineers and managers involved in chip packaging and board, connector and interconnect design, to understand how these passive elements affect the electrical performance of a system and how they can be incorporated in system simulation. It illustrates how to perform engineering estimates of important electrical parameters and evaluate technology trade-offs. Examples are selected from a wide variety of common systems, including on-chip interconnects, wire bonds, flip chip attach, multilayer circuit boards, DIPs, PGAs, BGAs, QFPs, MCM connectors, and cables.

While most textbooks emphasize theoretical derivation and mathematical rigor, this book emphasizes intuitive understanding, practical tools, and engineering discipline. We use the principles of electrical engineering and physics and apply them to the world of packaging and interconnects to establish a framework of understanding and a methodology of solving problems. The tools of time- and frequency-domain measurement, two- and three-dimensional field solvers, transmission-line simulations, circuit simulators, and analytical approximations are introduced to build verified equivalent circuit models for packages and interconnects.

There are two important questions that all designers should ask of any model they use: How accurate is it? And what is the bandwidth of the model? The answers to these questions can come only from measurements. Measurements play the very important role of risk reduction.

The three generic measurement instruments, the impedance analyzer, the vector-network analyzer (VNA) and the time-domain reflectometer (TDR) are introduced and the interpretation of their data explained. Examples of measurements from real interconnects such as IC packages, printed circuit boards, cables, and connectors are included throughout this book to illustrate the principles and, by example, the value of characterization tools.

This book has been designed for use by people of all levels of expertise and training: engineers, project managers, sales and marketing managers, technology developers, and scientists. We start out with an overview of why designing the

interconnects for high-speed digital systems is difficult and what major technical hurdles must be overcome to reach high-frequency operation.

We apply the tools of electrical engineering and physics to the problems of signal integrity in digital signals through the entire range of interconnects. The concept of equivalent circuit models is introduced to facilitate the quantified prediction of performance. The rest of the book describes how the circuit models of interconnects affect the electrical performance of the system in terms of the four families of noise problems: reflections, cross talk, rail collapse in the power distribution network, and EMI.

This book originated from a series of short courses and semester-long courses the author gave to packaging, circuit-board, and design engineers. It is oriented to all people who need to balance electrical performance with all other packaging and interconnect concerns in their system designs. This book provides the foundation to understand how the physical design world of geometries and material properties affects electrical performance.

If you remember nothing else about signal integrity, you should remember the following important general principles. These are summarized here and described in more detail throughout this book.

Top Ten Signal Integrity Principles

1. The key to efficient high-speed product design is to take advantage of analysis tools that enable accurate performance prediction. Use measurements as a way of validating the design process, reducing risk, and increasing confidence in the design tools.
2. The only way to separate myth from reality is to put in the numbers using rules of thumb, approximations, numerical simulation tools, or measurements. This is the essential element of engineering discipline.
3. Each interconnect is a transmission line with a signal and a return path, regardless of its length, shape, or signal rise time. A signal sees an instantaneous impedance at each step along its way down an interconnect. Signal quality is dramatically improved if the instantaneous impedance is constant, as in a transmission line with a uniform cross section.
4. Forget the word *ground*. More problems are created than solved by using this term. Every signal has a return path. Think *return path* and you will train

your intuition to look for and treat the return path as carefully as you treat the signal path.

5. Current flows through a capacitor whenever the voltage changes. For fast edges, even the air gap between the edge of a circuit board and a dangling wire can have a low impedance through the fringe field capacitance.
6. Inductance is fundamentally related to the number of rings of magnetic-field lines completely surrounding a current. If the number of rings of field lines ever changes, for whatever reason, a voltage will be created across the conductor. This is the origin of some reflection noise, cross talk, switching noise, ground bounce, rail collapse, and some EMI.
7. Ground bounce is the voltage created on the ground return conductor due to changing currents through the total inductance of the return path. It is the primary cause of switching noise and EMI.
8. The bandwidth of a signal is the highest sine-wave frequency component that is significant, compared to an equivalent frequency square wave. The bandwidth of a model is the highest sine-wave frequency at which the model still accurately predicts the actual performance of the interconnect. Never use a model in an application where the signal bandwidth is higher than the model's bandwidth.
9. Never forget, with few exceptions, every formula used in signal integrity is either a definition or an approximation. If accuracy is important, do not use an approximation.
10. The problem caused by lossy transmission lines is the rise-time degradation. The losses increase with frequency due to skin depth and dielectric losses. If the losses were constant with frequency, the rise time would not change and lossy lines would be only a minor inconvenience.
11. The most expensive rule is the one that delays the product ship.

A C K N O W L E D G M E N T S

Many colleagues, friends, and students contributed to my understanding that went into the content for both the first and second editions. Literally thousands of engineers from Intel, Cisco, Motorola, Altera, Qualcomm, Raytheon, and other companies who attended my classes provided feedback on what explanations worked and what didn't work.

In the second edition, my reviewers, Greg Edlund, Tim Swettlen, and Larry Smith, provided excellent feedback. I learned a lot from these experts.

My publisher, Bernard Goodwin, was always patient and encouraging, even when I missed deadlines, and never complained when my science fiction novel was completed ahead of this second edition.

Thank you all for the wonderful support and encouragement.

This page intentionally left blank

A B O U T T H E A U T H O R



Eric Bogatin received his B.S. in physics from MIT in 1976 and his M.S. and Ph.D. in physics from the University of Arizona in Tucson in 1980. For more than thirty years he has been active in the fields of signal integrity and interconnect design. He worked in senior engineering and management roles at AT&T Bell Labs, Raychem Corp., Sun Microsystems, and Interconnect Devices Inc.

Recognizing a need in the industry for quality technical training in signal integrity, he created Bogatin Enterprises, which has grown to be a world-leading provider of signal integrity training services. As a “Signal Integrity Evangelist,” Eric turns complexity into practical design principles, leveraging commercially available analysis techniques and measurement tools.

Over the years, he has created a number of live classes and presented to more than five thousand engineers, worldwide. These include topics on transmission lines, differential pairs, switching noise, ground bounce, the power distribution network, and EMI. Some courses cover the use of TDR and VNA measurement techniques to characterize interconnects.

In addition, Eric is a prolific author with more than three hundred publications, many posted on his web site, www.beTheSignal.com, for free download. He regularly presents at DesignCon, PCB West, Mentor User Group Meetings, and the IPC’s Designer Day annual event.

In the past ten years, he has written regular monthly columns for *Printed Circuit Design and Fabrication* magazine, Semiconductor International, Electronic Packaging and Production, Altera Corporation, and Mentor Graphics Corporation. He is on the editorial board of *Printed Circuit Design and Fabrication* magazine and *Micointerconnects Newsletter*.

While many engineers specialize in the electromagnetics aspects of signal integrity, Eric has equal experience in interconnect technologies. He has written four other books on packaging technologies and incorporates examples of the entire interconnect hierarchy in his materials, from on-chip, through packages, sockets, interposers, circuit boards, connectors, and cables.

In 2005, he recognized the increasing value of web-based, distance learning and created an online presence at www.beTheSignal.com. His was the first company to introduce a complete curriculum of web-based signal integrity content, including lectures, labs, and quizzes, available through a subscription plan for individuals or entire companies.

SIGNAL AND POWER INTEGRITY—

SIMPLIFIED

SECOND EDITION

In physical science the first essential step in the direction of learning any subject is to find principles of numerical reckoning and practicable methods for measuring some quality connected with it. I often say that when you can measure what you are speaking about, and express it in numbers, you know something about it; but when you cannot measure it, when you cannot express it in numbers, your knowledge is of a meagre and unsatisfactory kind; it may be the beginning of knowledge, but you have scarcely in your thoughts advanced to the state of Science, whatever the matter may be.

—Lord Kelvin (1824–1907)

This page intentionally left blank

Time and Frequency Domains

In this chapter, we explore the basic properties of signals in preparation for looking at how they interact with interconnects. We will find that there are multiple ways of looking at a signal, each providing a different perspective. The quickest path to the answer may not be the most obvious path. The different perspectives we will use to look at signals are called domains. In particular we'll use the time domain and the frequency domain.

We will find that while we may generally be more familiar with the time domain, the frequency domain can provide valuable insight to understand and master many signal-integrity effects such as impedance, lossy lines, the power-distribution network, measurements, and models.

After introducing the two domains, we will look at how to translate between the two for some special cases. We will apply what we learn to relate two important quantities: rise time and bandwidth. The first is a time-domain term and the second a frequency-domain term. However, as we will see, they are intimately related.

Finally, we'll apply this concept of bandwidth to interconnects, models, and measurements.

2.1 The Time Domain

We use the term a lot—the *time domain*. But what do we really mean? What is the time domain? What are the features that are special about the time domain that make it useful? These are surprisingly difficult questions to answer because they seem so obvious and we rarely think about what we really mean by the time domain.

TIP The time domain is the real world. It is the only domain that actually exists.

We take it for granted because from the moment we are born, our experiences are developed and calibrated in the time domain. We are used to seeing events happen with a time stamp and ordered sequentially.

The time domain is the world of our experiences and is the domain in which high-speed digital products perform. When evaluating the behavior of a digital product, we typically do the analysis in the time domain because that's where performance is ultimately measured.

For example, two important properties of a clock waveform are clock period and rise time. Figure 2-1 illustrates these features.

The clock period is the time interval to repeat one clock cycle, usually measured in nanoseconds (nsec). The clock frequency, F_{clock} , or how many cycles per second the clock goes through, is the inverse of the clock period, T_{clock} .

$$F_{\text{clock}} = \frac{1}{T_{\text{clock}}} \quad (2-1)$$

where:

F_{clock} = the clock frequency, in GHz

T_{clock} = the clock period, in nsec

For example, a clock with a period of 10 nsec will have a clock frequency of $1/10 \text{ nsec} = 0.1 \text{ GHz}$ or 100 MHz.

The rise time is related to how long it takes for the signal to transition from a low value to a high value. There are two popular definitions of rise time. The 10–90 rise time is how long it takes for the signal to transition from 10% of its final value to 90% of its final value. This is usually the default meaning of rise time. It can be read directly off the time domain plot of a waveform.

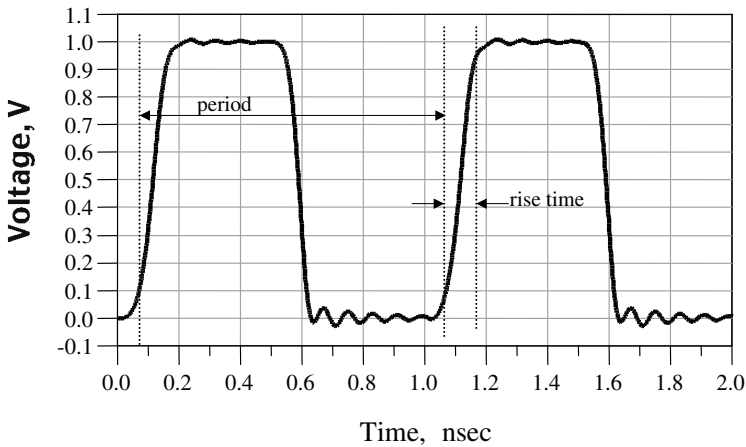


Figure 2-1 Typical clock waveform showing the clock period and the 10–90 rise time for a 1-GHz clock. The fall time is typically slightly shorter than the rise time and sometimes creates more noise.

The second definition is the 20–80 rise time. This is the time it takes for the signal to transition from 20% of its final value to 80% of its final value. Of course, for the same waveform the 20–80 rise time is shorter than the 10–90 rise time. Some IBIS models of real devices use the 20–80 definition of rise time. This makes it confusing. To remove ambiguity, it's often good practice referring explicitly to the 10–90 rise time or the 20–80 rise time.

There is a corresponding value for the fall time of a time-domain waveform. Depending on the logic family, the fall time is usually slightly shorter than the rise time. This is due to the design of typical CMOS output drivers. In a typical output driver, a p and an n transistor are in series between the V_{CC} (+) and the V_{SS} (–) power rails. The output is connected to the center, between them. Only one transistor is on at any one time, depending on whether the output is a low or a high.

When the driver switches from a low to a high (i.e., rising edge), the n transistor turns off and the p transistor turns on. The rise time is related to how fast the p transistor can turn on. When switching from the high to the low state (i.e., a falling edge), the p transistor turns off and the n transistor turns on. In general, for the same feature-size transistor, an n transistor can turn on faster than a p transistor. This means switching from high to low, the falling edge will be shorter than the rising edge. In general, signal-integrity problems are more likely to occur when switching from a high to low transition than from a low to high transition. By

making the n channel transistor larger than the p channel, the rising and falling edges can be closely matched.

Having established an awareness of the time domain as a distinct way of looking at events, we can turn our attention to one of a number of alternative ways of analyzing the world—the frequency domain.

2.2 Sine Waves in the Frequency Domain

We hear the term *frequency domain* quite a bit, especially when it involves radio frequency (rf) or communications systems. We will also encounter the frequency domain in high-speed digital applications. There are few engineers who have not heard of and used the term multiple times. Yet, what do we really mean by the frequency domain? What is the frequency domain and what makes it special and useful?

TIP The most important quality of the frequency domain is that it is not real. It is a mathematical construct. The only reality is the time domain. The frequency domain is a mathematical world where very specific rules are followed.

The most important rule in the frequency domain is that the only kind of waveforms that exist are sine waves. Sine waves are the language of the frequency domain.

There are other domains that use other special functions. For example, the JPEG picture-compression algorithm takes advantage of special waveforms that are called wavelets. The wavelet transform takes the space domain, with a lot of x-y amplitude information content, and translates it into a different mathematical description that is able to use less than 10% of the memory to describe the same information. It is an approximation, but a very good one.

It's common for engineers to think that we use sine waves in the frequency domain because we can build any time-domain waveform from combinations of sine waves. This is a very important property of sine waves. However, there are many other waveforms with this property. It is not a property that is unique to sine waves.

In fact, there are four properties that make sine waves very useful for describing any other waveform. These properties are as follows:

1. Any waveform in the time domain can be completely and uniquely described by combinations of sine wave.
2. Any two sine waves with different frequencies are orthogonal to each other. If you multiply them together and integrate over all time, they integrate to zero. This means you can separate each component from every other.
3. They are well defined mathematically.
4. They have a value everywhere with no infinities and they have derivatives that have no infinities anywhere. This means they can be used to describe real world waveforms, since there are no infinities in the real world.

All of these properties are vitally important, but are not unique to sine waves. There is a whole class of functions called *orthonormal functions*, or sometimes called *eigenfunctions* or *basis functions*, which could be used to describe any time-domain waveform. Other orthonormal functions are Hermite Polynomials, Legendre Polynomials, Laguerre Polynomials, and Bessel Functions.

Why did we choose sine waves as our functions in the frequency domain? What's so special about sine waves? The real answer is that by using sine waves, some problems related to the electrical effects of interconnects will be easier to understand and solve using sine waves. If we switch to the frequency domain and use sine-wave descriptions, we can sometimes get to an answer faster than staying in the time domain.

TIP After all, if the time domain is the real world, we would never leave it unless the frequency domain provides a faster route to an acceptable answer.

Sine waves can sometimes provide a faster path to an acceptable answer because of the types of electrical problems we often encounter in signal integrity. If we look at the circuits that describe interconnects, we find that they will often include combinations of resistors (R), inductors (L), and capacitors (C). These elements in a circuit can be described by a second-order linear differential equation. The solution to this type of differential equation is a sine wave. In these circuits, the naturally occurring waveforms will be combinations of the waveforms that are solutions to the differential equation.

We find that in the real world, if we build circuits that contain Rs, Ls, and Cs and send any arbitrary waveform in, more often than not, we get waveforms out that look like sine waves and can more simply be described by a combination of a few sine waves. An example of this is shown in Figure 2-2.

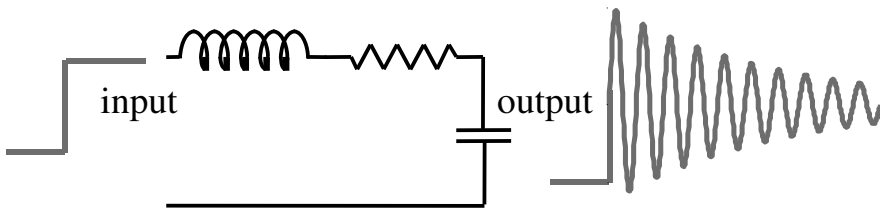


Figure 2-2 Time-domain behavior of a fast edge interacting with an ideal RLC circuit. Sine waves are naturally occurring when digital signals interact with interconnects, which can often be described as combinations of ideal RLC circuit elements.

2.3 Shorter Time to a Solution in the Frequency Domain

TIP The only reason we would ever want to move to another domain is to get to an acceptable answer faster.

In some situations, if we use the naturally occurring sine waves in the frequency domain rather than in the time domain, we may arrive at a simpler description to a problem and get to a solution faster.

It is important to keep in mind that there is fundamentally no new information in the frequency domain. The time- and the frequency-domain descriptions of the same waveforms will each have exactly the same information content.

However, some problems are easier to understand and describe in the frequency domain than in the time domain. For example, the concept of bandwidth is intrinsically a frequency-domain idea. We use this term to describe the most significant sine-wave frequency components associated with a signal, a measurement, a model, or an interconnect.

Impedance is defined in both the time and the frequency domain. However, it is far easier to understand, to use, and to apply the concepts of impedance in the frequency domain. We need to understand impedance in both domains, but we will often get to an answer faster by solving an impedance problem in the frequency domain first.

Looking at the impedance of the power and ground distribution in the frequency domain will allow a simpler explanation and solution to rail-collapse problems. As we shall see, the design goal for the power-distribution system is to keep its impedance below a target value from direct current (DC) up to the bandwidth of the typical signals.

When dealing with EMI issues, both the FCC specifications and the methods of measuring the electromagnetic compliance of a product are more easily performed in the frequency domain.

With today's current capabilities of hardware and software tools, the quality of the measurements and the computation speed of the numerical-simulation tools can sometimes be better in the frequency domain.

A high signal-to-noise ratio (SNR) means higher quality measurements. The SNR of a vector-network analyzer (VNA), which operates in the frequency domain, is constant over its entire frequency range, which can be -130 dB from 10 MHz up to 50 GHz and more. For a time-domain reflectometer (TDR), the effective bandwidth may be as high as 20 GHz, but the SNR starts at -70 dB at low frequency and drops to as low as -30 dB at 20 GHz.

Many of the effects related to lossy transmission lines are more easily analyzed, measured, and simulated by using the frequency domain. The series resistance of a transmission line increases with the square root of frequency, and the shunt AC leakage current in the dielectric increases linearly with frequency. The transient (time-domain) performance of lossy transmission lines is often more easily obtained by first transforming the signal into the frequency domain, looking at how the transmission line affects each frequency component separately, and then transforming the sine-wave components back to the time domain.

2.4 Sine Wave Features

As we now know, by definition, the only waveforms that exist in the frequency domain are sine waves. We should also be familiar with the description of a sine wave in the time domain. It is a well-defined mathematical curve that has three terms that fully characterize absolutely everything you could ever ask about it. An example is shown in Figure 2-3.

The following three terms fully describe a sine wave:

- Frequency
- Amplitude
- Phase

The frequency, usually identified using a small f , is the number of complete cycles per second made by the sine wave, in Hertz. Angular frequency is measured in radians per second. A radian is like degrees, describing a fraction of a cycle. There are $2 \times \pi$ radians in one complete cycle. The Greek letter ω is often

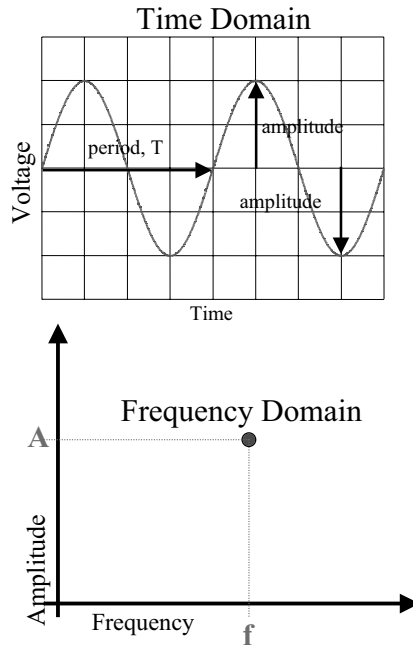


Figure 2-3 Top: Description of a sine wave in the time domain. It is composed of over one thousand voltage-versus-time data points. Bottom: Description of a sine wave in the frequency domain. Only three terms define a sine wave, which is a single point in the frequency domain.

used to refer to the angular frequency, measured in radians per second. The sine-wave frequency and the angular frequency are related by:

$$\omega = 2\pi \times f \quad (2-2)$$

where:

ω = angular frequency, in radians/sec

π = constant, 3.14159...

f = sine-wave frequency, in Hz

For example, if the frequency of a sine wave is 100 MHz, the angular frequency is $2 \times 3.14159 \times 100 \text{ MHz} \sim 6.3 \times 10^8$ radians/sec.

The amplitude is the maximum value of the peak height above the center value. The wave peak goes below the horizontal just as much as it goes above.

The phase is more complicated and identifies where the wave is in its cycle at the beginning of the time axis. The units of phase are in cycles, radians, or degrees, with 360 degrees in one cycle. While phase is important in mathematical analysis, we will minimize the use of phase in most of our discussion to concentrate on the more important aspects of sine waves.

In the time domain, describing a sine wave requires plotting a lot of voltage-versus-time data points to draw the complete sine-wave curve. However, in the frequency domain, describing a sine wave is much simpler.

In the frequency domain, we already know that the only waveforms we can talk about are sine waves, so all we have to identify are the amplitude, frequency, and phase. If there is only one sine wave we are describing, all we need are these three values and we have identified a complete description of the sine wave.

Since we are going to ignore phase for right now, we really only need two terms to completely describe a sine wave: its amplitude and its frequency. These two values are plotted with the frequency as one axis and the amplitude as the other axis, as shown in Figure 2-3. Of course, if we were including phase, we'd have a third axis. A sine wave, plotted in the frequency domain, is just one single data point. This is the key reason why we will go into the frequency domain. What might have been a thousand voltage-versus-time data points in the time domain is converted to a single amplitude-versus-frequency data point in the frequency domain.

When we have multiple frequency values, the collection of amplitudes is called the spectrum. As we will see, every time-domain waveform has a particular pattern to its spectrum. The only way to calculate the spectrum of a waveform in the time domain is with the Fourier Transform.

2.5 The Fourier Transform

The starting place for using the frequency domain is being able to convert a waveform from the time domain into a waveform in the frequency domain. We do this with the Fourier Transform. There are three types of Fourier Transforms:

- Fourier Integral (FI)
- Discrete Fourier Transform (DFT)
- Fast Fourier Transform (FFT)

The Fourier Integral (FI) is a mathematical technique of transforming an ideal mathematical expression in the time domain into a description in the frequency domain. For example, if the entire waveform in the time domain were just a short pulse, and nothing else, the Fourier Integral would be used to transform to the frequency domain.

This is done with an integral over all time from $-\infty$ to $+\infty$. The result is a frequency-domain function that is also continuous from 0 to $+\infty$ frequencies. There is a value for the amplitude at every continuous frequency value in this range.

For real-world waveforms, the time-domain waveform is actually composed of a series of discrete points, measured over a finite time, T . For example, a clock waveform may be a signal from 0 v to 1 v and have a period of 1 nsec and a repeat frequency of 1 GHz. To represent one cycle of the clock, there might be as many as 1000 discrete data points, taken at 1-psec intervals. An example of a 1-GHz clock wave in the time domain is shown in Figure 2-4.

To transform this waveform into the frequency domain, the Discrete Fourier Transform (DFT) would be used. The basic assumption is that the original time-domain waveform is periodic and repeats every T seconds. Rather than integrals, just summations are used so any arbitrary set of data can be converted to the frequency domain using simple numerical techniques.

Finally, there is the Fast Fourier Transform (FFT). It is exactly the same as a DFT, except that the actual algorithm used to calculate the amplitude values at each frequency point uses a trick of very fast matrix algebra. This trick works only if the number of time-domain data points is a power of two, for example 256 points, or 512 points, or 1024 points. The result is a DFT, only calculated 100–10,000 times faster than the general DFT algorithm, depending on the number of voltage points.

In general, it is common in the industry to use all three terms, FI, DFT, and FFT, synonymously. We now know there is a difference between them, but they have the same purpose—to translate a time-domain waveform into its frequency-domain spectrum.

TIP Once in the frequency domain, the description of a waveform is a collection of sine-wave frequency values. Each frequency component has an amplitude and phase associated with it. We call the entire set of frequency values and their amplitudes the spectrum of the waveform.

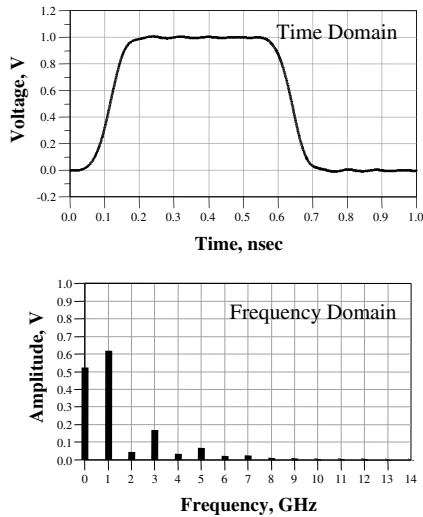


Figure 2-4 One cycle of a 1-GHz clock signal in the time domain (top) and frequency domain (bottom).

An example of a simple time-domain waveform and its associated spectrum, calculated by using a DFT, is shown in Figure 2-4.

At least once in his or her life, every serious engineer should calculate a Fourier Integral by hand, just to see the details. After this, we never again need to do the calculation manually. We can always get to an answer faster by using one of the many commercially available software tools that calculate Fourier Transforms for us.

There are a number of relatively easy-to-use, commercially available software tools that calculate the DFT or FFT of any waveform entered. Every version of SPICE has a function called the `.FOUR` command that will generate the amplitude of the first nine frequency components for any waveform. Most versions of the more advanced SPICE tools will also compute the complete set of amplitude and frequency values using a DFT. Microsoft Excel has an FFT function, usually found in the “engineering add-ins.”

2.6 The Spectrum of a Repetitive Signal

In practice, the DFT or FFT is used to translate a real waveform from the time domain to the frequency domain. It is possible to take a DFT of any arbitrary, measured waveform. A key requirement of the waveform is that it be repetitive. We usually designate the repeat frequency of the time-domain waveform with the capital letter F .

For example, an ideal square wave might go from 0 v to 1 v, with a repeat time of 1 nsec and a 50% duty cycle. As an ideal square wave, the rise time to transition from 0 v to 1 v is precisely 0 sec. The repeat frequency would be $1/1 \text{ nsec} = 1 \text{ GHz}$.

If a signal in the time domain is some arbitrary waveform over a time interval from $t = 0$ to $t = T$, it may not look repetitive. However, it can be turned into a repetitive signal by just repeating the interval every T seconds. In this case, the repeat frequency would be $F = 1/T$. Any arbitrary waveform can be made repetitive and the DFT used to convert it to the frequency domain. This is illustrated in Figure 2-5.

For a DFT, only certain frequency values exist in the spectrum. These values are determined by the choice of the time interval or the repeat frequency. When using an automated DFT tool, such as in SPICE, it is recommended to choose a value for the period equal to the clock period. This will simplify the interpretation of the results.

The only sine-wave frequency values that will exist in the spectrum will be multiples of the repeat frequency. If the clock frequency is 1 GHz, for example, the DFT will only have sine wave components at 1 GHz, 2 GHz, 3 GHz, etc.

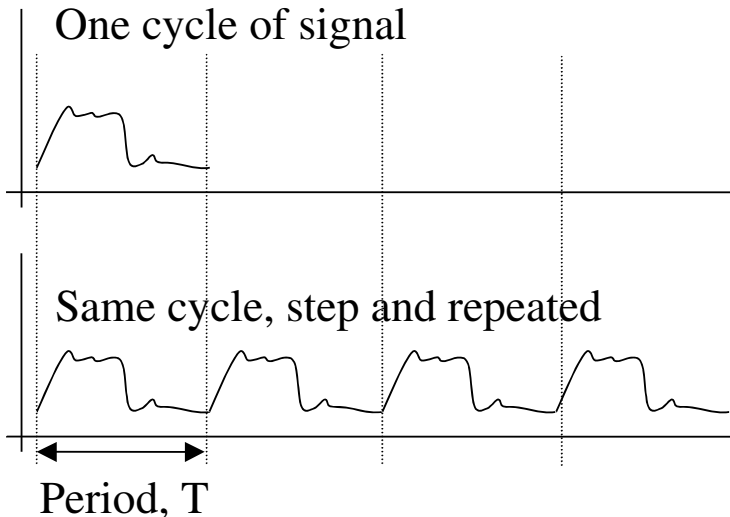


Figure 2-5 Any arbitrary waveform can be made to look repetitive. A DFT can be performed only on a repetitive waveform.

The first sine-wave frequency is called the first harmonic. The second sine-wave frequency is called the second harmonic, and so on. Each harmonic will have a different amplitude and phase associated with it. The collection of all the harmonics and their amplitudes is called the spectrum.

The actual amplitudes of each harmonic will be determined by the values calculated by the DFT. Every specific waveform will have its own spectrum.

2.7 The Spectrum of an Ideal Square Wave

An ideal square wave has a zero rise time, by definition. It is not a real waveform; it is an approximation to the real world. However, useful insight can be gained by looking at the spectrum of an ideal square wave and using this to evaluate real waveforms later. An ideal square wave has a 50% duty cycle, is symmetrical, and has a peak voltage of 1 v. This is illustrated in Figure 2-6.

If the ideal square-wave repeat frequency is 1 GHz, the sine-wave frequency values in its spectrum will be multiples of 1 GHz. We expect to see components at $f = 1 \text{ GHz}$, 2 GHz , 3 GHz , and so on. But what are the amplitudes of each sine wave? The only way to determine this is to perform a DFT on the ideal square wave. Luckily, it is possible to calculate the DFT exactly for this special case of an ideal square wave. The result is relatively simple.

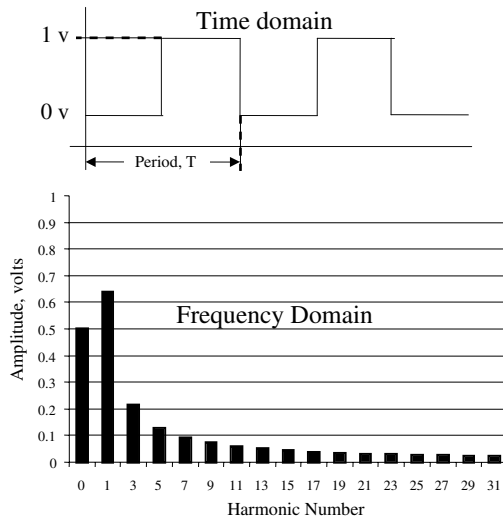


Figure 2-6 Time and frequency domain views of an ideal square wave.

The amplitudes of all the even harmonics (e.g., 2 GHz, 4 GHz, 6 GHz) are all zero. It is only odd harmonics that have values. The amplitudes, A_n , of the odd harmonics are given by:

$$A_n = \frac{2}{\pi \times n} \quad (2-3)$$

where:

A_n = the amplitude of the n^{th} harmonic

π = the constant, 3.14159...

n = the harmonic number, only odd allowed

For example, an ideal square wave with 50% duty-cycle and 0 v to 1 v transition has a first harmonic amplitude of 0.63 v. The amplitude of the third harmonic is 0.21 v. We can even calculate the amplitude of the 1001st harmonic. It is 0.00063 v. It is important to note that the amplitudes of higher sine-wave-frequency components decrease with $1/f$.

If the transition-voltage range of the ideal square wave were to double to 0 v to 2 v, the amplitudes of each harmonic would double as well.

There is one other special frequency value, 0 Hz. Since sine waves are all centered about zero, any combination of sine waves can only describe waveforms in the time domain that are centered about zero. To allow a DC offset, or a nonzero average value, the DC component is stored in the zero-frequency value. This is sometimes called the zeroth harmonic. Its amplitude is equal to the average value of the signal. In the case of the 50% duty-cycle square wave, the zeroth harmonic is 0.5 v.

To summarize:

- The collection of sine-wave-frequency components and their amplitudes is called the spectrum. Each component is called a harmonic.
- The zeroth harmonic is the DC value.
- For the special case of a 50% duty-cycle ideal square wave, the even harmonics have an amplitude of zero.
- The amplitude of any harmonic can be calculated as $2/(\pi \times n)$.

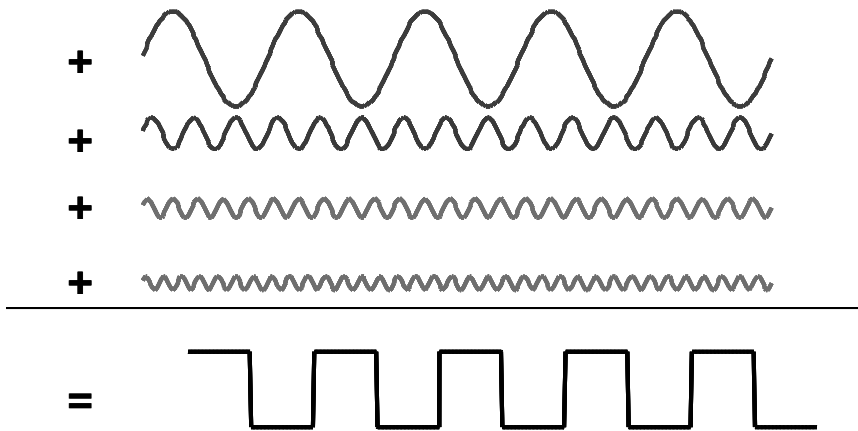


Figure 2-7 Convert the frequency-domain spectrum into the time-domain waveform by adding up each sine-wave component.

2.8 From the Frequency Domain to the Time Domain

The spectrum, in the frequency domain, represents all the sine-wave-frequency amplitudes of the time-domain waveform. If we have a spectrum and want to look at the time-domain waveform, we simply take each frequency component, convert it into its time-domain sine wave, then add it to all the rest. This process is called the Inverse Fourier Transform. It is illustrated in Figure 2-7.

Each component in the frequency domain is a sine wave in the time domain, defined from $t = -\infty$ to $t = +\infty$. To re-create the time-domain waveform, we take each of the sine waves described in the spectrum and add them up in the time domain at each time-interval point. We start at the low-frequency end and add each harmonic based on the spectrum.

For a 1-GHz ideal-square-wave spectrum, the first term in the frequency domain is the zeroth harmonic, with amplitude of 0.5 v. This component describes a constant DC value in the time domain.

The next component is the first harmonic, which is a sine wave in the time domain with a frequency of 1 GHz and an amplitude of 0.63 v. When this is added to the previous term, the result in the time domain is a sine wave, offset to 0.5 v. It is not a very good approximation to the ideal square wave. This is shown in Figure 2-8.

The next term is the third harmonic. The amplitude of the 3-GHz sine-wave-frequency component is 0.21 v. When we add this to the existing time-domain

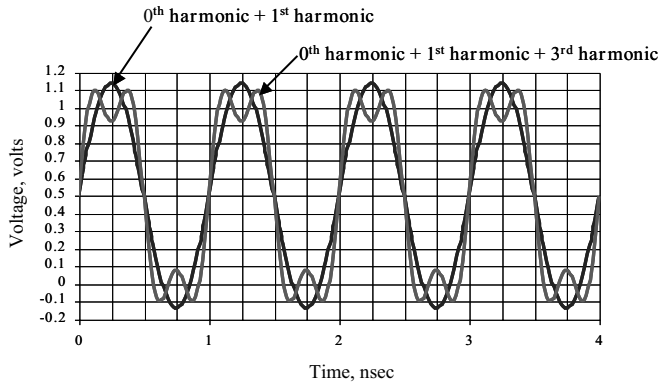


Figure 2-8 The time-domain waveform is created by adding together the zeroth harmonic and first harmonic and then the third harmonic, for a 1-GHz ideal square wave.

waveform, we see that it changes the shape of the new waveform slightly. The top is a bit more flat, better approximating a square wave, and the rise time is a little sharper. As we go through this process, adding each successive higher harmonic to re-create the ideal square wave, the resulting waveform begins to look more and more like a square wave. In particular, the rise time of the resulting time-domain waveform changes as we add higher harmonics.

To illustrate this in more detail, we can zoom in on the rise time of the waveform, centered about the beginning of a cycle. As we add all the harmonics up to the seventh harmonic, and then all the way up to the nineteenth, and finally, all the way up to the thirty-first harmonic, we see that the rise time of the resulting waveform in the time domain continually gets shorter. This is shown in Figure 2-9.

Depending on how the DFT was set up, there could be over 100 different harmonics listed in the spectrum. The logical question to ask is, do we have to include all of them, or can we still re-create a “good enough” representation of the original time-domain waveform with just a limited number of harmonics? What really is the impact of limiting the highest harmonic included in the re-created time-domain waveform? Is there a highest sine-wave-frequency component at which we can stop?

2.9 Effect of Bandwidth on Rise Time

The term *bandwidth* is used for the highest sine-wave-frequency component that is significant in the spectrum. This is the highest sine-wave frequency we need to include to adequately approximate the important features of the time-domain

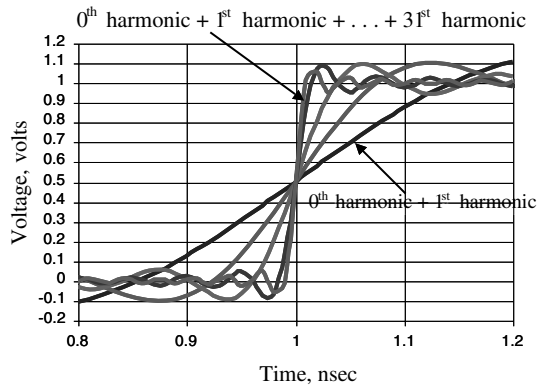


Figure 2-9 The time domain waveform created by adding together the zeroth harmonic and first harmonic, then the third harmonic and then up to the seventh harmonic, then up to the nineteenth harmonic, and then all harmonics up to the thirty-first harmonic, for a 1-GHz ideal square wave.

waveform. All frequency components of higher frequency than the bandwidth can be ignored. In particular, as we will see, the bandwidth we choose will have a direct effect on the shortest rise time of the signal we are able to describe in the time domain.

The term *bandwidth* historically is used in the rf world to refer to the range of frequencies in a signal. In rf applications, a carrier frequency is typically modulated with some amplitude or phase pattern. The spectrum of frequency components in the signal falls within a band. The range of frequencies in the rf signal is called the bandwidth. Typical rf signals might have a carrier frequency of 1.8 GHz with a bandwidth about this frequency of 100 MHz. The bandwidth of an rf signal defines how dense different communications channels can fit.

With digital signals, bandwidth also refers to the range of frequencies in the signal's spectrum. It's just that for digital signals, the low frequency range starts at DC and extends to the highest frequency component. In the world of digital signals, since the lowest frequency will always be DC, bandwidth will always be a measure of the highest sine wave frequency component that is significant.

When we created a time-domain waveform from just the zeroth, the first, and the third harmonics included, as in Figure 2-8, the bandwidth of the resulting waveform was just up to the third harmonic, or 3 GHz in this case. By design, the highest sine-wave-frequency component in this waveform is 3 GHz. The amplitude of all other sine-wave components in this time-domain waveform is exactly 0.

When we added higher harmonics to create the waveforms in Figure 2-9, we designed their bandwidths to be 7 GHz, 19 GHz, and 31 GHz. If we were to take the shortest rise-time waveform in Figure 2-9 and transform it back into the frequency domain, its spectrum would look exactly like that shown in Figure 2-6. It would have components from the zeroth to the thirty-first harmonics. Beyond the thirty-first harmonic, all the components would be zero. The highest sine-wave-frequency component that is significant in this waveform is the thirty-first harmonic, or the waveform has a bandwidth of 31 GHz.

In each case, we created a waveform with a higher bandwidth, using the ideal-square-wave's spectrum as the starting place. And, in each case, the higher-bandwidth waveform also had a shorter 10–90 rise time. The higher the bandwidth, the shorter the rise time and the more closely the waveform approximates an ideal square wave. Likewise, if we do something to a short rise-time signal to decrease its bandwidth (i.e., eliminate high-frequency components), its rise time will increase.

For example, it is initially difficult to evaluate the time-domain response of a signal propagating down a lossy transmission line in FR4. As we will see, there are two loss mechanisms: conductor loss and dielectric loss. If each of these processes were to attenuate low-frequency components the same as they do high-frequency components, there would simply be less signal at the far end, but the pattern of the spectrum would look the same coming out as it does going in. There would be no impact on the rise time of the waveform.

However, both conductor loss and dielectric loss will attenuate the higher-frequency components more than the low-frequency components. By the time the signal has traveled through even four inches of trace, the high-frequency components, above about 8 GHz, can have lost more than 50% of their power, leaving the low-frequency terms less affected. In Figure 2-10 (top), we show the measured attenuation of sine-wave-frequency components through a four-inch length of transmission line in FR4. This transmission line happens to have a 50-Ohm characteristic impedance and was measured with a network analyzer. Frequency components below 2 GHz are not attenuated more than -1 dB, while components at 10 GHz are attenuated by -4 dB.

This preferential attenuation of higher frequencies has the impact of decreasing the bandwidth of a signal that would propagate through the interconnect. Figure 2-10 (bottom) is an example of the measured rise time of a 50-psec signal entering a 36-inch-long trace in FR4 and this same waveform when it exits the trace. The rise time has been increased from 50 psec to nearly 1.5 nsec, due to the higher attenuation of the high-frequency components. Thirty-six inches is a typi-

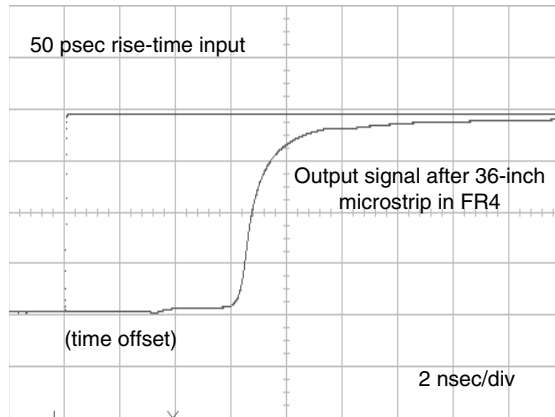
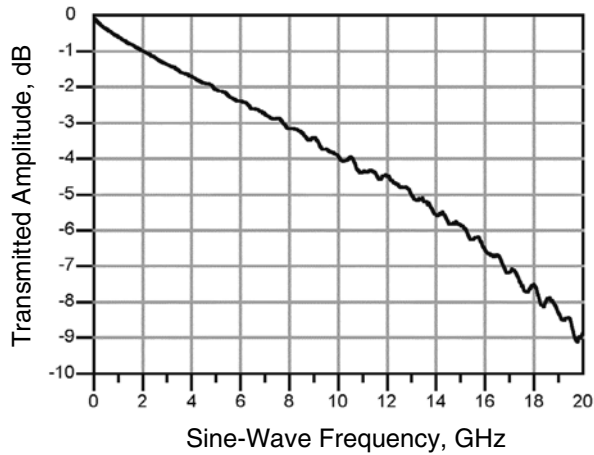


Figure 2-10 Top: The measured attenuation through a 4-inch length of 50-Ohm transmission line in FR4 showing the higher attenuation at higher frequencies. Bottom: The measured input and transmitted signal through a 36-inch 50-Ohm transmission line in FR4, showing the rise time to have degraded from 50 psec to more than 1.5 nsec.

cal length for a trace that travels over two 6-inch-long daughter cards and 24 inches of backplane. This rise-time degradation is the chief limitation to the use of FR4 laminate in high-speed serial links above 1 GHz.

TIP In general, a shorter rise-time waveform in the time domain will have a higher bandwidth in the frequency domain. If something is done to the spectrum to decrease the bandwidth of a waveform, the rise time of the waveform will be increased.

The connection between the highest sine-wave-frequency component that is significant in a spectrum and the corresponding rise time of the waveform in the time domain is a very important property.

2.10 Bandwidth and Rise Time

The relationship between rise time and bandwidth for a re-created ideal square wave can be quantified. In each synthesized waveform in the previous example re-creating an ideal square wave, the bandwidth is explicitly known because each waveform was artificially created by including sine-wave-frequency components only up to a specified value. The rise time, defined as the time from the 10% point to the 90% point, can be measured from time-domain plots.

When we plot the measured 10–90 rise time and the known bandwidth for each waveform, we see that empirically there is a simple relationship. This is a fundamental relationship for all signals and is shown in Figure 2-11.

For the special case of a re-created square wave with only some of the higher harmonics included, the bandwidth is inversely related to the rise time. We can fit a straight-line approximation through the points and find the relationship between bandwidth and rise time as:

$$BW = \frac{0.35}{RT} \quad (2-4)$$

where:

BW = the bandwidth, in GHz

RT = the 10–90 rise time, in nsec

For example, if the rise time of a signal is 1 nsec, the bandwidth is about 0.35 GHz or 350 MHz. Likewise, if the bandwidth of a signal is 3 GHz, the rise time of the signal will be about 0.1 nsec. A signal with a rise time of 0.25 nsec, such as might be seen in a DDR3-based system, has a bandwidth of $0.35/0.25 \text{ nsec} = 1.4 \text{ GHz}$.

There are other ways of deriving this relationship for other waveforms, such as with Gaussian or exponential edges. The approach we took here for square waves is purely empirical and makes no assumptions. It is one of the most useful rules of thumb in our toolbox.

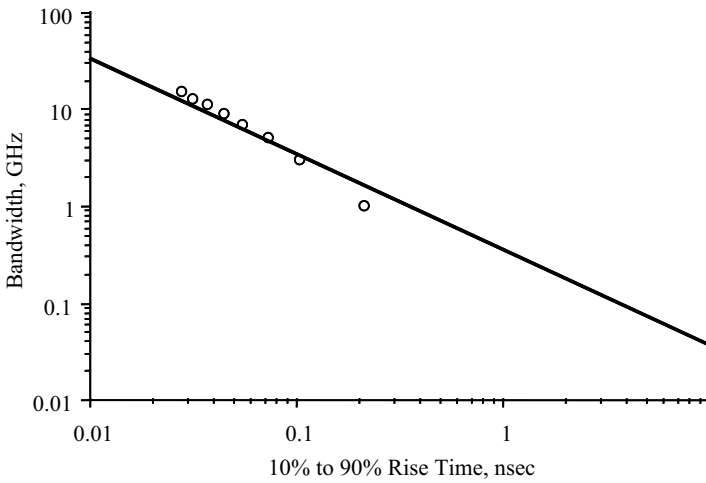


Figure 2-11 Empirical relationship between the bandwidth of a signal and its 10–90 rise time, as measured from a re-created ideal square wave with each harmonic added one at a time. Circles are the values extracted from the data; line is the approximation of $BW = 0.35/\text{rise time}$.

It is important to keep the units straight. When rise time is in microseconds, the bandwidth is in MHz. For example, a very long rise time of 10 microseconds has a bandwidth of about $0.35/10 \text{ microsec} = 0.035 \text{ MHz}$. This is equivalent to 35 kHz.

When the rise time is in nanoseconds, the bandwidth is in GHz. A 10-nsec rise time, typical of a 10-MHz clock frequency, has a bandwidth of about $0.35/10 \text{ nsec} = 0.035 \text{ GHz}$ or 35 MHz.

2.11 What Does *Significant* Mean?

We defined the bandwidth of a signal as the highest sine-wave-frequency component that is significant. In the example, where we started with an ideal square wave and limited the high-frequency components, there was absolutely no ambiguity about what *significant* meant. We explicitly cut off all higher frequency sine-wave components in the frequency domain so that the highest significant component was the last harmonic in the spectrum.

We simply showed that if we include 100% of all the frequency components of an ideal square wave, up to the bandwidth, we would be able to re-create a square wave with a limited rise time, where the relationship of $\text{rise time} = 0.35/\text{BW}$. But what is the impact from adding only a fraction of the next component?

For example, if we take an ideal-square-wave clock signal with clock frequency of 1 GHz, its first harmonic will be a 1-GHz sine-wave frequency. If we were to include 100% of every component up to the twenty-first harmonic, the bandwidth would be 21 GHz and the resulting rise time of the re-created signal would be $0.35/21 \text{ GHz} = 0.0167 \text{ nsec}$ or 16.7 psec.

How would the rise time change if we added the twenty-third harmonic? The rise time would be $0.35/23 \text{ GHz} = 0.0152 \text{ nsec}$ or 15.2 psec. The rise time dropped by 1.5 psec. This is about 10% of the rise time, which is consistent, because we increased the bandwidth by 10%. The magnitude of the component we added was just 0.028 v, compared with the first harmonic of 0.63 v. Even though this amplitude is a small amount, less than 5% of the first harmonic amplitude and less than 3% of the peak value of the original square wave, it had the impact of dropping the rise time by 10%.

The spectrum of an ideal square wave has components that extend to infinite frequency. In order to achieve the zero rise time of an ideal square wave, each of these components is needed and is significant.

For a real time-domain waveform, the spectral components will almost always drop off in frequency faster than those of an ideal square wave of the same repeat frequency. The question of significance is really about the frequency at which amplitudes of the higher harmonics become small compared to the corresponding amplitudes of an ideal square wave.

By “small,” we usually mean when the power in the component is less than 50% of the power in an ideal square wave’s amplitude. A drop of 50% in power is the same as a drop to 70% in amplitude. This is really the definition of significant. Significant is when the amplitude is still above 70% of an ideal square wave’s amplitude of the same harmonic.

TIP For any real waveform that has a finite rise time, *significant* refers to the point at which its harmonics are still more than 70% of the amplitude of an equivalent repeat-frequency ideal square wave’s.

In a slightly different view, we can define *significant* as the frequency at which the harmonic components of the real waveform begin to drop off faster than $1/f$. The frequency at which this happens is sometimes referred to as the *knee frequency*. The harmonic amplitudes of an ideal square wave will initially drop off similarly as $1/f$. The frequency at which the harmonic amplitudes of a real waveform begin to significantly deviate from an ideal square wave is the knee frequency.

To evaluate the bandwidth of a time-domain waveform, we are really asking what is the highest frequency component that is just barely above 70% of the same harmonic of an equivalent ideal square wave. When the harmonic amplitudes of the real waveform are significantly less than an ideal square wave's, these lower amplitude harmonics will not contribute significantly to decreasing the rise time and we can ignore them.

For example, we can compare, in the time-domain waveform, two clock waves with a repeat frequency of 1 GHz: an ideal square wave and an ideal trapezoidal waveform, which is a non-ideal square wave with a long rise time. In this example, the 10–90 rise time is about 0.08 nsec, which is a rise time of about 8% of the period, typical of many clock waveforms. These two waveforms are shown in Figure 2-12.

If we compare the frequency components of these waveforms, at what frequency will the trapezoid's spectrum start to differ significantly from the ideal square wave's? We would expect the trapezoid's higher frequency components to begin to become insignificant at about $0.35/0.08$ nsec = about 5 GHz. This is the fifth harmonic. After all, we could create a non-ideal square wave with this rise time if we were to take the ideal-square-wave spectrum and drop all components above the fifth harmonic, as we saw earlier.

When we look at the actual spectrum of the trapezoid compared to the square wave, we see that the first and third harmonics are about the same for each. The trapezoid's fifth harmonic is about 70% of the square wave's, which is still a large fraction. However, the trapezoid's seventh harmonic is only about 30% of the ideal square wave's. This is illustrated in Figure 2-12.

We would conclude, by simply looking at the spectra of the trapezoid, that harmonics above the fifth harmonic (i.e., the seventh and beyond) are contributing only a very small fraction of the amount of voltage as in the ideal square wave. Thus, their ability to further affect the rise time is going to be minimal. From the spectrum, we would say that the highest sine-wave-frequency component that is significant in the trapezoid, *compared to that in the ideal square wave*, is the fifth harmonic, which is what our approximation gave us.

There are higher harmonics in the trapezoid's spectrum than the fifth harmonic. However, the largest amplitude is 30% of the square wave's and then only a few percent after this. Their magnitude is such a small fraction of the amplitude of the ideal square wave's that they will contribute very little to the decrease of the rise time and can be ignored.

The bandwidth of any waveform is always the highest sine-wave-frequency component in its spectrum that is comparable in magnitude to a corresponding ideal

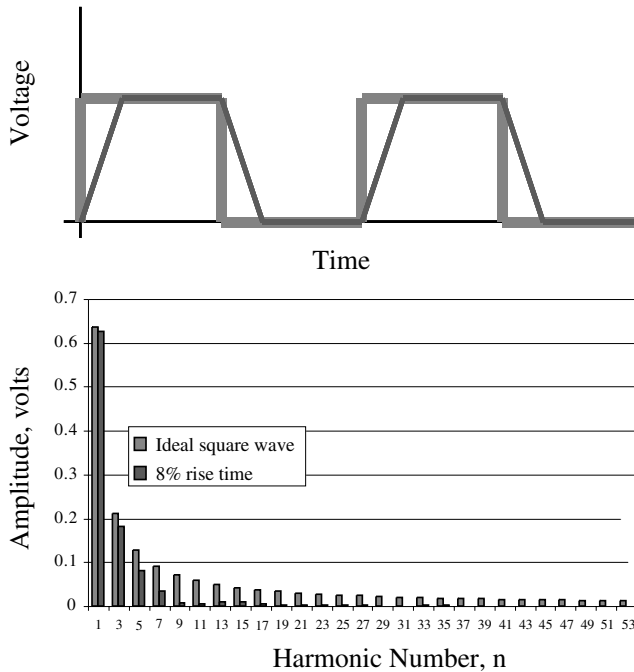


Figure 2-12 Top: Time domain waveforms of 1-GHz repeat frequency: an ideal square wave and an ideal trapezoidal wave with 0.08-nsec rise time. Bottom: Frequency-domain spectra of these waveforms showing the drop-off of the trapezoidal wave's higher harmonics, compared to the square wave's.

square wave. We can find out the bandwidth of any waveform by using a DFT to calculate its spectrum and compare it to an ideal square wave. We identify the frequency component of the waveform that is less than 70% of the ideal square wave, or we can use the rule of thumb developed earlier, that the BW is $0.35/\text{rise time}$.

TIP It is important to note that this concept of bandwidth is inherently an approximation. It is really a rule of thumb, identifying roughly where the amplitude of frequency components in a real waveform begin to drop off faster than in an ideal square wave.

If you have a problem where it is important to know whether the bandwidth of a waveform is 900 MHz or 950 MHz, you should not use this term *bandwidth*. Rather, you should use the whole spectrum. The entire spectrum is always an accurate representation of the time-domain waveform.

2.12 Bandwidth of Real Signals

Other than the approximation for the bandwidth of a waveform based on its rise time, there is little calculation we can do by hand. Fourier Transforms of arbitrary waveforms can only be done using numerical simulation.

For example, the spectrum of a good-quality, nearly square wave signal has a simple behavior. If a transmission line circuit is poorly terminated, the signal may develop ringing. The resulting spectrum will have peaks at the ringing frequency. The amplitudes of the ringing frequency can be more than a factor of 10 greater than the amplitudes of the signal without ringing. This is shown in Figure 2-13.

The bandwidth of a waveform with ringing is clearly higher than one without. When ringing is present in a waveform, the bandwidth is better approximated

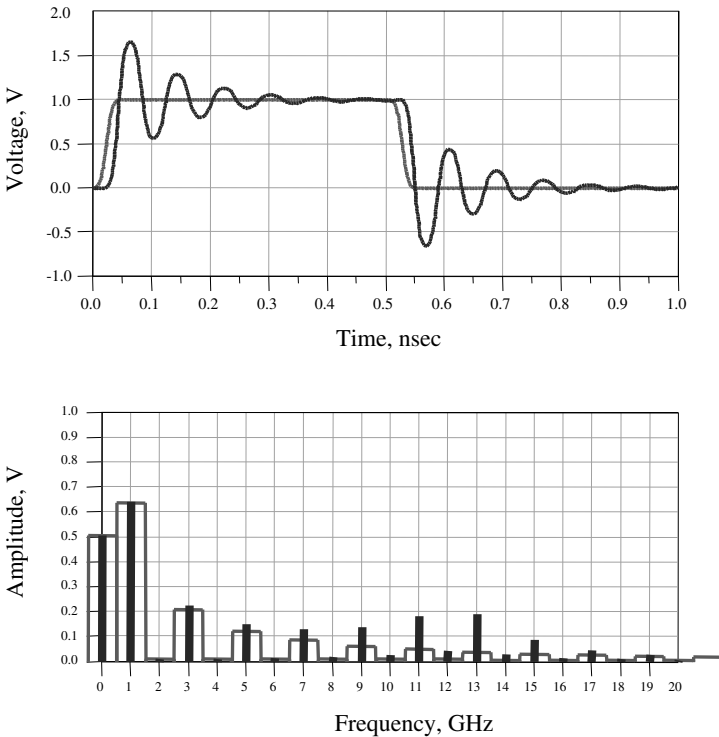


Figure 2-13 Top: The time-domain waveform of a near-square wave and one that has significant ringing due to poor termination. Bottom: the resulting DFT spectrum of these two waves, showing the effect of the ringing on the spectrum. The wide bars are for the ideal waveform while the narrow bars are for the ringing waveform.

by the ringing frequency. Just using the bandwidth to characterize a ringing signal, though, may be misleading. Rather, the whole spectrum needs to be considered.

EMI arises from each frequency component of the currents radiating. For the worst offender, the common currents, the amount of radiated emissions will increase linearly with the frequency. This means that if the current had an ideal-square-wave behavior, though the amplitude of each harmonic drops off at a rate of $1/f$, the ability to radiate would increase at the rate of f , so all harmonics contribute equally to EMI. To minimize EMI, the design goal is to use the absolute lowest bandwidth possible in all signals. Above the bandwidth, the harmonic amplitudes drop off faster than $1/f$, and would contribute to less radiated emissions. By keeping the bandwidth low, the radiated emissions will be kept to a minimum.

Any ringing in the circuits may increase the amplitudes of higher-frequency components and increase the magnitude of radiated emissions by a factor of 10. This is one reason why solving all signal-integrity problems is usually a starting place to minimize EMI problems.

2.13 Bandwidth and Clock Frequency

As we have seen, bandwidth relates to the rise time of a signal. It is possible to have two different waveforms, with exactly the same clock frequency but different rise times and different bandwidths. Just knowing the clock frequency cannot tell us what the bandwidth is. Figure 2-14 shows four different waveforms, each with exactly the same clock frequency of 1 GHz. However, they have different rise times and hence different bandwidths.

Sometimes, we don't always know the rise time of a signal but need an idea of its bandwidth anyway. Using a simplifying assumption, we can estimate the bandwidth of a clock wave from just its clock frequency. Still, it is important to keep in mind that it is not the clock frequency that determines the bandwidth, it is the rise time. If all we know about the waveform is the clock frequency, we can't know the bandwidth for sure; we can only guess.

To evaluate the bandwidth of a signal from just its clock frequency, we have to make a very important assumption. We need to estimate what a typical rise time might be for a clock wave.

How is the rise time related to the clock period in a real clock waveform? In principle, the only relationship is that the rise time must be less than 50% of the period. Other than this, there is no restriction, and the rise time can be any arbitrary fraction of the period. It could be 25% of the period, as in cases where the

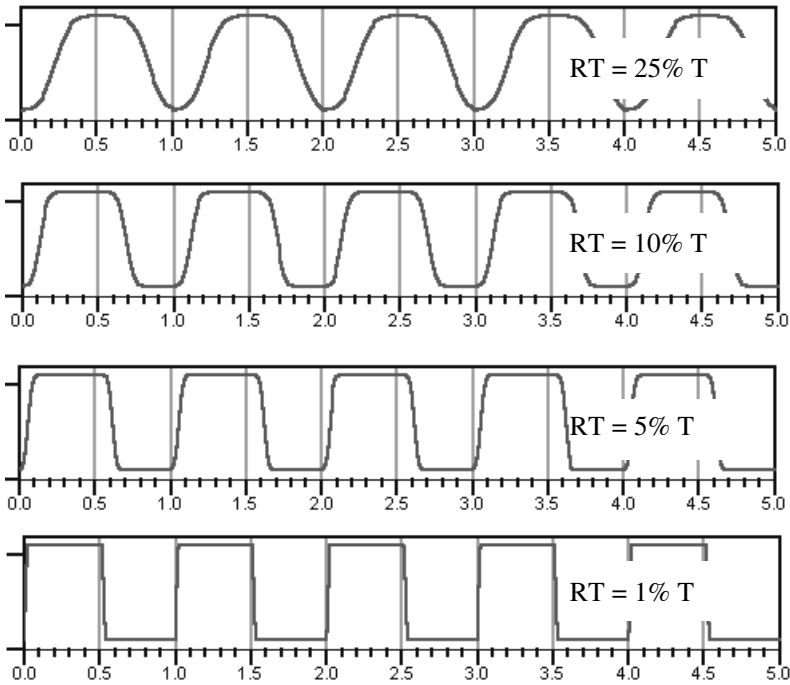


Figure 2-14 Four different waveforms, each with exactly the same 1-GHz clock frequency. Each of them has a different rise time, as a fraction of the period, and hence different bandwidths.

clock frequency is pushing the limits of the device technology, such as in 1-GHz clocks. It could be 10% of the period, which is typical of many microprocessor-based products. It could be 5% of the period, which is found in high-end FPGAs driving external low-clock-frequency memory buses. It could even be 1% if the board-level bus is a legacy system.

If we don't know what fraction of the period the rise time is, a reasonable generalization is that the rise time is 7% of the clock period. This approximates many typical microprocessor-based boards and ASICs driving board-level buses. From this, we can estimate the bandwidth of the clock waveform.

It should be kept in mind that this assumption of the rise time being 7% of the period is a bit aggressive. Most systems are probably closer to 10%, so we are assuming a rise time slightly shorter than might typically be found. Likewise, if we are underestimating the rise time, we will be overestimating the bandwidth, which is safer than underestimating it.

If the rise time is 7% of the period, then the period is 1/0.07 or 15 times the rise time. We have an approximation for the bandwidth as 0.35/rise time. We can relate the clock frequency to the clock period, because they are each the inverse of the other. Replacing the clock period for the clock frequency results in the final relationship; the bandwidth is five times the clock frequency:

$$BW_{\text{clock}} = 5 \times F_{\text{clock}} \quad (2-5)$$

where:

BW_{clock} = the approximate bandwidth of the clock, in GHz

F_{clock} = the clock repeat frequency, in GHz

For example, if the clock frequency is 100 MHz, the bandwidth of the signal is about 500 MHz. If the clock frequency is 1 GHz, the bandwidth of the signal is about 5 GHz.

This is a generalization and an approximation, based on the assumption that the rise time is 7% of the clock period. Given this assumption, it is a very powerful rule of thumb, which can give an estimate of bandwidth with very little effort. It says that the highest sine-wave-frequency component in a clock wave is typically the fifth harmonic!

It's obvious, but bears repeating, that we always want to use the rise time to evaluate the bandwidth. Unfortunately, we do not always have the luxury of knowing the rise time for a waveform. And yet, we need an answer *now*!

TIP Sometimes getting an OK answer is often more important than getting a BETTER answer LATE.

2.14 Bandwidth of a Measurement

So far, we have been using the term *bandwidth* to refer to signals, or clock waveforms. We have said that the bandwidth is the highest significant sine-wave-frequency component in the waveform's spectrum. And, for signals, we said *significant* was based on comparing the amplitude of the signal's harmonic to the amplitude of an equivalent repeat frequency ideal square wave's.

We also use this term *bandwidth* to refer to other quantities. In particular, it can relate to the bandwidth of a measurement, the bandwidth of a model, and the bandwidth of an interconnect. In each case, it refers to the highest sine-wave-

frequency component that is significant, but the definition of significant varies per application.

The bandwidth of a measurement is the highest sine-wave-frequency component that has significant accuracy. When the measurement is done in the frequency domain, using an impedance analyzer or a network analyzer, the bandwidth of the measurement is very easy to determine. It is simply the highest sine-wave frequency in the measurement.

The measured impedance of a decoupling capacitor, from 1 MHz up to 1 GHz, shows that below about 10 MHz, the impedance behaves like an ideal capacitor, but above 10 MHz, it looks like an ideal inductor. Such a measurement is shown in Figure 2-15. There is good, accurate data up to the full range of the network analyzer, in this case, up to 1 GHz. The bandwidth of the measurement is 1 GHz in this example. The measurement bandwidth is not the same as the useful application bandwidth of the device.

When the measuring instrument works in the time domain, such as a time-domain reflectometer (TDR), the bandwidth of the measurement can be found by the rise time of the fastest signal that can be launched into the DUT. After all, this is a rough measure of when the higher-frequency components are small.

In a typical TDR, a fast step edge is created and its change due to interaction with the DUT is measured. A typical rise time entering the DUT is 35 psec to 70

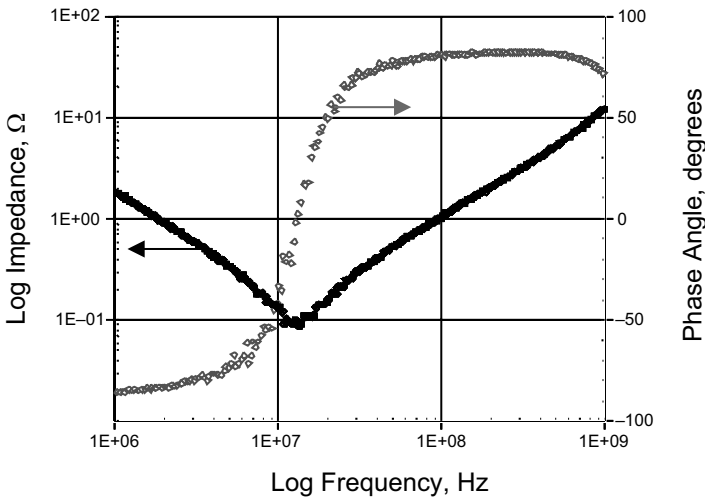


Figure 2-15 Measured impedance of a small 1206 ceramic decoupling capacitor. The measurement bandwidth for this data is 1 GHz.

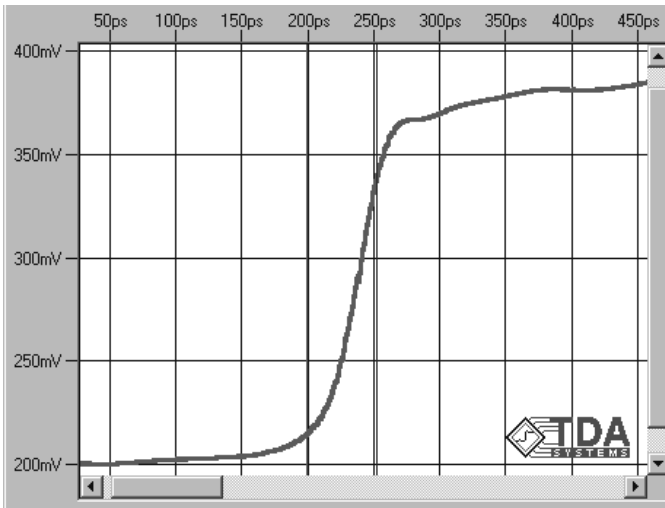


Figure 2-16 Measured TDR profile from the output of a 1-meter cable and microprobe tip, open at the end. The TDR rise time after the cable and probe is about 52 psec. The bandwidth of the measurement is about $0.35/52$ psec = 7 GHz. The measurement was recorded with TDA Systems IConnect software, using a GigaTest Labs Probe Station.

psec, depending on the probes and cables used. Figure 2-16 shows the measured rise time of a TDR as about 52 psec. The bandwidth of the edge is $0.35/52$ psec = 0.007 THz or 7 GHz. This is the bandwidth of the signal coming out of the TDR and is a good first order measure of the bandwidth of the measurement.

In state of the art TDRs, calibration techniques allow the bandwidth of the measurement to exceed the bandwidth of the signal. The bandwidth of the measurement is set by when the signal-to-noise ratio of a frequency component is below a reasonable value, like 10. The bandwidth of the measurement of some TDRs can exceed the signal's bandwidth by a factor of 3-5, making the bandwidth of a TDR's measurement as high as 30 GHz.

2.15 Bandwidth of a Model

TIP When we refer to the bandwidth of a model, we are referring to the highest sine-wave-frequency component where the model will accurately predict the actual behavior of the structure it is representing. There are a few tricks that can be used to determine this, but in general, only a comparison to a measurement will give a confident measure of a model's bandwidth.

The simplest starting equivalent circuit model to represent a wire bond is an inductor. Up to what bandwidth might this be a good model? The only way to really tell is to compare a measurement with the prediction of this model. Of course, it will be different for different wire bonds.

As an example, we take the case of a very long wire bond, 300 mils long, connecting two pads over a return-path plane 10 mils below. This is diagrammed in Figure 2-17. A simple starting circuit model is a single ideal inductor and ideal resistor in series, such as shown in Figure 2-18. The best values for the L and R give a prediction for the impedance that closely matches the measured impedance up to 2 GHz. The bandwidth of this simple model is 2 GHz. This is shown in Figure 2-18.

We could confidently use this simple model to predict performance of this physical structure in applications that had signal bandwidths of 2 GHz. It is surprising that for a wire bond this long, the simplest model, that of a constant ideal inductor and resistor, works so well up to 2 GHz. This is probably higher than the useful bandwidth of the wire bond, but the model is still accurate up to this high a frequency.

Suppose we wanted a model with an even higher bandwidth that would predict the actual impedance of this real wire bond to higher frequency. We might add the effect of the pad capacitance. Building a new model, a second-order model, and finding the best values for the ideal R, L, and C elements result in a simulated impedance that matches the actual impedance to almost 4 GHz. This is shown in Figure 2-18.

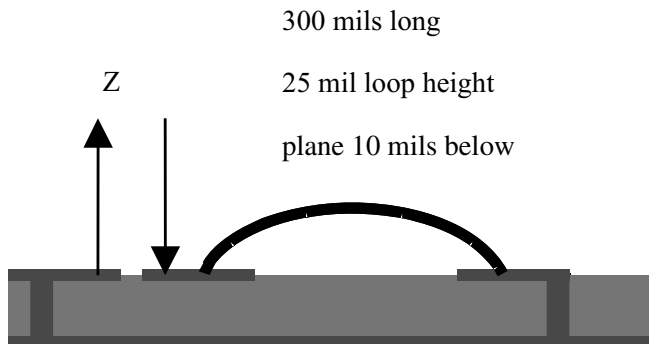


Figure 2-17 Diagram of a wire-bond loop between two pads, with a return path about 10 mils beneath the wire bond.

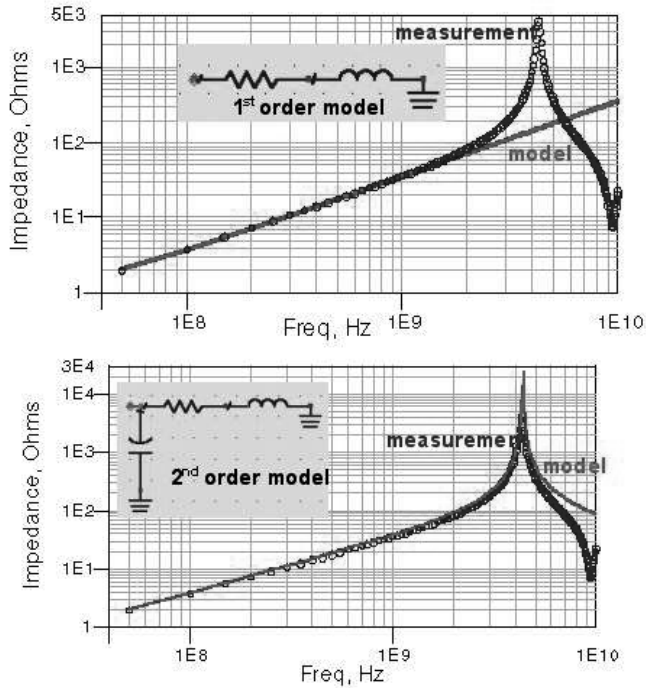


Figure 2-18 Top: Comparison of the measured impedance and the simulation based on the first-order model. The agreement is good up to a bandwidth of about 2 GHz. Bottom: Comparison of the measured impedance and the simulation based on the second-order model. The agreement is good up to a bandwidth of about 4 GHz. The bandwidth of the measurement is 10 GHz, measured with a GigaTest Labs Probe Station.

2.16 Bandwidth of an Interconnect

The bandwidth of an interconnect refers to the highest sine-wave-frequency component that can be transmitted by the interconnect without significant loss. What does *significant* mean? In some applications, a transmitted signal that is within 95% of the incident signal is considered too small to be useful. In other cases, a transmitted signal that is less than 10% of the incident signal is considered usable. In long-distance cable-TV systems, the receivers can use signals that have only 1% of the original power. Obviously, the notion of how much transmitted signal is significant is very dependent on the application and the particular specification. In reality, the bandwidth of an interconnect is the highest sine-wave frequency at which the interconnect still meets the performance specification for the application.

TIP In practice, *significant* means when the transmitted frequency-component amplitude is reduced by -3 dB, which means that its amplitude is reduced to 70% of the incident value. This is often referred to as the 3-dB bandwidth of an interconnect.

The bandwidth of an interconnect can be measured in either the time domain or the frequency domain. In general, we have to be careful interpreting the results if the source impedance is different than the characteristic impedance of the line, due to the complication of multiple reflections.

Measuring the bandwidth of an interconnect in the frequency domain is very straightforward. A network analyzer is used to generate sine waves of various frequencies. It injects the sine waves in the front of the interconnect and measures how much of each sine wave comes out at the far end. It is basically measuring the transfer function of the interconnect, and the interconnect is acting like a filter. This is also sometimes referred to as the *insertion loss* of the interconnect. The interpretation is simple when the interconnect is 50 Ohms, matched to the network analyzer’s impedance.

For example, Figure 2-19 shows the measured transmitted amplitude of sine waves through a 4-inch length of a 50-Ohm transmission line in FR4. The

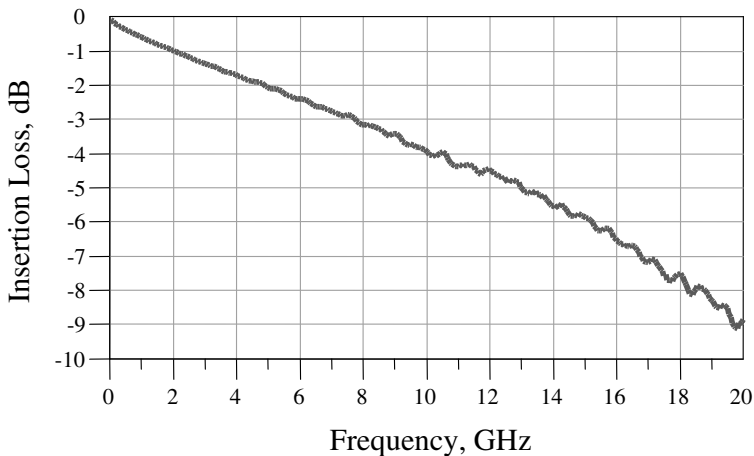


Figure 2-19 Measured transmitted amplitude of different sine-wave signals through a 4-inch-long transmission line made in FR4. The 3 dB bandwidth is seen to be about 8 GHz for this cross section and material properties. Measured with a GigaTest Labs Probe Station.

measurement bandwidth is 20 GHz in this case. The 3-dB bandwidth of the interconnect is seen to be about 8 GHz. This means that if we send in a sine wave at 8 GHz, at least 70% of the amplitude of the 8-GHz sine wave would appear at the far end. More than likely, if the interconnect bandwidth were 8 GHz, nearly 100% of a 1-GHz sine wave would be transmitted to the far end of the same interconnect.

The interpretation of the bandwidth of an interconnect is the approximation that if an ideal square wave were transmitted through this interconnect, each sine-wave component would be transmitted, with those components lower than 8 GHz having roughly the same amplitude coming out as they did going in. But the amplitude of those components above 8 GHz would be reduced to insignificance.

A signal that might have a rise time of 1 psec going into the interconnect would have a rise time of $0.35/8 \text{ GHz} = 0.043 \text{ nsec}$ or 43 psec when it came out. The interconnect will degrade the rise time.

TIP The bandwidth of the interconnect is a direct measure of the minimum rise-time signal an interconnect can transmit.

If the bandwidth of an interconnect is 1 GHz, the fastest edge it can transmit is 350 psec. This is sometimes referred to as its intrinsic rise time. If a signal with a 350-psec edge enters the interconnect, what will be the rise time coming out? This is a subtle question. The rise time exiting the interconnect can be approximated by:

$$RT_{\text{out}}^2 = RT_{\text{in}}^2 + RT_{\text{interconnect}}^2 \quad (2-6)$$

where:

RT_{out} = the 10–90 rise time of the output signal

RT_{in} = the 10–90 rise time of the input signal

$RT_{\text{interconnect}}$ = the intrinsic 10–90 rise time of the interconnect

This assumes that both the incident spectra and the response of the interconnect correspond to a Gaussian-shaped rise time.

For example, in the case of this 4-inch-long interconnect, if a signal with a rise time of 50 psec were input, the rise time of the transmitted signal would be:

$$\text{sqrt}(50 \text{ psec}^2 + 43 \text{ psec}^2) = 67 \text{ psec.} \tag{2-7}$$

This is an increase of about 17 psec in the rise time of the transmitted waveform compared to the incident rise time.

In Figure 2-20, we show the measured time-domain response of the same 4-inch-long, 50-Ohm interconnect that was measured in the frequency domain above. The input waveform has been time shifted to lie directly at the start of the measured output waveform.

The rise time of the waveform going into the PCB trace is 50 psec. The measured 10–90 rise time of the output waveform is about 80 psec. However, this is somewhat distorted by the long roll to stabilize at the top, characteristic of the behavior of lossy lines. The extra delay at the 70% point is about 15 psec, which is very close to what our approximation above predicted.

If a 1-nsec rise-time signal enters an interconnect with an intrinsic rise time of 0.1 nsec, the rise time of the signal transmitted would be about $\text{sqrt}(1 \text{ nsec}^2 + 0.1 \text{ nsec}^2)$, or 1.005 nsec, which is still basically 1 nsec. The interconnect would not affect the rise time. However, if the interconnect intrinsic rise time were 0.5 nsec, the output rise time would be 1.1 nsec, and would start to have a significant impact.

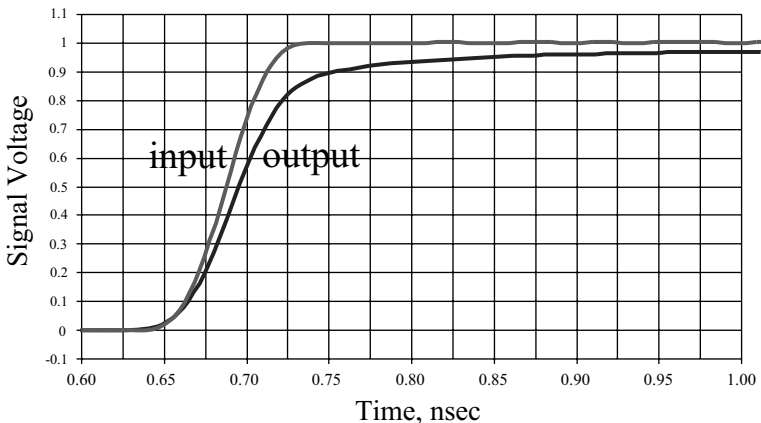


Figure 2-20 Measured input and transmitted signal through a 4-inch long, 50-Ohm transmission line in FR4 showing the rise-time degradation. The input rise time is 50 psec. The predicted output rise time is 67 psec based on the measured bandwidth of the interconnect. Measured with a GigaTest Labs Probe Station.

TIP As a simple rule of thumb, in order for the rise time of the signal to be increased by the interconnect less than 10%, the intrinsic rise time of the interconnect should be shorter than 50% of the rise time of the signal.

TIP In the frequency-domain perspective, to support the transmission of a 1-GHz bandwidth signal, we want the bandwidth of the interconnect to be at least twice as high, or 2 GHz.

It is important to keep in mind that this is a rule of thumb and it should not be used for design sign-off. It should be used only for a rough estimate or to identify a goal. If the bandwidth of an interconnect is within a factor of two of the bandwidth of the signal, it would probably be important to perform an analysis of how the interconnect affected the entire signal's spectrum.

2.17 The Bottom Line

1. The time domain is the real world and is typically where high-speed digital performance is measured.
2. The frequency domain is a mathematical construct where very specific, specialized rules apply.
3. The only reason to ever leave the time domain and use the frequency domain is to get to an answer faster.
4. The rise time of a digital signal is commonly measured from 10% of the final value to 90% of the final value.
5. Sine waves are the only waveform that can exist in the frequency domain.
6. The Fourier Transform converts a time-domain waveform into its spectrum of sine-wave-frequency components.
7. The spectrum of an ideal square wave has amplitudes that drop off at a rate of $1/f$.
8. If the higher-frequency components are removed in the square wave, the rise time will increase.
9. The bandwidth of a signal is the highest sine-wave-frequency component that is significant, compared to the same harmonics in an ideal square wave with the same repeat frequency.

10. A good rule of thumb is that the bandwidth of a signal is $0.35/\text{rise time}$ of the signal.
11. Anything that decreases the bandwidth of a signal will increase its rise time.
12. The bandwidth of a measurement is the highest sine-wave frequency where the measurement has good accuracy.
13. The bandwidth of a model is the highest sine-wave frequency where the predictions of the model give good agreement with the actual performance of the interconnect.
14. The bandwidth of an interconnect is the highest sine-wave frequency where the performance of the interconnect still meets specifications.
15. The 3-dB bandwidth of an interconnect is the highest sine-wave frequency where the attenuation of a signal is less than -3 dB.

This page intentionally left blank

- 2D field solvers
 - calculating characteristic impedance, 265–270
 - calculating differential impedance, 494–495
 - calibrating, 264
 - capacitance, 143–146
 - Maxwell capacitance matrix, 417–423
 - parasitic extraction tool, 34
- 2D modeling tool, 39
- 3D field solver, 34, 164, 166, 185
- 3M C-Ply, 137–138

- A**
- A_{cond} , 380, 579–580
- A_{diel} , 579–580
- AC current, 193–194, 366
- AC simulation, 27, 102–105
- active elements, 102
- active equalization, 403
- active net. *See* aggressor net
- aggressor net, 405–410, 427–429, 447, 453–464, 466–469, 471, 517, 539–542
- Agilent
 - 86100 DCA TDR, 10
 - 54120 TDR, 395
 - Advanced Design System (ADS), 103
 - N5230 VNA, 563
 - PLTS, 565
- Alloy 42, 119, 154, 202–204

- alloys, 154, 202–204
- Altera Stratix II GX FPGA, 627
- alumina, 134
- aluminum, 119
- AN-905 National Semiconductor Application Note, 493–494
- analytical approximations, 30–34
- angular frequency, 49–50, 94, 97, 346, 357–359, 364, 368, 382
- Ansoft
 - High Frequency Structure Simulator (HFSS), 25
 - Q3D field solver, 164
 - SI2D field solver, 145
 - 2D Extractor, 144
- antipads, 401, 620
- approximations
 - analytical, 30–34
 - capacitance per length, 138–143
 - characteristic impedance, 262–265
 - loop inductance, 175–176, 652–661
 - microstrip, 141, 264–265
 - parallel plate, 347–348
 - resistance of interconnects, 115–117
 - stripline, 142, 264–265
- area
 - cross-section, 116, 120
 - of the loop, 174–176
 - planes, 136, 359, 690–692

asymmetric stripline, 213
 asymmetries, 481, 524, 529–531, 537, 605–607
 attenuation, 3, 60–61, 231–232, 342
 decibels (dB), 371–376
 in lossy lines, 376–390, 400–402
 napiers, 372
 S-parameters (scattering parameters),
 579–580
 AVX, 671–672, 700–701
 AWG (American Wire Gauge) reference, 120
 axial-lead resistors, 108–109, 330–331

B

backward cross-talk coefficient, 440, 519
 backward-moving current, 410, 432, 436–
 439, 453
 balanced S-parameters. *See* differential
 S-parameters
 balanced transmission lines, 213–214
 Ball grid arrays (BGAs), 8, 219, 267, 309–
 310, 587–588, 664–666, 710–711
 bandwidth
 clock frequency, 68–70
 estimating, 69–70
 interconnect, 74–78, 390–396
 lumped-circuit model, 274–275
 of a measurement, 70–72
 model, 72–74
 rise time and, 43, 58–63
 signals, 67
 barium titanate, 134, 137, 154
 BCB, 134
 Bell, Alexander Graham, 373–374
 Bell (Bel) scale, 374
 Berkeley Nuclear Corp (BNC), 139, 230
 Bismaleimide triazine (BT), 134, 143, 353,
 393
 bit error rate, 339–340, 399, 606–607, 613
 blind vias, 400, 605
 bounce diagrams, 292–294
 BR, 604–605
 branch, 6–7, 282, 309
 broadside-coupled differential stripline, 480,
 498, 500–501

bulk capacitance, 632–635, 676, 679, 681
 bulk conductivity, 202, 349–351, 359
 bulk resistivity, 118–119, 342–343, 344
 buried vias, 400, 605
 bus noise, 454–457

C

C_{even} , 548–549
 C_{load} , 547–549
 C_{loaded} , 419
 C_{odd} , 547–548
 C_{planes} , 677–680, 688–689
 C11, 414, 422, 442, 464–465, 487–491, 547
 C12, 414, 427–428, 433–434, 464, 486–491,
 547–550
 C-Ply laminates, 13–14, 137–138
 calibrating 2D field solvers, 264
 capacitance
 approximations, 130–131
 coax cable, 139–140
 corners, 320
 decoupling, 135–138, 179, 181, 187, 631
 dielectric constant, 133–134
 displacement current, 129–130
 effective dielectric constant, 146–149
 of an ideal capacitor, 89–91, 99
 input-gate, 311–313
 insulating dielectric, 129
 measurement of, 127–129
 negative values of, 420–423
 parallel plate approximation, 131–132
 per length, 138–143, 320–321, 327
 planes, 677–681
 of a sphere, 130–131
 2D field solvers, 143–146
 voltage and, 89–91, 127–128
 capacitance matrix, 413–423, 486, 546–550
 See also Maxwell capacitance matrix;
 SPICE (Simulation Program with
 Integrated Circuit Emphasis)
 capacitive coupling, 9
 capacitive delay adders, 317–319
 capacitive discontinuities, 314–317, 324
 capacitively coupled currents, 431

- capacitor(s)
 - chip, 632
 - current flow through, 128–130
 - DC blocking, 528–529
 - decoupling, 644–646
 - electrolytic, 631–634, 676–677
 - ESL, 649–652
 - estimating needs, 681–683
 - interdigitated capacitors (IDCs), 254, 650–651, 700–702, 713
 - location effects, 703–707
 - loop inductance in, 180
 - MLCC, 632, 646–650, 701, 711
 - mountings, 661–667
 - mutual capacitor, 411–412
 - in parallel, 667–673
 - reverse aspect ratio, 700
 - and SRF, 673–675
 - tantalum capacitors, 631–634, 677
 - values, 675–681, 687–692
- cavity spreading inductance, 652, 666, 695
- center-to-center separation, 140, 165–166, 170–173, 176–177, 654
- characteristic impedance
 - approximations, 262–265
 - calculating, 265–270
 - coax cable, 230
 - even-mode, 520, 546–550
 - of free space, 231
 - frequency variation, 278–279
 - imaginary part, 367–368
 - lossy transmission lines, 367–369
 - magnitude, 368–369
 - matrix, 547–553
 - odd-mode, 520
 - proximity effect, 488
 - real part, 367–368
 - single-ended, 486, 489, 490, 520
 - transmission lines, 227–233, 385–390
 - 2D field solvers and, 265–270
- chip capacitors, 632
- chip-scale packages (CSPs), 8, 11, 642
- chokes, 15, 82, 538–541, 545
- circuit model. *See* models and modeling
- circuit theory, 26, 101–105, 362
- circuit topology, 99, 114–115, 190, 528
- circular loop inductance, 175
- clearance holes, 187–188
- clock cycle, 44
- clock frequency, 16–20
 - bandwidth and, 68–70
 - increasing, 1–3
 - and signal integrity problems, 1–2
 - and signal rise times, 3
- clock period, 68–70
- coax cable, 139–140, 230, 262–263
- cobalt, 154, 202
- coils, 539
- collapse, 340, 399, 613
- common impedance, 524–528, 535–536
- common impedance, 508–511
- common mode signals, 597
- common signals, 478–482
 - chokes, 538–541
 - common signal component, 481–482
 - component in LVDS, 479
 - conversion to, 529–534
 - EMI and, 534–539
 - modes and, 508–513, 605–608
 - pi and tee topologies, 525–528
 - S-parameters (scattering parameters), 596–600
 - terminating, 522–529, 522–533
- compensation, 331–334
- complex dielectric constant, 356–358, 385, 391–393
- conductivity, 118, 196, 202, 348
- controlled-impedance board, 228, 282
- controlled-impedance interconnects, 230
- controlled-impedance lines, 227–230
- convolution integral, 610–612
- coplanar, 146, 212–213, 480
- copper, 119, 122, 124, 137, 200, 343
 - electron velocity in, 214–215
 - skin depth, 195–196, 198–200
 - surface smoothness, 381
- copper puddle, 691
- corners, 319–323, 335

cosine waves, 96–97
 coupled transmission lines, 413–417, 451–452
 coupling, 9, 10
 cross talk, 407–409, 411
 differential impedance and, 482–493
 differential pairs, 541, 544–546, 551
 high Q resonators and, 585–588
 inductive coupling, 9, 29
 models, 411
 cross talk, 10–11
 active net/quiet net, 405–409, 431
 capacitive coupling, 9
 capacitively coupled currents, 431–435
 coupling, 407–409, 411
 design principle, 41
 dielectric constant, 464–465
 differential pairs, 539–542
 equivalent circuit model, 411–413
 far-end, 409–411, 426, 441–451
 fringe fields, 407–408
 guard traces, 457–464
 impedance and, 82–84
 induced voltage, 160
 inductance matrix, 424–425
 inductively coupled currents, 9, 435–437
 Maxwell capacitance matrix, 417–423
 near-end, 409–411, 426, 429, 438–451, 463, 520
 NEXT and FEXT, 409–411, 438
 noise budget, 440
 noise sources, 9–11
 quiet net, 405
 reduction strategies, 473
 saturation length, 429–432, 438–439, 454
 signal swing, 405, 440
 simulating, 451–457
 SPICE capacitance matrix, 413–417
 superposition, 406–407
 switching noise, 409, 469–473
 timing, 466–469
 2D field solvers, 417–423
 in uniform transmission lines, 425–431, 473

current distributions
 in a differential pair, 496–502
 skin depth and, 193–201
 current flow (direction), 168–170, 436–437
 CyanateEster, 353, 393

D

damping, 586, 679, 711–712
 data mining, 594–596
 DC-blocking capacitor, 528–529
 DC (direct current), 48, 56, 92–93, 193, 200, 349, 365
 decibels (dB), 49, 75–76, 371–376
 decoupling capacitance, 135–138, 179, 181, 187, 631
 decoupling capacitors, 644–646, 699–703
 delay adders, 233, 312–313, 317–320, 324, 331–332
 Delphi Electronics, 38–39
 delta I noise, 9, 16, 93, 161, 189, 196, 435–437, 469–471, 475
 design methodology, 22–24
 diagonal elements
 converting, 421–422
 impedance matrix, 551
 inductance matrix, 424, 548
 Maxwell capacitance matrix, 420
 SPICE capacitance matrix, 416
 diamond, 134
 dielectric constant, 217–218, 385
 capacitance, 133–134, 146
 complex, 356–358, 385, 391–393
 cross talk, 464–465
 dissipation factor and, 352–353, 355–359
 Dk, 133, 580, 637–638, 677–678, 704
 effective dielectric constant, 146–149
 frequency and, 134
 imaginary part, 356–358, 385
 real part, 356–359, 382–383, 385
 dielectric-loss shunt resistance, 361–362
 dielectric material, 134, 143, 184, 444–446, 448–450, 464
 dielectric spectroscopy, 352
 difference voltage, 476, 482, 511

- differential impedance, 482–486, 493–496, 506–508, 526–527
 - differential insertion loss, 600–606
 - differential mode, 506, 553, 597, 605
 - differential mode signals, 597
 - differential noise, 540–542
 - differential pairs
 - characteristic impedance matrix, 550–553
 - common impedance, 508–511
 - common signal component, 481–482
 - coupling, 482–493, 544–546
 - cross-sections, 480–481
 - cross talk, 539–542
 - current distribution, 496–502
 - difference voltage, 476, 482, 511
 - differential impedance, 482–486, 493–496, 506–508, 526–527
 - differential signaling, 475–480
 - EMI, 476, 534–539
 - far-end cross talk, 516–518
 - modes, 504
 - odd and even modes, 502–511, 513–518, 546–550
 - pair makeup, 480
 - return path gaps, 542–544
 - signal velocity, 513–518
 - differential S-parameters, 596–600, 607–609
 - differential signals, 475–480, 505
 - conversion to common signals, 529–534
 - pi and tee topologies, 525–528
 - terminating, 522–529
 - dipoles
 - dielectric materials and, 134
 - dipole moment, 352
 - dissipation factor and, 351–354, 385
 - reorientation, 349
 - Discrete Fourier Transform (DFT), 51–55
 - dispersion, 370–371, 601
 - displacement current, 129–130
 - dissipation factor, 342, 351–359, 367, 382–383, 385, 402, 580–581
 - distortions, 7, 83, 300–301, 320, 529
 - domains. *See* frequency domain; time domain
 - double bonding, 172
 - DriClad (IBM), 353, 393
 - DTDR (differential TDR), 521–523
 - DUT (device under test), 35
 - dV/dt, 16, 129, 311–312, 315, 346, 355, 426–428
- ## E
- eddy currents, 204–206, 245–247, 435–437
 - edge-coupled microstrip, 480, 496–499, 502–505, 509–511, 543–544
 - edge-coupled stripline, 480, 493–494
 - effective dielectric constant, 146–149
 - effective inductance, 156, 167–174, 192
 - electrolytic capacitors, 631–634, 676–677
 - electromagnetic compatibility (EMC) test, 607, 617
 - electromagnetic fields, 24–25
 - electromagnetic interference (EMI), 3, 14–15, 41, 68, 82–84, 534–539
 - electromagnetic interference (EMI)
 - certification tests, 535–537
 - electron velocity, 214–215
 - embedded microstrip, 148–149, 213, 444–445, 450
 - emissions, 15
 - equalization, 402–403
 - equivalent electrical circuit model. *See* models and modeling
 - equivalent inductance, 172, 189–192, 709, 715
 - equivalent series inductance (ESL), 181, 189–190, 254, 649–652
 - See also* capacitor(s); PDN (power distribution network)
 - equivalent series resistance (ESR), 254, 668–674, 679, 711–712
 - Ethernet, 476
 - eutectic Pb/Sn solder, 119
 - even mode, 411, 502–506, 511–518
 - even-mode characteristic impedance, 520, 546–550
 - even-mode impedance, 411, 508–511, 520–522, 552
 - even-mode voltage components, 511–513

external self-inductance, 193, 200–202
 eye diagrams, 337–340, 342, 399–402,
 612–613

F

f (frequency) designation, 49–50
 F (repeat frequency), 44, 52–55, 64–66, 70
 f_{res} , 272, 586–587, 603–604, 704
 “fab” (chip-fabrication facility), 19–20
 fall time, 18, 45, 300
 false triggering, 5, 8
 far-end cross talk, 10, 426, 513–518
 coefficient, 442–444, 451
 decreasing, 448–451
 differential pairs, 516–519
 FEXT, 409–411, 438, 442–444
 TD and, 514
 far-end termination, 305
 far-end Thevenin termination, 305
 far-field electric-field strength, 14, 536
 FCC (Federal Communications Commission)
 EMI tests, 20, 535–536, 607
 FDTI (frequency domain target impedance)
 method, 692–698
 field solvers. *See* 2D field solvers
 ferrite core, 539
 ferrites, 15, 82, 202
 ferromagnetic metals, 154, 202
 50-Ohm line, 143, 261
 50 Ohms, 231–235
 first-order model, 101
 forward-moving current, 434–437, 460
 .FOUR command, 53
 four-point probe, 122–123
 Fourier Transforms
 Discrete Fourier Transform (DFT), 51–55,
 58, 66–67
 Fast Fourier Transform (FFT), 51–53
 Fourier Integral (FI), 51–53
 inverse, 57, 609
 FPGAs, 11, 69, 627, 693, 710
 FR4, 14, 60–61, 134, 137, 219, 353, 393
 bulk conductivity, 350
 dielectric constant, 134

 dissipation factor, 383
 FR5, 581–583
 free space, 130–132, 231
 frequency-dependent losses, 337–340, 386
 frequency domain, 25–27, 43
 bandwidth and, 48
 converting the spectrum into the
 waveform, 57
 EMI and, 49
 impedance and, 48
 lossy transmission lines and, 49
 S-parameters (scattering parameters),
 609–613
 simulation, 27, 102–105
 sine waves, 46–51
 VNA and, 49
 frequency ranges, 632
 fringe fields, 132, 145, 268–269, 407–408,
 422, 466, 469
 fully embedded microstrip, 149, 445, 450
 FWHM, 586

G

G_L (shunt conductance), 362–365, 367–368,
 377–379
 gaps in return paths, 542–544
 gate capacitance, 637–638
 gauge chart, wire, 120
 GETek, 134, 353, 393
 GHz, 19, 63
 Gigabit Ethernet, 22
 GigaTest Labs Probe Station, 37
 glass, 134, 218, 353, 393
 gold, 119–120
 Grasso, Charles, 186
 Green’s function, 610
 ground bounce, 3, 9–10, 168–173, 184
 PDN, 616–617
 reducing, 469–470
 return path, 249, 253
 switching noise and, 169, 170
 ground line. *See* return path
 ground planes, 82, 135–138, 184–188
 guard traces, 457–464

- H**
- hacking interconnects, 559, 605
 - harmonics, 55–60, 66, 623
 - Henry (Weber/Amp), 155
 - high-density interconnects (HDI), 11
 - high-permeability materials, 202–204
 - high-speed regime, 3
 - high-speed serial links, 21, 339, 342, 606
 - humidity, 353
- I**
- I_{comm} , 535–536
 - I_{peak} , 626
 - I_{max} , 625
 - I_{trans} , 286
 - $I_{\text{transient}}$, 624–628
 - IBIS (input/output buffer interface spec), 27–29
 - ideal circuit elements, 29, 48, 85, 86–94, 99, 347
 - ideal differential pair, 519–520
 - ideal distributed transmission line, 258–259, 270–271
 - ideal lossy transmission lines, 360–367, 397–398
 - ideal resistor, 85, 88–89, 99, 108, 347, 398
 - ideal RLC circuit, 48
 - ideal square wave, 54–60, 65–66, 391
 - ideal transmission line, 88, 106, 209–210, 257, 270–274, 519–520
 - IM Intermark, 15
 - image currents, 204–205
 - impedance profile, sculpting, 687, 691–698
 - impedance, 5–9, 32, 81–86
 - analyzer, 35, 71
 - common, 508–511, 524–528, 535–536
 - controlled, 227–230
 - differential impedance, 482–486, 493–496, 506–508, 526–527
 - discontinuities, 6–7, 281–284, 307, 589
 - even-mode, 411, 508–511, 520–522, 552
 - in the frequency domain, 94–99
 - i/o connectors, 15
 - ideal capacitor, 89–92, 647
 - ideal inductor, 92–94, 99
 - ideal resistor, 88–89, 108
 - inductance, 640–642
 - input, 234–238
 - instantaneous, 5, 36, 223–228, 235–236, 281
 - interconnect, 16, 81–82
 - matrix, 550–553
 - measuring, 234–235
 - models, 99–101
 - odd-mode, 411, 506–508, 520–522, 528–529, 551
 - odd-mode characteristic impedance, 520, 546–550
 - PDN, 621–629, 645
 - peak, 628, 641, 670–681, 712–716
 - port, 559, 573–574, 599
 - real versus ideal circuit elements, 86–88
 - shunt impedance, 315–316
 - single-ended, 40, 484–486, 497–501
 - single-ended characteristic impedance, 489–491, 520
 - source, 290–292
 - target, 618, 621–629
 - traces, 7
 - transmission line, 233–238, 282–284, 385–390
 - 2D field solver, 265–270
 - See also* characteristic impedance; SPICE (Simulation Program with Integrated Circuit Emphasis)
 - impulse response waveforms, 609–612
 - in-phase currents, 355–359
 - induced current, 204–206, 245–247, 435–437
 - induced voltage, 159–160
 - inductance, 92, 99, 152–161
 - circular loop, 175
 - common definition, 152
 - decreasing, 175
 - effective, 167–174, 192
 - equivalent, 172, 189–192, 709, 715
 - ferromagnetic metals, 154
 - ground bounce, 168–173
 - loop mutual, 188–189, 192, 413, 471

inductance (*continued*)

loop self-inductance, 167, 173–178, 192, 197, 424–425
 magnetic-field lines, 152–161
 mounting, 631, 650–652, 684, 695, 703–706
 partial, 156, 161–166, 192
 partial mutual, 166, 171, 192
 partial self-inductance, 161–165, 169, 174, 176, 190, 192, 197
 per length, 207, 227, 260, 366, 440
 per square of planes, 183–184, 656–661
 power integrity and, 178–183
 principles of, 152–161
 self-inductance, 156–158, 192–193, 201
 spacing rules and, 170–173
 spreading, 186, 653, 657, 662, 685, 704–710
 total, 156
 types of, 192
 voltage and, 158–161
 Webers, 153–154
See also loop inductance; mutual inductance

inductance matrix, 424–425, 547–550
 inductive coupling, 9, 29
 inductively coupled currents, 9, 435–437
 Infiniband, 21
 input-gate capacitance, 311–313
 input impedance, 234–238
 insertion losses, 75, 386–390
 differential insertion loss, 600–606
 magnitude of, 577–582
 in non-50-Ohm lines, 589–594
 simulating, 567–570
 instantaneous impedance, 5, 36, 223–228, 235–236
 See also transmission lines
 instantaneous voltage, 311, 428–429
 insulators, 133–134
 integrated passive devices (IPDs), 107–109
 Intel processor chips, 16–18
 inter-symbol interference (ISI), 8, 337–340, 396
 interconnect(s), 334
 alloys, 154

approximation of resistance, 115–117
 bandwidth, 74–78, 390–396
 capacitance and, 128
 capacitance per length approximations, 138–140
 dielectric constants of insulators, 133–134
 eye diagram, 612
 impedance, 16, 81–82
 Maxwell's Equations and, 113–114
 models and, 28
 PDN, 632
 permeability, 202
 propagation delay, 219
 speed of light in, 218
 substrates, 121
 transparent, 569–573
 interdigitated capacitors (IDCs), 254, 650–651, 700–702, 713
 internal self-inductance, 193–194, 200–201
 interposer, 593–594, 692
 intrinsic rise time, 76–78
 inverse Fourier Transforms, 57, 609
 ionic motion, 349
 IPC approximations, 141–143, 145–146, 264–267
 IR drop, 618
 iron, 154, 202
 ITRS (International Technology Roadmap for Semiconductors), 17

J

jitter, 338–340, 613

K

k_b , 438–440, 451
 k_f , 443–451, 519
 Kapton, 134, 353
 kink of field, 216–217
 knee frequency, 64
 Kovar, 119, 154, 202–203

L

L_{odd} , 548
 L_{pkg} , 641–642, 715–716

- L_{self} , 32, 424
 L_{spread} . *See* loop spreading inductance
 L_{via} , 387–388, 659–660, 685, 705
 laminate materials, 393
 Laplace's Equation, 143, 417–418
 See also Maxwell's Equations
 lattice diagrams. *See* bounce diagrams
 lead, 119
 leading edge of signal, 219
 leakage current, 347, 350
 Lenz's law, 435–436
 line drivers, 240
 loaded line, 325–327
 loop inductance, 13–14, 156, 167–173, 192
 approximations, 175–176, 652–661
 capacitors, 180
 matrix, 547–550
 PDN, 178–183, 653
 per length, 176–178, 258, 548, 655
 per square of planes, 183–184, 656–661
 of planes and vias, 184–188
 power-distribution network and, 178–183
 radius and, 176–177
 transmission lines and reflections, 327–331
 of two rods, 177
 loop mutual inductance, 188–189, 192, 413, 471
 loop self-inductance, 167, 173–178, 192, 197, 424–425
 loop spreading inductance, 658–659, 662–663, 685, 708–709
 loss angle, 352, 357–359, 385
 lossless transmission lines, 278–279, 340–342
 lossy transmission lines, 360–367
 analyzing, 337–338
 attenuation, 338–339, 342, 376–390, 400–402
 characteristic impedance, 367–369
 conductor loss, 342–346
 dielectric loss, 346–351
 eye diagrams, 399–402
 frequency dependence, 338–339
 intersymbol interference (ISI), 337, 339–340, 396, 399
 measured properties of, 385–390
 modeling, 360–367
 signal velocity, 369–371
 time domain behavior, 397–400
 low-loop inductance decoupling capacitors, 178
 low-loss regime, 366–371
 lumped circuit elements, 88, 106
 lumped circuit model, 270–278, 411–412, 546–547
 LVDS (low-voltage differential signals), 476–479, 523, 541
- M**
 magnetic-field lines, 157–158, 160, 167–170, 193, 202–205, 619
 magnitude, 95–96, 368–369, 577–582
 matrix
 algebra, 52
 impedance, 550–553
 loop inductance, 547–550
 matrix elements, 562–567
 Maxwell capacitance matrix, 417–423
 notation, 414
 transform matrix, 607–609
 See also SPICE (Simulation Program with Integrated Circuit Emphasis)
 Maxwell, James Clerk, 129
 Maxwell capacitance matrix, 417–423
 Maxwell's Equations, 24–26, 33, 113–114, 143, 216–217
 Mears, James, 493
 Mentor Graphics Hyperlynx, 2
 MHz, 3–8, 17–20, 63, 66, 679–681
 microseconds, 63, 180
 microstrip
 approximations, 141, 266
 edge-coupled, 480, 496–499, 502–505, 509–511, 543–544
 embedded, 148–149, 213, 444–445, 450
 interconnects, 141–146, 149
 lines, 458–459
 traces, 450–451
 microvias, 605

mixed-mode S-parameters. *See* differential S-parameters

MLCC capacitor, 632, 646–650, 701, 711

mode conversion, 605–607

mode conversion quadrants, 605

models and modeling

bandwidth and, 72–74, 100–101, 106–110

capacitively coupled currents, 431

circuit topology, 99, 114–115, 190, 528

cost and accuracy, 106

creating models from calculation, 30–35

first-order model, 101

ideal transmission lines in, 106, 109

introduction and basics, 105–110

lossy transmission lines, 360–367

lumped circuit model, 270–278, 411–412, 546–547

real versus ideal circuit elements, 86–88

simplicity in, 105–106

modes of the pair, 504

molybdenum, 119

monotonically, 328

Moore's Law, 20

mounting inductance, 631, 650–652, 684, 695, 703–706

mutual capacitance, 489

mutual capacitor, 411–412

mutual-field line rings, 157–158, 160, 167, 170, 205

mutual inductance, 10–11, 41, 156–158, 171, 192, 411–412, 489

N

n-section lumped circuit model, 270–278, 411–412, 546–547

nanoseconds, 44, 63

Napier, John, 372

Napiers (nepers), 364, 372–373, 377–378

near-end cross talk, 10, 426, 463

coefficients, 438–441, 520

NEXT, 409–411

transmission lines, 429–433, 438–441

neck downs, 300, 306–308, 481

negative capacitance, 420–423

NelcoN6000SI, 353, 393

net inductance. *See* effective inductance

nets. *See* aggressor net

network theory, 259–260

NEXT, 40, 409–411

nH (nanoHenry), 155, 158, 176, 683–687

nickel, 119, 154, 202–203

noise, 3–4

budget, 178, 301, 440

cross talk, 9–11, 41

design principles, 41

differential, 540–542

EMI, 13–15, 41

rail-collapse, 11–13, 41, 184

signal quality, 4–9, 41

simultaneous switching output (SSO), 9–10

switching noise, 9–10

undershoot, 281

voltage, 617–618

See also attenuation; ground bounce; near-end cross talk; reflections; switching noise

nonmonotonicity, 3, 328

nonuniform transmission lines, 212–213, 228, 473

numerical simulations, 30–31, 34–35

Nyquist frequency, 604–605

O

OC (optical-carrier), 21, 476

odd mode, 502–506, 511–513

odd-mode characteristic impedance, 520, 546–550

odd-mode impedance, 411, 506–508, 520–522, 528–529, 551

odd-mode time delay, 411, 520

off-diagonal elements, 416, 420–424, 548, 551

ohmmeter, 234–235

Ohms, 117–118, 122

on-die capacitance, 637–639

orthonormal functions, 47

out-of-phase currents, 355–359

overshoot, 328

- P**
- P_{\max} , 626
 - package barrier, 639–644
 - package inductance, 631–632, 640–643, 715–716
 - parallel plate approximation, 131–132, 135, 347–348
 - parallel resonant frequency (PRF), 670–675
 - parallel resonant peak, 670–674
 - parameter values. *See* parasitic values
 - parasitic extraction tool, 34, 114
 - parasitic values, 87, 99
 - Paricon interposer, 594
 - partial inductance, 156, 161–166, 192
 - partial mutual inductance, 161–175, 191–192
 - partial self-inductance, 161–165, 169, 174, 176, 190, 192, 197
 - passive devices. *See* passive elements
 - passive elements, 24, 27–29, 102, 107–109
 - pattern-dependent noise. *See* inter-symbol interference (ISI)
 - PCBs, 121
 - PCI-express, 21
 - PDN (power distribution network), 12–13, 615–617
 - capacitor location effects, 703–707
 - capacitor mountings, 661–667
 - capacitor values, 675–681, 687–692
 - capacitors and SRF, 673–675
 - capacitors in parallel, 667–673
 - chip capacitors, 632
 - decoupling capacitors, 644–646, 699–703
 - design guidelines, 620
 - equivalent series inductance (ESL), 650–652, 681–687
 - equivalent series resistance (ESR), 668–673, 694, 711, 716
 - FDTI (frequency domain target impedance) method, 692–698
 - five parts of, 631–633
 - frequency ranges, 632
 - interconnects, 632
 - IR drop, 618
 - loop inductance and, 178–183
 - loop inductance approximations, 652–661
 - MLCC capacitor, 632, 646–650, 701, 711
 - on-die capacitance, 637–639
 - package barrier, 639–644
 - parallel resonant frequency (PRF), 670–675
 - primary functions, 616–617
 - ripple, 618–619, 623–630
 - spectrum, 618–619, 621–624
 - SPICE simulations, 635–637
 - spreading inductance, 704–710
 - target impedance, 619, 621–629
 - voltage, 178, 617–619
 - VRM (voltage regulator module), 633–635
 - peak impedance, 628, 641, 670–681, 712–716
 - peak resonant frequencies, 272
 - permeability of free space, 183, 217, 231
 - permeability of the conductor, 202–204
 - permittivity, 130–132, 136, 139–141, 217, 231, 250–251, 351, 359
 - pF, 130–132, 261, 311–317, 534
 - pH, 699–703
 - phase, 51, 96
 - phase shift, 94–98
 - Pi-termination, 525–528
 - pitch, 165–166, 232, 448, 451, 465, 499, 654
 - planes
 - capacitance, 677–681
 - with clearance holes, 187–188
 - ground, 82, 135–138, 184–188
 - loop inductance, 183–184
 - power, 135–137, 690–691
 - polyethylene, 134, 139, 353
 - Polyimide/glass, 134, 353, 393, 465
 - polymers, 133, 217–218, 352–353
 - port assignment labeling, 561–562
 - port impedance, 559, 573–574, 599
 - port indices, 598–599
 - power bounce, 3
 - power planes, 135–137, 690–691
 - power supply voltage, 11
 - PowerPoser, 693–698
 - PQFP (plastic quad flat pack), 25, 117
 - PRBS pseudo random bit stream, 611–613
 - pre-emphasis, 402–403

prepreg material, 450
 printed circuit board (PCB), 2
 propagation delay, 40, 82, 219, 227
 proximity effect, 488

Q

Q (resonance), 585–588
 Q3D field solver, 184
 quad flat pack (QFP), 212
 quarter wave stub resonance, 602–605
 quartz, 134
 quiet loop, 189, 470–471
 quiet net. *See* victim net

R

R_{equiv} , 525–528
 R_{shunt} , 361–362
 radians per second measurement, 49, 94
 radiated emissions, 15, 68, 535, 537–539, 578
 radiated field levels, 535–539
 radio frequency (rf), 46, 59
 rail collapse
 and C-Ply laminates, 13–14
 design principle, 41
 impedance and, 82–84
 noise, 11–13, 41, 184
 PDN, 178–183
 rail droop. *See* rail collapse
 reactance, 367, 370
 real versus ideal circuit elements, 86–88
 reflection coefficient, 283, 460–461, 521
 transmission lines and reflections, 284–290,
 293, 295, 300, 304, 307, 311–312, 589–
 593
 reflections, 3, 224
 capacitive end terminations, 311–313
 short-series transmission lines, 306–309
 See also transmission lines and reflections
 relative dielectric constant. *See* dielectric constant
 reorientation of electric dipoles, 349–351
 repeat frequency (F), 44, 52–55, 64–66, 70
 resistance
 bulk resistivity, 117–119
 conductivity, 118

 of interconnects, 115–117
 measurement, 117
 Ohms-length measurement, 118
 of 1-mil-diameter wire bond, 116
 physical basis, 113–115
 resistance per length, 119–121
 sheet resistance, 121–124
 resistor component technologies, 108–109
 resistor impedance, 88–89, 108
 resonances in the planes, 256
 return current distribution, 496–502
 return losses, 36, 386, 558, 562–565, 567–
 569, 571–573, 596
 return path, 139, 174, 177, 197, 210–214, 475
 gaps, 328, 542–544
 ground bounce, 249, 253
 transmission lines, 241–256
 reverse aspect ratio capacitors, 700
 RG58 coax cable, 139, 230
 RG174 coax cable, 230
 ribbon cable, 177–178, 198
 ringing, 3, 7, 67, 282, 293
 ripple, 178, 180, 574, 581, 601, 618–619,
 622–630
 rise time (RT), 219, 338–339, 518, 528–530
 bandwidth and, 43, 58–62
 and clock period estimates, 18, 68–70
 degradation, 395–398, 400–402
 distortion magnitude, 7
 intrinsic, 76–78
 laminate materials, 393
 10–90, 18, 45
 20–80, 45
 units of measurement, 63
 unterminated lines and, 304
 RLC circuit, 48, 100–102, 105, 648–649,
 668–669, 703
 rod over plane, 139–140, 263–264
 RogersRF35, 353, 393

S

S_{d} , 607–608
 S_{dB} , 560
 S_{s} , 607–608

- S11, 36, 386, 558, 562–565, 567, 596
- S21, 75, 386–390
 - differential insertion loss, 600–606
 - magnitude of, 577–582
 - phase of, 574–577
 - polar plot, 582–583
 - simulating, 567–570
- S22, 564–567, 597, 613
- S31, 563, 584, 595–596
- S32, 596
- S41, 563, 584, 596
- S42, 596
- S43, 584, 595–596
- S-parameters, 36
 - attenuation, 579–580
 - behavioral model, 555–556
 - common signals, 596–600
 - cross talk, 582–589
 - data mining, 594–596
 - dB and magnitude, 560, 571, 575, 588
 - differential, 596–609
 - dissipation factor, 580–582
 - insertion loss, 36, 75, 386–390, 567–570, 574–583
 - insertion loss, non-50-Ohm lines, 589–594
 - magnitude, 560, 562–565, 577–582
 - matrix elements, 562–567
 - mode conversion, 605–607
 - phase, 560–561, 563, 574–577
 - port, 559, 562
 - port assignment labeling, 561
 - port impedance, 559, 573–574, 599
 - port indices, 598–599
 - return loss, 36, 386, 558, 562–565, 567–569, 571–573, 596
 - reverse notation, 562
 - simulators, 569–570
 - sine waves, 559–560, 568–569, 576
 - single-ended, 596–600
 - time and frequency domains, 609–613
 - transform matrix, 607–609
 - transparent interconnect, 569–573
 - two-port device, 564–566
 - unique elements, 566–567
 - saturation length, 429–432, 439, 518
 - scalar network analyzer, 558
 - SCD11, 599, 606
 - SCD21, 599, 606–608
 - schematic, 26, 29, 99
 - SCSI bus, 476
 - sculpting the impedance profile, 687, 691–698
 - second-order model, 73–74, 100–101, 108, 165
 - self-field line rings, 157–159, 167–170, 194
 - self-inductance, 156–158, 192
 - self-resonant frequency (SRF), 181, 649–650, 668–675, 677–680
 - serial ATA, 21
 - series loop inductance, 327–331
 - series resistance, 49, 200, 342, 360–362, 365–368, 371, 378
 - sheet inductance, 183–184, 186, 656–661, 700
 - sheet resistance, 122–123
 - shield radius, 499–500
 - shielded twisted pair, 499–500, 537–538
 - shielding, 15
 - short-series transmission lines, 306–309
 - short-stub transmission lines, 309–311
 - shorting vias, 460–463
 - shunt conductance (G_L), 362–365, 367–368, 377–379
 - shunt impedance, 315–316
 - shunt resistance, 360–362
 - SIA (Semiconductor Industry Association), 17–18
 - Siemens, 118, 196
 - signal path, 138–139, 174, 177, 197, 210–214
 - signal-to-noise ratio (SNR), 49, 72
 - signal velocity, 369–371, 513–518
 - signal-voltage swing, 306, 329, 405, 440, 479, 483
 - significant waveforms, 63–66
 - silver, 119
 - silver-filled epoxy, 119
 - silver-filled glass, 119
 - silver plating, 204
 - simulations
 - AC simulations, 27
 - behavioral simulators, 24, 27

- simulations (*continued*)
 - circuit simulators, 24, 26–27
 - electromagnetic simulators, 24–25
 - Maxwell's Equations, 24–25
 - SPICE, 26–27
 - transient, 26–27
 - simultaneous switching noise (SSN), 9, 189, 616–617
 - simultaneous switching output (SSO), 9–10
 - sine waves
 - features, 49–55, 94
 - in frequency domain, 46–50
 - phase, 49, 94
 - ratio, 95
 - S-parameters, 559–560, 568–569, 576
 - in time domain, 50
 - single-ended characteristic impedance, 483–484, 489–491, 494, 500–501, 520, 546
 - single-ended impedance, 40, 484–486, 497–501
 - single-ended NEXT, 40
 - single-ended S-parameters, 596–600
 - single-ended signaling, 476, 491
 - single-ended transmission lines, 413, 480, 497, 520, 539–542, 596–598
 - skew, 8–9, 481, 529–533, 606
 - See also* time delay (TD)
 - skin depth, 193–201, 342–346, 352, 365–366
 - Smith, Larry, 694
 - SMT resistors, 107–109, 330–331
 - solder mask, 265–270, 509–510
 - source impedance, 290–292
 - source-series termination, 304–305, 334, 452–453, 460
 - spatial extent of leading edge, 219–220, 277
 - spectroscopy, 352, 588
 - spectrum, 66, 68
 - PDN (power distribution network), 618–619, 621–624
 - of a repetitive signal, 53–55
 - of a waveform, 51–53
 - to waveform conversion, 57
 - speed of light, 216–218, 234
 - sphere capacitance, 130–131
 - SPICE (Simulation Program with Integrated Circuit Emphasis)
 - capacitance matrix, 413–418, 421–423, 547–549
 - circuit theory and, 101–105
 - .FOUR command, 53
 - history, 26–27
 - impedance simulations, 635–637
 - transmission lines and reflections, 293–295
 - spreading inductance, 186, 653, 657, 662, 685, 704–710
 - square wave, ideal, 55–66
 - step edge, 72, 295, 557–558, 609–610
 - stripline
 - approximations, 266–268
 - broadside-coupled differential, 480, 498, 500
 - edge-coupled differential, 480, 493–494
 - interconnects, 141–143
 - stub resonance, 602–605
 - stubs, 309–311, 401, 602–605
 - Sun Microsystems, 12–13
 - superposition, 406–407
 - switching noise, 3, 9–10, 161, 469–473, 616–617
 - loop mutual inductance and, 471
 - reducing, 189, 469
 - See also* ground bounce
- T**
- tangent of the loss angle, 352, 354, 357–359, 385
 - tantalum capacitors, 631–634, 677
 - target impedance, 618, 621–629
 - TDA Systems IConnect, 37, 71
 - TD_{even}, 514, 549
 - TD_{odd}, 514, 548
 - TDR (time domain reflectometer), 10, 35–37, 71–72
 - DTDR (differential TDR), 521–523
 - measuring reflections, 295–299
 - response, 609
 - TDT (time domain transmitted) wave, 557–558, 610

- tee-termination, 525–529
- Teflon, 134, 353, 394, 581–582
- terminating resistors, 29, 107–108, 304–306
- terminating the line, 304
- termination topologies, 525–529
- terminations, 301–306, 311–313, 522–529
- time delay (TD), 529–530
 - cross talk and, 466–469, 514
 - delay adders, 233, 312–313, 317–320, 331–332
 - interconnect length and, 218–219
 - return paths, 241
 - transmission lines, 259–261, 271–272, 275–276, 301–304, 307–309
 - unloaded lines, 325–327
 - See also* skew
- time domain, 25–26
 - clock frequency and, 44
 - clock period and, 44–45
 - frequency domain and, 43
 - rise time and, 44–45
 - S-parameters (scattering parameters), 609–613
 - simulation, 102
 - sine waves, 51
 - waveform, 45, 53, 59, 66, 609–612
- timing, 3, 8–9, 466–469
- tin, 119
- total inductance. *See* effective inductance
- trace resistance, 121
- trace spacing, 457–464
- trade-off analysis, 30
- transfer function, 644
- transform matrix, 607–609
- transient current, 624–628
- transient simulation, 26, 102
- transistors, 45
- transmission coefficient, 284, 287
- transmission lines
 - balanced line, 213–214
 - characteristic impedance, 227–233
 - coupled, 413–417, 451–452
 - driving, 238–241
 - electron velocity, 214–215
 - first-order model, 257–262
 - ground line, 210
 - ideal transmission line, 106, 209–210, 270–274, 519–520
 - impedance, 233–238
 - input impedance, 234–238
 - kink of field, 216–217
 - lossless, 278–279
 - lumped circuit model, 270–278
 - nonuniform, 212–213, 228, 473
 - return paths, 210, 241–256
 - speed, 214–219
 - time delay, 218–219, 259–261, 271–272, 275–276, 301–304, 307–309
 - unbalanced line, 213–214
 - uniform, 212–214, 425–431, 473, 574–582
 - zeroth-order model, 224–227
 - See also* cross talk; differential pairs; lossless transmission lines; lossy transmission lines; transmission lines and reflections
- transmission lines and reflections
 - bounce diagrams, 292–294
 - capacitive delay adders, 317–319
 - capacitive discontinuities, 314–317, 324
 - capacitive end terminations, 311–313
 - compensation, 331–334
 - corners, 319–323
 - delay adders, 317–319, 324, 331–332
 - impedance discontinuities, 281–284
 - incident voltage, 285–288
 - loaded lines, 325–327
 - loop inductance, 327–331
 - negative voltage, 289
 - noise budget, 301
 - reflected voltage, 283, 288–289
 - reflection coefficient, 284–289, 295, 312
 - short-series, 306–309
 - short-stub lines, 309–311
 - source impedance, 290–292
 - source resistance, calculating, 292
 - SPICE, 293–296
 - TDR, 295–299
 - terminations, 301–306

transmission lines and reflections (*continued*)

- transmission coefficient, 287
- transmitted voltage, 285–287
- unintentional discontinuities, 299–301
- unterminated lines, 301–304
- vias, 323–324, 401

transparent interconnect, 569–573

tungsten, 119

twin rods, 139–140, 263

twinaX, 480

twisted pairs, 15, 230, 232–233, 480, 498, 539

U

unbalanced line, 213–214

undershoot noise, 281, 314–315, 317

uniform transmission lines, 212–214, 425–431, 473, 574–582

unshielded twisted pair, 500, 537, 607–608

unterminated lines, 301–304

V V_a , 438–439, 442–443, 446, 470–471, 519 V_b , 438–439, 519 V_{cc} , 12, 45, 173, 627–628 V_{comm} , 478–479, 511, 535–536 V_{dd} , 211, 617, 619, 624, 626 V_{ddq} , 627 V_{diff} , 477–479, 482, 484, 511 V_{even} , 511–512, 517–519 V_f , 442–446, 517–519 $V_{incident}$, 36, 283, 521, 576 V_{noise} , 161, 189, 624 V_{odd} , 511–512, 515–519 V_{PDN} , 619 $V_{reflected}$, 36, 283, 521 V_{ripple} , 619

vector, 558

vector-network analyzer (VNA), 35–36, 39, 386, 558–559

velocity, 369–371, 385–390, 429, 513–518

vias, 172–173

blind, 400, 605

buried, 400, 605

corners and, 319–324

loop inductance, 184–187, 661

 L_{via} , 387–388, 659–660, 685, 705

microvias, 605

shorting, 460–463

transmission lines and reflections, 323–324, 401

victim net, 9, 405, 427–429, 453–463, 466–468, 472, 541–542

voltage

capacitance and, 89–91, 127–128

difference, 476, 482, 511

drop, 11–12, 92–93, 168–169, 178–179

ground bounce, 168–169

incident, 285–288

inductance and, 158–161

instantaneous, 311, 428–429

negative, 289

noise, 617–618

PDN and, 178

polarity, 92, 160

rails, 135, 615, 620, 626–631

ratios, 377

reflected, 283, 288–289

transmitted, 285–287

voltage regulator module (VRM), 615, 619, 624, 631–635, 644–646, 711

volume resistivity, 119

 V_{ss} , 45, 173, 617**W**

waveforms

conversion, 57

frequency domain, 94

impulse, 557

impulse response, 609–612

significant, 63–66

step edge, 72, 295, 557–558, 609–610

time domain, 45, 53, 59, 66, 609–612

wavelets, 46

Webers, 153–155

wire bond, 73, 115–116, 120, 165–172

wire material composition, 154

www.beTheSignal.com, 672

X

XAUI, 22

X2Y Attenuators, 647, 650–651, 700–703

Z Z_{diff} , 484–486, 494, 507 Z_{even} , 508–509, 519, 524–527, 549, 552 Z_{odd} , 507, 519, 524–527, 548, 552 Z_{PDN} , 619, 624 Z_{peak} , 670–671 Z_{target} , 619, 621–629 Z_{cap} , 315–316 $Z_{\text{capacitors}}$, 681

zeroth harmonic, 56–60

zeroth-order model, 224–227, 242, 260