

Index

A

AC characteristics, 21
Amoeba technology, 99
Analog-digital converter (ADC), 23
Antenna Check, 87
ASIC, 1, 21, 22
Automatic Test Pattern Generation (ATPG), 27, 37
Automation, 54

B

Back end, 18, 81, 83, 93, 95
Ball Grid Array (BGA), 22
Binary coding, 126
Block-based design, 105–106
Boolean function, 137

Boundary scan, 37–38
Buffer-tree network, 103
Built-In Self Test (BIST), 15, 27, 37
Bus-interconnect, 117
Bus-invert (BI) coding, 127

C

CAD tools, 84
Clock design, 90
Clock-gating, 27
Clock-tree synthesis, 103
CMOS power dissipation, 114
Code coverage, 51
Code excited linear prediction (CELP), 5, 121
Control flow analysis, 48

Crosstalk, 85, 86
CVS, 54

D

Data flow analysis, 48, 61
DC characteristics, 21
Deep submicron (DSM), 95
Delay calculation, 18
Design analysis, 32
Design flow, 10, 25
Design for integration, 44
Design for test (DFT), 15, 27, 37–40, 53
Design methodology, 16
Design partitioning, 100
Design Rule Check (DRC), 86
Design rule constraints, 26
Design validation, 34
Detail routing, 84
Device Under Test (DUT), 39
DFT sign-off, 87
Digital signal processing (DSP), 5, 73, 121
Digital-analog converter (DAC), 23
Dual in-line, 22
Dynamic power dissipation, 113, 116

E

EDA tools, 84
EDIF, 32

Electromigration, 86
Electrical Rule Check, 87
Embedded array, 32
Ethernet, 4
External interface emulation, 48

F

FIFO, 59, 78
Finite-impulse-response (FIR) filter, 121
Finite-state-machine (FSM) encoding, 124
Flip flop, 23, 130–131
Floorplanning, 17, 81–82, 98, 106–107
FPGA to ASIC conversion, 32–33
Front end, 17, 82, 93, 95
Full-timing-delay model, 143
Functional sign-off, 87
Functional simulation, 25

G

Gate array, 32
Gate-level tools, 144
GDSII, 8, 18, 84
Glitch, 27, 128
Global bus design, 91
Global positioning system (GPS), 135
Global routing, 84–85
Gray coding, 126, 127

H

Hamming distance, 124, 127
HDL, 25, 49
Hierarchical layout block, 89
Hierarchical logic blocks (HLB), 28
Hierarchical methodology, 27, 92
Hierarchical techniques, 100
HW/SW integration, 49
HW/SW partitioning, 121

I

In-place optimization (IPO), 103
Intellectual Property (IP), 1, 7–12
 firm IP, 9
 hard IP, 8
 soft IP, 9
Interface Logic Models (ILM), 27
IP verification, 53–55
IR drop, 85, 103

J

JTAG standard, 37–38

K

Karnaugh map, 136

L

Latch, 23, 129, 130
Layout versus Schematic (LVS), 87
Leakage Current, 115
Lint tools, 25
Logical hierarchy, 99
Low-power design, 111, 119
Low-power design flow, 119
Low-power techniques, 117

M

Makefiles, 54
Memory partitioning, 133
Memory optimization, 132–133
Mesh-based clocking, 84
Methodology, 94
MicroNetwork, 14
Modeling methodology, 73
Modern physical design, 93
MPEG, 2, 5, 65, 73
MPEG Processor, 66
Multiple supply voltage, 122

N

New Design Flow, 96
NMOS, 87

O

On-chip bus (OCB), 44
 On-chip interconnect, 6
 On-chip processor, 1
 Open Core Protocol (OCP), 15, 71,
 159–164
 Optimization techniques, 85
 architecture-level, 122
 algorithm-level, 121
 RT-level, 124
 gate-level, 136

P

Partial-bus-invert (PBI) coding,
 127
 Partitioning, 108
 Physical compiler, 27
 Physical design, 6, 18–19, 81–82
 physical design flow, 82
 modern physical design, 93
 Physical hierarchy, 89
 Physical prototype, 96
 Physical sign-off, 87
 Physical synthesis, 102
 Physical verification, 86
 Pin Grid Array (PGA), 22
 Pin assignment rules, 23
 Place and route, 18
 Multiple place and route, 92
 Placement-based synthesis, 27, 87

PLL, 23, 165–171
 PLL basics, 165
 PLL ideal behavior, 166
 PLL errors, 168
 PMOS, 87
 Post-routing, 85
 Power analysis, 26
 Power consumption, 22, 99
 Power dissipation, 112
 Power estimation, 138–140
 Power grid design, 103
 Power management, 133–136
 Power on-off, 23
 Power optimization, 118
 algorithm-level, 121
 architecture-level, 122
 clock gating, 124
 de-glitching, 128
 memory, 132–133
 RT-level, 124
 signal encoding, 124
 gate-level, 136
 Power-optimization tools, 140
 behavior-level, 142
 gate-level, 144
 transistor-level, 144
 Power supply (V_{DD}), 115
 Power estimation, 26
 Power reduction, 26
 Pulse code modulation (PCM), 5

Q

Quad flat pack (QFP), 22

R

RC extraction, 27
RCS, 54
Regression planning, 49
Resource sharing, 60
Reuse methodology, 19
RISC, 78
Round-Robin Arbitration, 76
RTL coding, 25

S

Set-Top Box (STB), 5, 56, 57
STB characteristics, 58
Short-circuit current, 116
Short-circuit power dissipation,
113, 115
Signal integrity, 85–86
Silicon Ensemble, 86
Silicon virtual prototype, 94, 97,
104
SiliconBackplane, 14, 45, 56, 60
Simulation-based power estimation,
138–140
Sleep mode, 133
Small outline package (SOP), 22
SOC, 1
SOC verification, 47–52
SPICE, 37–38
STAMP models, 27
Standard delay format (SDF), 17,
100

Standard-cell technologies, 32
Static power dissipation, 113, 115
Static timing analysis (STA), 16,
27, 50
system mode, 30
test mode, 30
Supply voltage, 22
Surface-mount, 22
Switched capacitance, 117
Switching activity, 117, 123
Synthesis, 25
logic synthesis, 25
placement-based synthesis, 27,
87
System partitioning, 63

T

Tapeout, 18
Test Access Port (TAP), 37–38
Testbenches
BFM-based, 35
C-based, 35
vector-based, 35
Time-to-market (TTM), 19, 47, 111
Timing analysis, 6, 27
Timing closure, 93–94, 98
Timing Optimization, 85, 86
Timing sign-off, 87
Transistor-level tools, 144
Turn Around Time (TAT), 12
degree of difficulty, 24
Two's complement, 123

U

Unit-delay model, 143
Utopia, 4, 6, 67

V

Verification, 104, 109
 analog mixed-signal (AMS),
 36–37
 assertion-based verification
 (ABV), 36
 code coverage, 36
 emulation, 37
 formal verification, 36
 functional verification, 35
 simulation, 35
 testbenches, 35
Verification planning, 48
Verilog, 9, 25, 32, 36, 49, 53, 117,
 144
Version control, 54
VHDL, 9, 25, 32, 36, 49, 50, 53,
 144

Virtual component (VC), 7
Virtual component interface (VCI),
 15
Voice over IP (VoIP), 1, 44, 45, 58
Voltage drop, 85
Voice over Network (VoN), 121

W

Wire-load models (WLM), 25, 96

X

Xilinx Netlist Format (XNF), 32

Z

Zero-delay model, 143